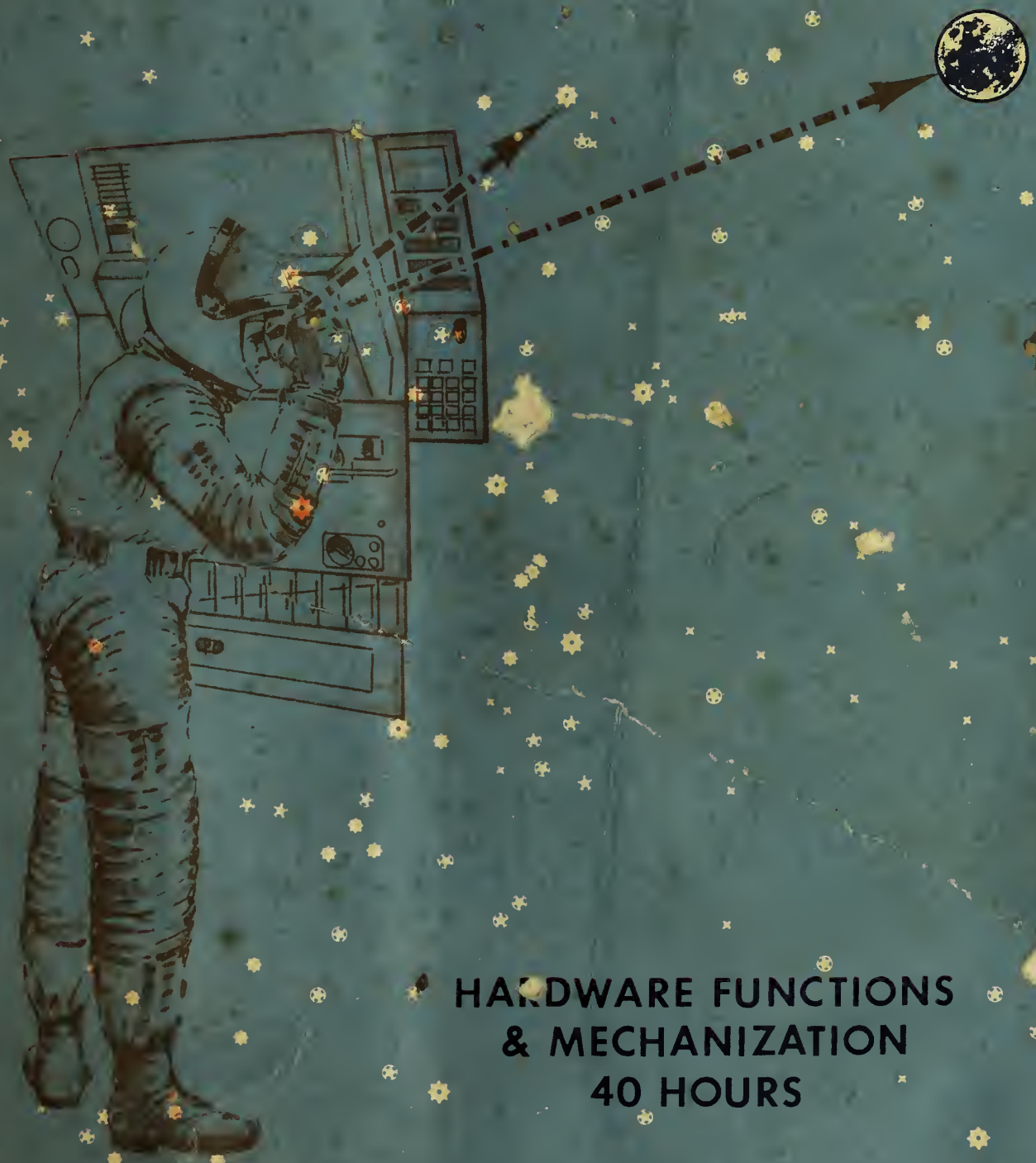
John B. Mortimer
3-17-66

APOLLO GUIDANCE AND NAVIGATION SYSTEM STUDY GUIDE

BLOCK 1 (SERIES 100) G&N SYSTEM COURSE



HARDWARE FUNCTIONS & MECHANIZATION 40 HOURS

AC ELECTRONICS DIVISION

GENERAL MOTORS CORPORATION

APOLLO

GUIDANCE & NAVIGATION SYSTEM

BLOCK I (SERIES 100)

STUDENT STUDY GUIDE

GUIDANCE & NAVIGATION SYSTEM COURSE 1100

G&N HARDWARE FUNCTIONS AND MECHANIZATION FH1100

PREPARED BY

AC ELECTRONICS

DIVISION OF GENERAL MOTORS

MILWAUKEE, WISCONSIN

1 AUGUST 1965

REVISION A
31 JANUARY 1966

PREFACE

This student study guide has been prepared by AC Electronics in response to:

Contract Change Order 42 to NAS 9-497

for

System Assembly and Test, Inertial

Measurement Unit, Coupling Display Unit

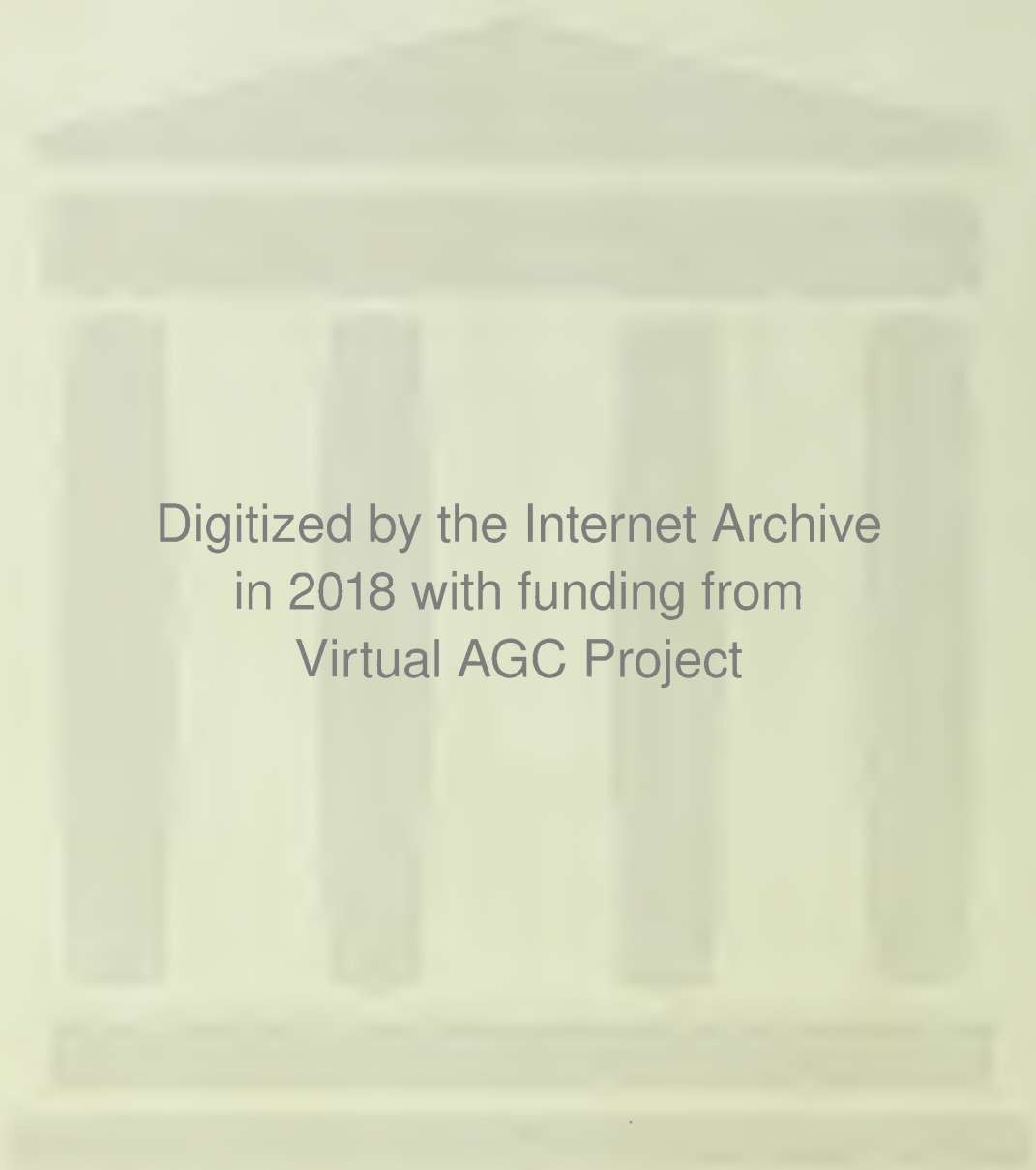
Power and Servo Assembly - Project APOLLO

This study guide contains training material and should be used for instructional purposes only.

TABLE OF CONTENTS

		Page
Section I	Introduction to the G&N System	1-1
Block 1.1	Guidance and Navigation Requirements	1-1
1.1.1	Inertial Guidance	1-1
1.1.2	Optical Navigation	1-1
Block 1.2	G&N System Interface	1-1
1.2.1	Spacecraft Systems Interface	1-1
1.2.1.1	Stabilization and Control System	1-1
1.2.1.2	Service Propulsion System	1-4
1.2.1.3	Reaction Control Systems	1-4
1.2.1.4	Electrical Power System	1-4
1.2.1.5	Environmental Control System	1-5
1.2.1.6	Communication and Instrumentation System	1-5
1.2.2	Astronaut Interfaces	1-5
Block 1.3	G&N Systems	1-6
1.3.1	G&N System Equipment	1-6
1.3.2	Inertial Subsystem	1-8
1.3.3	Optical Subsystem	1-11
1.3.4	Computer Subsystem	1-11
Block 1.4	G&N System Functions and Relation to Mission Phases	1-12
1.4.1	Prelaunch IMU Alignment	1-12
1.4.2	Guidance Monitor	1-12
1.4.3	Oribtal Navigation	1-12
1.4.4	Inflight IMU Alignment	1-12
1.4.5	Injection	1-18
1.4.6	Midcourse Navigation	1-18
1.4.7	Midcourse Correction	1-18
1.4.8	Entry	1-18
1.4.9	Attitude Control	1-18
Block 1.5	Summary	1-18
	Review Questions for Section I	1-24
Section II	Introduction to the Inertial Subsystem	2-1
Block 2.1	ISS Purpose	2-1
Block 2.2	ISS Equipment	2-1
Block 2.3	ISS Functional Blocks	2-3
2.3.1	Navigation Base	2-3
2.3.2	Inertial Measurement Unit Structure	2-3
2.3.3	Temperature Control and Indicator Circuits	2-3
2.3.4	Stabilization Loop	2-5
2.3.5	Coarse Align Amplifiers	2-5
2.3.6	Fine Align Torquing Electronics	2-5

		Page
2.3.7	Accelerometer Loops	2-5
2.3.8	Coupling Display Units and Electronics	2-6
2.3.9	Resolving Network	2-6
2.3.10	Lower Display and Control Panel	2-6
2.3.11	Main Display and Control Panel	2-7
2.3.12	Power Supplies	2-7
2.3.13	Malfunction Detection Circuits	2-7
2.3.14	Mode Switching Circuit	2-7
Block 2.4	Summary	2-7
	Review Questions for Section II	2-8
Section III	Description and Mechanization of the Inertial Measurement Unit	3-1
Block 3.1	IMU Gimbal Assemblies	3-1
3.1.1	Stable Member	3-1
3.1.2	Inter-Gimbal Assembly	3-1
3.1.3	Middle Gimbal	3-3
3.1.4	Outer Gimbal	3-3
3.1.5	Gimbal Case	3-3
Block 3.2	Axes	3-3
Block 3.3	Stabilization Loop	3-13
3.3.1	Stabilization Loop Operation	3-13
3.3.2	Stabilization Loop Mechanization	3-13
3.3.2.1	25 Inertial Reference Integrating Gyro	3-16
3.3.2.2	Angular Differentiating Accelerometer	3-18
3.3.2.3	ADA Preamplifier	3-22
3.3.2.4	25 IRIG Preamplifier	3-22
3.3.2.5	Gimbal Servo Amplifier	3-22
3.3.2.6	Torque Motors	3-22
Block 3.4	Gyro Torquing Operation	3-24
3.4.1	Ternary Current Switch	3-24
3.4.2	Calibration Module	3-24
Block 3.5	Accelerometer Loop	3-29
3.5.1	Accelerometer Loop Operation	3-29
3.5.2	Accelerometer Loop Mechanization	3-29
3.5.2.1	16 PIP	3-29
3.5.2.2	AC Differential Amplifier	3-32
3.5.2.3	Interrogator	3-32
3.5.2.4	Binary Current Switch	3-33
3.5.2.5	Calibration Module	3-33
3.5.2.6	Constant Current Source	3-36
3.5.2.7	Forward-Backward Counter	3-36
Block 3.6	Summary	3-37
	Review Questions for Section III	3-41



Digitized by the Internet Archive
in 2018 with funding from
Virtual AGC Project

https://archive.org/details/apolloguidancena00acel

TABLE OF CONTENTS (cont)

		Page
Section IV	Coupling Display Unit	4-1
Block 4.1	Coupling Display Unit	4-1
Block 4.2	Coupling Display Unit Operation	4-1
4.2.1	Digital Encoder	4-5
4.2.2	Encoder Electronics	4-5
4.2.3	Digital to Analog Converter	4-5
Block 4.3	CDU Mechanization for Inertial Subsystem	4-7
Block 4.4	Summary	4-7
	Review Questions for Section IV	4-9
Section V	ISS Modes of Operation	5-1
Block 5.1	Modes of Operation	5-1
Block 5.2	Mode Control	5-1
Block 5.3	ISS Premoding Conditions	5-1
5.3.1	Standby	5-1
5.3.2	IMU Turn-On	5-2
Block 5.4	Mode Mechanization	5-2
5.4.1	Zero Encoder	5-2
5.4.2	Coarse Align	5-2
5.4.3	Manual CDU	5-5
5.4.4	Fine Align	5-5
5.4.5	Attitude Control	5-8
5.4.6	Entry Mode	5-11
Block 5.5	Summary	5-13
5.5.1	Zero Encoder	5-13
5.5.2	Coarse Align	5-13
5.5.3	Manual CDU	5-13
5.5.4	Fine Align	5-13
5.5.5	Attitude Control	5-13
5.5.6	Entry	5-13
	Review Questions for Section V	5-14
Section VI	Temperature Control System	6-1
Block 6.1	IMU Temperature Control System	6-1
6.1.1	Modes of Operation	6-1
6.1.1.1	Auto Override Position	6-1
6.1.1.2	Proportional Position	6-1
6.1.1.3	Backup Position	6-1
6.1.1.4	Emergency Position	6-3
6.1.2	Temperature Sensors	6-3

		Page
6.1.3	Heating Elements	6-3
6.1.4	Amplifiers	6-3
6.1.5	Indications, Test Points and Self-Checks	6-5
Block 6.2	Proportional Temperature Control Circuit	6-5
Block 6.3	Backup Temperature Control Circuit	6-5
Block 6.4	Emergency Control Circuit	6-9
Block 6.5	Indicator Circuit	6-9
Block 6.6	Temperature Control System Operation	6-9
Block 6.7	Summary	6-12
	Review Questions for Section VI	6-13
Section VII	Display and Control Group	7-1
Block 7.1	Lower Display and Control Panels	7-1
Block 7.2	IMU Control Panel	7-1
7.2.1	Transfer Switch	7-1
7.2.2	Mode Control Switch Assembly	7-1
7.2.3	IMU-CDU Difference Meter	7-1
7.2.4	Manual Align Button	7-1
Block 7.3	Display and Control Electronics	7-5
7.3.1	Panel Brightness Control	7-5
7.3.2	100-Second Time Delay	7-5
7.3.3	Demodulator Circuit	7-5
Block 7.4	G&N Indicator Control Panel	7-5
7.4.1	IMU Temperature Control Group	7-5
7.4.1.1	Temperature Control Mode Selector	7-8
7.4.1.2	Zero Pushbutton	7-8
7.4.1.3	IRIG Gain Pushbutton	7-8
7.4.1.4	PIPA Gain Pushbutton	7-8
7.4.2	Check Coolant	7-8
7.4.3	Attitude Impulse Control	7-8
Block 7.5	Condition Annunciator Assembly	7-8
Block 7.6	Main Display and Control Panels	7-8
Block 7.7	Summary	7-9
	Review Questions for Section VII	7-10

TABLE OF CONTENTS (cont)

		Page
Section VIII	ISS Power and Power Distribution	8-1
Block 8.1	ISS Power Supplies	8-1
8.1.1	-28 Volt DC Supply	8-1
8.1.2	Pulse Torquing DC Supply	8-1
8.1.3	800 CPS Power Supplies	8-4
8.1.4	25.6 KCPS Power Supply	8-4
8.1.5	3,200 CPS Power Supplies	8-4
Block 8.2	Power and Servo Assembly	8-8
8.2.1	Module Packaging	8-8
8.2.1.1	Cordwood Packaging	8-8
8.2.1.2	Heat Sink Packaging	8-8
Block 8.3	PSA Junction Box	8-14
Block 8.4	Summary	8-14
	Review Questions for Section VIII	8-15
Section IX	Signal Monitoring and Conditioning	9-1
Block 9.1	Signal Monitoring and Detection	9-1
9.1.1	Failure Detection	9-1
9.1.2	Condition Annunciator	9-3
Block 9.2	Signal Conditioner Assembly	9-5
9.2.1	Signal Conditioner Modules	9-5
9.2.2	Signal Conditioner Power Supplies	9-7
9.2.3	Inputs	9-7
9.2.4	Torque Motor Module	9-7
9.2.5	CDU Resolver Module	9-7
9.2.6	Scaling Module	9-9
9.2.7	IRIG and PIPA Module	9-9
9.2.8	Gimbal Resolver Module	9-9
9.2.9	Optics Module	9-9
Block 9.3	Summary	9-9
	Review Questions for Section IX	9-10
Section X	Introduction to the Optical Subsystem	10-1
Block 10.1	OSS Purpose	10-1
Block 10.2	OSS Equipment	10-1
Block 10.3	OSS Functional Blocks	10-3
10.3.1	Navigation Base	10-3
10.3.2	Telescope	10-3
10.3.3	Sextant	10-3
10.3.4	Shaft and Trunnion Drive	10-3

		Page
10.3.5	Shaft and Trunnion Repeaters	10-5
10.3.6	Drive Rate Resolution Circuit	10-5
10.3.7	Shaft Cosecant Normalization Circuit	10-5
10.3.8	Mode Switching	10-5
10.3.9	Display and Control Subsystem Operations	10-5
10.3.10	Power Supplies	10-5
Block 10.4	Summary	10-6
	Review Questions for Section X	10-7
Section XI	Optical Subsystem Equipment Description	11-1
Block 11.1	Optical Unit Assembly	11-1
11.1.1	Optical Base	11-1
11.1.2	Scanning Telescope	11-1
11.1.2.1	Double Dove Prism	11-7
11.1.2.2	Objective Lens Assembly	11-7
11.1.2.3	Reticle	11-7
11.1.2.4	Pechan Prism	11-7
11.1.2.5	Relay Lens Assembly	11-7
11.1.2.6	Eyepiece Window and Prism Assembly	11-11
11.1.2.7	SCT Eyepiece Assembly	11-11
11.1.2.8	SCT Optics Light Transmission	11-11
11.1.3	Sextant	11-11
11.1.3.1	Indexing Mirror Assembly	11-13
11.1.3.2	Right Angle Mirrors	11-13
11.1.3.3	Beam Splitter	11-13
11.1.3.4	SXT Telescope Optics	11-13
11.1.3.5	SXT Eyepiece Assembly	11-13
11.1.3.6	SXT Optics Light Transmission	11-13
11.1.4	Optical Subsystem Axes	11-15
Block 11.2	Associated Optical Equipment	11-15
11.2.1	Navigation Base	11-15
11.2.2	Bellows	11-17
11.2.3	G&N Indicator Control Panel	11-17
11.2.4	Coupling Display Units	11-19
11.2.5	Power and Servo Assembly	11-19
Block 11.3	Summary	11-19
	Review Questions for Section XI	11-21
Section XII	Optical Subsystem Mechanization	12-1
Block 12.1	Optical Loop Mechanization	12-1

		Page
Block 12.2	Modes of Operation	12-3
12.2.1	Zero Optics Mode	12-3
12.2.2	Manual Mode Operation	12-3
12.2.2.1	Manual Direct Operation	12-3
12.2.2.2	Manual Resolved Operation	12-7
12.2.2.3	Slave Telescope Modes	12-7
12.2.3	Computer Mode Operation	12-7
Block 12.3	Summary	12-11
	Review Questions for Section XII	12-12
Section XIII	Introduction to the Apollo Guidance Computer	13-1
Block 13.1	Brief AGC Functional Description	13-1
13.1.1	AGC Capabilities	13-1
Block 13.2	Brief AGC Physical Description	13-4
13.2.1	Logic Tray A	13-4
13.2.2	Memory Tray B	13-4
Block 13.3	AGC Organization	13-7
13.3.1	Timer	13-7
13.3.2	Sequence Generator	13-7
13.3.3	Central Processor	13-7
13.3.4	Memory	13-7
13.3.5	Priority Control	13-7
13.3.6	Input - Output	13-7
13.3.7	Power	13-7
Block 13.4	Pertinent AGC Characteristics	13-9
Block 13.5	AGC Information Flow	13-9
Block 13.6	Summary	13-12
	Review Questions for Section XIII	13-13
Section XIV	Apollo Guidance Computer	14-1
Block 14.1	Word Formats	14-1
14.1.1	Data Words	14-1
14.1.2	Instruction Words	14-1
Block 14.2	Addition Schemes	14-3
14.2.1	Non-Angular Data Addition	14-3
14.2.2	Angular Data Addition	14-3
Block 14.3	Logic Implementation	14-9

		Page
Block 14.4	Hardware Registers	14-13
14.4.1	Storage Element	14-13
14.4.2	Hardware Register Interface	14-15
Block 14.5	Timer	14-19
14.5.1	Clock Countdown	14-19
14.5.2	Scaler A	14-19
14.5.3	Scaler B	14-19
14.5.4	Time Pulse Generator	14-25
14.5.5	Start/Stop Logic	14-25
Block 14.6	Central Processor	14-25
14.6.1	G Register	14-25
14.6.2	Write Amplifiers	14-25
14.6.3	S Register and Bank Register	14-29
14.6.4	SQ Register	14-31
14.6.5	Z Register	14-31
14.6.6	A, LP and Q Registers	14-31
14.6.7	B Register	14-31
14.6.8	Adder	14-31
14.6.9	Parity Block	14-34
14.6.10	Basic Data Flow	14-38
Block 14.7	Memory	14-38
14.7.1	Erasable Memory	14-40
14.7.1.1	Core Application	14-40
14.7.1.2	Core Array	14-40
14.7.1.3	Addressing Erasable Memory	14-44
14.7.2	Fixed Memory	14-49
14.7.2.1	Core Application	14-49
14.7.2.2	Fixed Memory Layout	14-51
14.7.2.3	Addressing Fixed Memory	14-53
Block 14.8	Sequence Generator	14-60
14.8.1	Instructions	14-60
14.8.1.1	Regular Instructions	14-61
14.8.1.1.1	Instruction TC K (Order Code 0)	14-61
14.8.1.1.2	Instruction CCS K (Order Code 1)	14-61
14.8.1.1.3	Instruction NDX K (Order Code 2)	14-61
14.8.1.1.4	Instruction XCH K (Order Code 3)	14-61
14.8.1.1.5	Instruction CS K (Order Code 14)	14-63
14.8.1.1.6	Instruction TS K (Order Code 15)	14-63
14.8.1.1.7	Instruction AD K (Order Code 16)	14-63
14.8.1.1.8	Instruction MSK K (Order Code 17)	14-63
14.8.1.1.9	Instruction MP K (Order Code 11)	14-63
14.8.1.1.10	Instruction DV K (Order Code 12)	14-63
14.8.1.1.11	Instruction SU K (Order Code 13)	14-63
14.8.1.2	Involuntary Instructions	14-63
14.8.1.3	Miscellaneous Instructions	14-63

		Page
14.8.2	Sequence Generator Operations	14-65
14.8.2.1	Regular Instruction Execution	14-65
14.8.2.2	Involuntary Instruction Execution	14-68
14.8.2.2.1	Program Priority	14-68
14.8.2.2.2	Counter Instructions	14-71
14.8.2.3	Miscellaneous Instruction Execution	14-71
14.8.2.4	Branching	14-71
14.8.2.5	Instruction Flow	14-71
Block 14.9	Priority Control	14-75
14.9.1	Counter Priority Control	14-75
14.9.2	Interrupt Priority Control	14-77
14.9.2.1	T3RUPT Routine	14-80
14.9.2.2	RUPT 2	14-80
14.9.2.3	T4RUPT Routine	14-83
14.9.2.4	KEYRUPT Routine	14-83
14.9.2.5	UPRUPT Routine	14-83
14.9.2.6	DNRUPT Routine	14-83
Block 14.10	Input-Output	14-83
14.10.1	The AGC's Input Registers	14-84
14.10.1.1	IN 0 Register	14-84
14.10.1.2	IN 1 Register	14-86
14.10.1.3	IN 2 Register	14-86
14.10.1.4	IN 3 Register	14-88
14.10.2	The AGC's Output Registers	14-90
14.10.2.1	OUT 0 Register	14-90
14.10.2.2	OUT 1 Register	14-90
14.10.2.3	OUT 2 Register	14-93
14.10.2.4	OUT 3 Register	14-94
14.10.2.5	OUT 4 Register	14-94
14.10.3	Output Drive Pulses of the AGC	14-98
14.10.3.1	Program Controlled Drive Pulse Outputs	14-98
14.10.3.2	Continuous Drive Pulse Outputs	14-100
14.10.4	Telemetry Inputs and Outputs	14-100
14.10.4.1	Uplink Telemetry Inputs	14-100
14.10.4.2	Downlink Telemetry Outputs	14-103
14.10.5	AGC Malfunctions	14-107
14.10.5.1	Program Detected Malfunctions	14-107
14.10.5.2	Circuit Detected Malfunctions	14-109
Block 14.11	Power	14-110
Block 14.12	Summary of AGC Data Flow	14-112
Block 14.13	Summary	14-112
	Review Questions for Section XIV	14-113

		Page
Section XV	Display and Keyboard Functional Description	15-1
Block 15.1	Navigation Panel DSKY Keyboard	15-1
Block 15.2	Main Panel DSKY Keyboard	15-1
Block 15.3	Navigation Panel DSKY Display	15-6
Block 15.4	Main Panel DSKY Display	15-12
Block 15.5	DSKY Condition and Alarm Indicators	15-12
Block 15.6	DSKY Power Supply	15-15
Block 15.7	Summary	15-15
	Review Questions for Section XV	15-18
Section SVI	DSKY Operational Procedure	16-1
Block 16.1	CSS/Astronaut	16-1
Block 16.2	Verb-Noun List	16-5
16.2.1	Verb Codes	16-6
16.2.1.1	Ordinary Verbs	16-6
16.2.1.2	Extended Verbs	16-7
16.2.2	Verb Descriptions	16-8
16.2.2.1	Ordinary Verbs	16-8
16.2.2.2	Extended Verbs	16-9
16.2.3	Noun Codes	16-10
16.2.3.1	Normal Nouns	16-10
16.2.3.2	Mixed Nouns	16-12
16.2.3.3	Noun Scale Factors	16-13
16.2.4	Noun Descriptions	16-14
16.2.4.1	Normal Nouns	16-14
16.2.4.2	Mixed Nouns	16-15
Block 16.3	Summary	16-16
	Review Questions for Section XVI	16-17
Appendix		Appendix-1
Answers to Section I Review Questions		Appendix-11
Answers to Section II Review Questions		Appendix-11
Answers to Section III Review Questions		Appendix-12
Answers to Section IV Review Questions		Appendix-13
Answers to Section V Review Questions		Appendix-13

Page

Answers to Section VI Review Questions Appendix-14
Answers to Section VII Review Questions Appendix-14
Answers to Section VIII Review Questions Appendix-15
Answers to Section IX Review Questions Appendix-15
Answers to Section X Review Questions Appendix-16
Answers to Section XI Review Questions Appendix-16
Answers to Section XII Review Questions Appendix-16
Answers to Section XIII Review Questions Appendix-17
Answers to Section XIV Review Questions Appendix-17
Answers to Section XV Review Questions Appendix-17
Answers to Section XVI Review Questions Appendix-17

LIST OF ILLUSTRATIONS

Figure		Page
1-1	Guidance and Navigation Requirements	1-2
1-2	Guidance and Navigation System Interface	1-3
1-3	Guidance and Navigation Equipment	1-7
1-4	Location of Guidance and Navigation Equipment in the Spacecraft	1-9
1-5	Guidance and Navigation Subsystem Data Flow	1-10
1-6	Mission Phases Required for a Lunar Orbit	1-13
1-7	Prelaunch Alignment	1-15
1-8	Orbital Navigation Sighting	1-16
1-9	IMU Alignment Measurement	1-17
1-10	Midcourse Position Determination	1-19
1-11	Midcourse Navigational Measurement	1-20
2-1	Inertial Subsystem Equipment	2-2
2-2	Inertial Subsystem Interface	2-4
3-1	Stable Member	3-2
3-2	Support Structure and IMU Gimbals	3-4
3-3	Intergimbal Assembly	3-5
3-4	IMU Gimbal Assembly and Gimbal Axes	3-6
3-5	Stable Member Axes	3-7
3-6	25 IRIG Axes	3-7
3-7	16 PIP Axes	3-7
3-8	ADA Axes	3-8
3-9	Middle Gimbal Axes	3-8
3-10	Outer Gimbal Axes	3-9
3-11	Gimbal Case Axes	3-9
3-12	Navigation Base Axes	3-10
3-13	Spacecraft Axes	3-10
3-14	Spacecraft, IMU and Nav-Base Axes	3-11
3-15	Inner Gimbal Angle	3-12
3-16	Middle Gimbal Angle	3-12
3-17	Outer Gimbal Angle	3-12
3-18	Stabilization Loop	3-14
3-19	Gyro Error Resolver	3-15
3-20	25 IRIG (Generalized Pictoroal Schematic)	3-17
3-21	Signal Ducosyn	3-19
3-22	Torque Ducosyn	3-20
3-23	Angular Differentiating Accelerometer	3-21
3-24	Gimbal Servo Amplifier	3-23
3-25	Ternary Current Switch, Block Diagram	3-25
3-26	Calibration Circuit	3-26
3-27	Torquing Loop (IRIG)	3-27
3-28	IRIG Torquing Loop Pulse Relationship	3-28
3-29	Accelerometer Loop	3-30
3-30	16 PIP	3-31
3-31	Pulse Diagram - PIPA Loop	3-34
3-32	Interrogator	3-35
3-33	Binary Current Switch, Block Diagram	3-38

Figure		Page
3-34	Forward-Backward Counter, Loop Diagram	3-39
4-1	Coupling Display Panel	4-2
4-1a	Coupling Display Unit	4-2
4-2	Resolver Gimbal Angle Indicator Servo	4-3
4-3	CDU Digital Encoder	4-4
4-4	Digital to Analog Converter	4-6
4-5	CDU Functional Diagram	4-8
5-1	Zero Encoder Mode Mechanization	5-3
5-2	Coarse Align Mechanization (Inner Gimbal)	5-4
5-3	Manual CDU Mode Mechanization (Inner Gimbal)	5-6
5-4	Fine Align Loop (Inner Gimbal)	5-7
5-5	Attitude Control Mode Mechanization (Inner Gimbal)	5-9
5-6	Attitude Error Transformation	5-10
5-7	Entry Mode (Outer Gimbal)	5-12
6-1	Forced Convection Cooling System	6-2
6-2	Temperature Control Unit	6-4
6-3	Temperature Mode Control	6-6
6-4	Proportional Temp. Control Mode in Auto Override Position	6-7
6-5	Temp. Control - Backup Mode	6-8
6-6	Emergency Temp. Control Mode in Emergency Position S-16	6-10
6-7	Zero and Gain Switch Circuitry to Alarm Amplifier	6-11
7-1	Lower D & C Panels	7-3
7-2	IMU Control Panel	7-4
7-3	D & C Electronics	7-6
7-4	G&N Indicator Control Panel	7-7
8-1	Inertial Power Supplies	8-2
8-2	-28 VDC Supply	8-3
8-3	Pulse Torque Power Supply	8-3
8-4	800 CPS Supplies	8-5
8-5	25.6 KCPS Supply	8-6
8-6	3200 CPS Power Supplies	8-7
8-7	PSA Tray Module Location	8-9
8-8	PSA Tray	8-10
8-9	G&N Harness and Junction Box	8-11
8-10	Cordwood Module	8-12
8-11	Heat Sink Module	8-13
9-1	Failure Detection Circuitry	9-2
9-2	Condition Annunciator	9-4
9-3	Signal Conditioner	9-6
9-4	Signal Conditioner Power Supplies	9-8

Figure		Page
10-1	Optical Subsystem Equipment	10-2
10-2	Optical Subsystem Interface	10-4
11-1	Optical Unit Cutaway	11-2
11-2	Vertical Optical Limits	11-3
11-3	Scanning Telescope Cutaway	11-4
11-4	Sextant Cutaway	11-5
11-5	SCT Optical Schematic	11-6
11-6	SCT Gearing	11-8
11-7	Differential Gear Assembly	11-9
11-8	Pechan Prism	11-10
11-9	SXT Optical Schematic	11-12
11-10	Motion of Indexing Mirror	11-14
11-11	Optical Unit, Navigation Base and Bellows	11-16
11-12	G&N Indicator Control Panel	11-18
11-13	CDU Block Diagram	11-20
12-1	Optics Mechanization	12-2
12-2	Zero Optics Mode	12-4
12-3	Manual Direct Mode	12-5
12-4	Sextant Image Motion	12-6
12-5	Manual Resolved Mode	12-8
12-6	Gain Variation - Simplified Diagram	12-9
12-7	Computer Mode	12-10
13-1	Apollo Guidance Computer	13-2
13-2	Display and Keyboards	13-3
13-3	Logic Tray A	13-5
13-4	Memory Tray B	13-6
13-5	AGC Block Diagram	13-8
14-1	Word Formats	14-2
14-2	Number Representation	14-4
14-3	Addition Schemes for Non-Angular Data	14-5
14-4	+ $\Delta\theta$ Pulse Addition	14-8
14-5	- $\Delta\theta$ Pulse Addition	14-10
14-6	Logic Symbology	14-11
14-7	Basic Storage Element and Associated Waveforms	14-14
14-8	Hardware Register Interface	14-16
14-9	Register Data Transfer #1	14-17
14-10	Register Data Transfer #2	14-18
14-11	Clock Countdown	14-20
14-12	Binary Divider #1 Output Waveforms	14-21
14-13	Binary Divider #2 and Ring Counter Waveforms	14-22
14-14	Scaler A	14-23
14-15	Scaler B	14-23
14-16	Time Pulse Generator and Associated Waveforms	14-26
14-17	Start/Stop Logic	14-27
14-18	G Register Interface	14-28
14-19	Address Determination Scheme #1	14-29
14-20	Address Determination Scheme #2	14-29
14-21	Adder Block Diagram	14-32
14-22	Adder (Bit Position 1)	14-33

Figure		Page
14-23	Parity Logic and G Register Interface	14-35
14-24	Sample G Register Configuration	14-37
14-25	Parity Logic Signal Timeline	14-37
14-26	Parity Block Inputs #1	14-37
14-27	Parity Block Inputs #2	14-37
14-28	Central Processor Block Diagram	14-39
14-29	Erasable Memory Core Threading	14-41
14-30	Erasable Memory Core Array	14-42
14-31	Bit Plane Threading	14-43
14-32	Erasable Memory Block Diagram	14-45
14-33	"X" Selection Steering	14-47
14-34	Selection of "X" Plane	14-48
14-35	Hypothetical Rope Core	14-50
14-36	AGC Fixed Memory Layout	14-52
14-37	Set Line Selection Logic	14-55
14-38	Strand Line Selection Logic	14-56
14-39	Strand Gate Selection Logic	14-58
14-40	Fixed Memory Organization and Selection	14-59
14-41	BANK Register and Fixed Memory Bank Relationship	14-57
14-42	Sequence Generator Flow Diagram	14-66
14-43	Hypothetical Crosspoint Matrix	14-69
14-44	Inhibit Interrupt	14-70
14-45	Branching	14-72
14-46	TC0	14-73
14-47	STD2	14-74
14-48	Counter Priority Control	14-78
14-49	Counter Input Interface Flow Diagram	14-79
14-50	Program Interrupt Priority Control	14-82
14-51	IN 0 Register Bit Assignments	14-85
14-52	IN 2 Register Bit Assignments	14-87
14-53	IN 3 Register Bit Assignments	14-89
14-54	OUT 0 Register Bit Assignments	14-91
14-55	OUT 1 Register Bit Assignments	14-92
14-56	OUT 2 Register Bit Assignments	14-95
14-57	OUT 4 Register Bit Assignments	14-96
14-58	Input-Output Bit Assignments	14-97
14-59	Development and Control of Program Controlled Drive Pulse Outputs	14-99
14-60	Uplink Interface Flow Diagram	14-102
14-61	Uplink Word Format	14-104
14-62	Telemetry Timing	14-105
14-63	Downlink Formats	14-106
14-64	Downlink Converter Interface Flow Diagram	14-108
14-65	Power Supplies	14-111

Figure		Page
15-1	Navigation Panel Display and Keyboard	15-2
15-2	Main Panel Display and Keyboard	15-3
15-3	DSKY Keyboard and Associated Keycodes	15-4
15-4	Navigation Panel DSKY Indicators	15-7
15-5	Digit Indicator Relay Logic	15-8
15-6	Sign Indicator Relay Logic	15-9
15-7	DSKY Read and Command Relay Circuitry	15-10
15-8	DSKY R Relay Usage	15-11
15-9	Main Panel DSKY Indicators	15-13
15-10	Navigation Panel DSKY Alarm Circuitry	15-16
15-11	Main Panel DSKY Alarm Circuitry	15-17

LIST OF TABLES

Table		Page
1-1	G&N System Functions per Mission Phase	1-14
3-1	Logic Table, Forward-Backward Counter	3-40
7-1	D & C Panel Switches	7-2
13-1	Pertinent AGC Characteristics	13-10
14-1	Angular Data Representation	14-7
14-2	Scaler A Outputs	14-24
14-3	Addressing	14-30
14-4	Address Decoder Outputs	14-46
14-5	Fixed Memory Selection Signals	14-54
14-6	Regular Instructions	14-62
14-7	Involuntary Instructions	14-64
14-8	Miscellaneous Instructions	14-64
14-9	Sequence Generator Codes	14-67
14-10	Counter Interrupts	14-76
14-11	Program Interrupts	14-81
14-12	Continuous Drive Pulse Outputs	14-101

OBJECTIVES

The intent of this study guide is to give the student a basic understanding of the G & N System Block I (Series 100) hardware mechanization. The computer hardware input/output interface section is intended to tie together the system hardware. The computer control and operation of the system is described in the Computer Program Study Guide C1100.

This study guide is used in conjunction with the G & N System Hardware Course No. FH1100. The study guide will be presented to the student on the first day of the course and retained by the student after the course as a reference document. Maximum white space is available throughout the study guide to accommodate the student's class notes.

The study guide is organized in the sequence of instruction of the course and is divided into 16 major sections. Each section contains the documentation and copies of the visual aids used during the class presentation of the section. A summary and review questions are included at the end of each section, to be used by the student for review and self-evaluation. The answers to the review questions are located in the appendix.

The objectives of this study guide are to provide the student with:

a. The course materials organized in the sequence of classroom presentation for self-study.

b. A list of references for further self-study.

c. Section summaries for reviewing.

d. Review questions for self-evaluation.

REFERENCES

The following documents were used in the preparation of this study guide:

ND-1021037	Apollo Guidance and Navigation System Familiarization Manual
ND-1021068	Optical Unit
ND-1021001	Computer Subsystem
ND-1021036	Guidance and Navigation System
LED-540-12	Design Reference Mission Apollo Mission Planning Task Force
R-477	Guidance and Navigation System Operations Plan
R-467	The Complete Sunrise Being a Description of Program Sunrise
DG Memo No. 330	Navigator's Check List (Preliminary)
1015560	Apollo Inertial Subsystem One Line Mechanization Drawing
1009502	Functional Diagram (Optical Subsystem Block I-100)
1017510	IMU Temperature Control Block I (Series 100) Print
1015560	Stabilization Loop One Line Mechanization Print
1015562	Stabilization Loop Two Line Mechanization Print
1015561	PIPA Loop Two Line Mechanization Loop
R-500	Space Navigation, Guidance and Control
1009502	Functional Diagram Optics Subsystem Block I (100)
1009512	Two Wire Mechanization Optics Block I (100)

SECTION I

INTRODUCTION TO THE G&N SYSTEM

INTRODUCTION

This section develops the G&N requirements for the Apollo mission, describes the relationship of the G&N system to the spacecraft and the astronaut, and briefly describes the G&N functions as related to the Apollo lunar orbit mission phases.

1.1 GUIDANCE AND NAVIGATION REQUIREMENTS

The Apollo G&N system performs two basic functions: inertial guidance and optical navigation as shown in figure 1-1. These two basic functions are described below:

1.1.1 INERTIAL GUIDANCE. The inertial guidance portion of the G&N system employs accelerometers mounted on a gyroscopically stabilized gimbal-mounted platform and a central data processing element. The inertial guidance system senses acceleration and attitude changes instantaneously and provides attitude control and thrust control signals to the stabilization and control system.

1.1.2 OPTICAL NAVIGATION. The optical navigation portion of the G&N system employs a scanning telescope and sextant to make sightings of celestial bodies and landmarks on the surface of the moon and earth. These sightings are used by the central data processing element to:

a. Determine the spacecraft position and velocity.

b. Establish proper alignment of the stable platform.

A digital computer serves as the central data processing element of the G&N system. It contains a catalog of celestial bodies and is programed to calculate steering, thrust and alignment commands using the information obtained from the optical sightings and the inertial measurement unit. The computer uses data on gravitational fields and celestial perturbations to calculate future position and velocity of the spacecraft.

1.2 G&N SYSTEM INTERFACE

The Apollo G&N system has direct interfaces with six spacecraft systems: the stabilization and control system (SCS), service propulsion system (SPS), reaction control system (RCS), electrical power system (EPS), environmental control system (ECS), and the communication and instrumentation system (C&IS). The G&N system interface with the various spacecraft systems is illustrated in figure 1-2 and described in the paragraphs below.

1.2.1 SPACECRAFT SYSTEMS INTERFACE.

1.2.1.1 Stabilization and Control System. The stabilization and control system (SCS) is located in the command module and can sense and control spacecraft attitude and velocity changes during any phase of flight. Steering and thrust signals can be generated either by the stabilization and control system or the G&N system. The signals are processed and conditioned by the stabilization and control system and used to operate the reaction control and service propulsion systems.

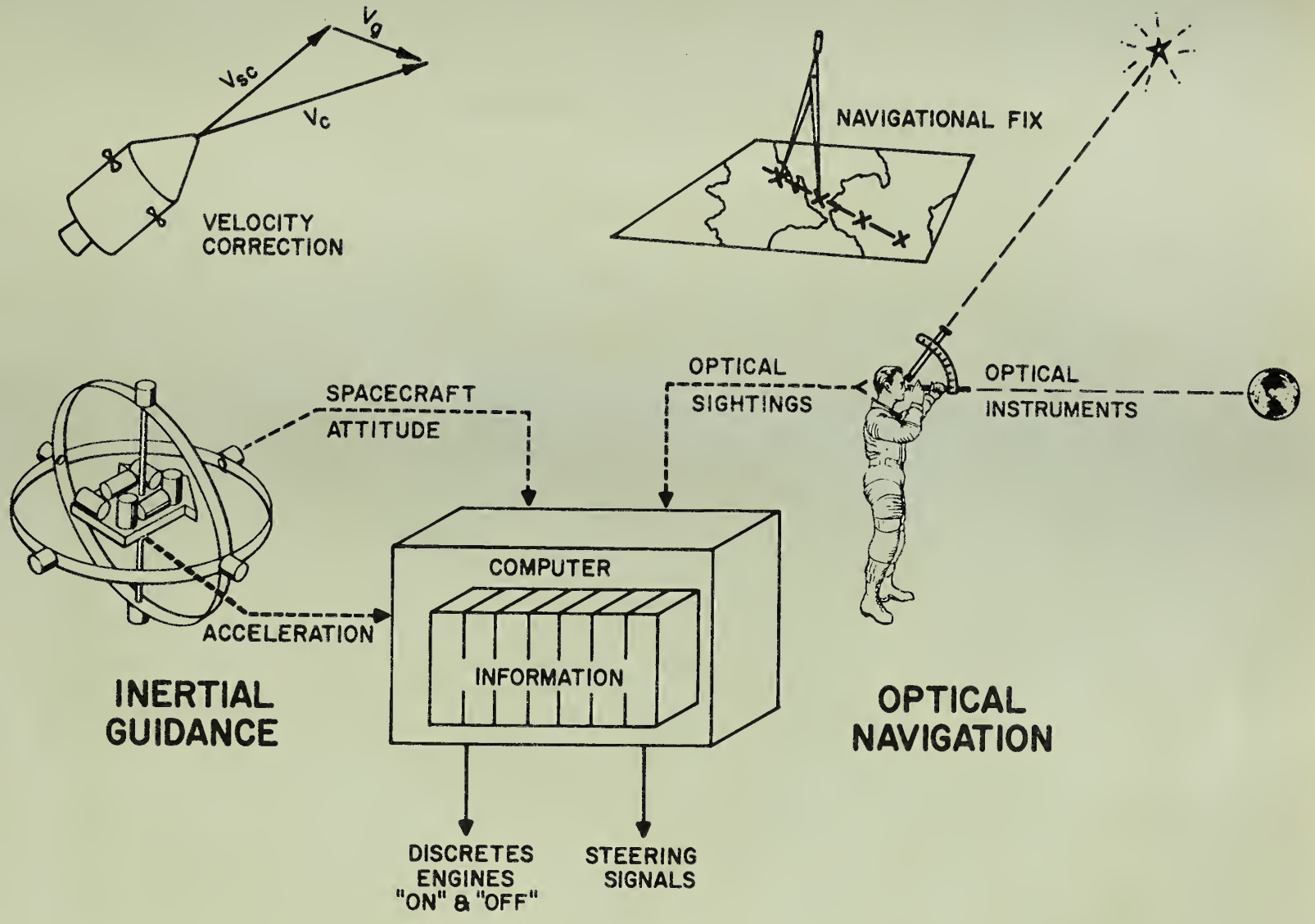


Figure 1-1. Guidance and Navigation Requirements

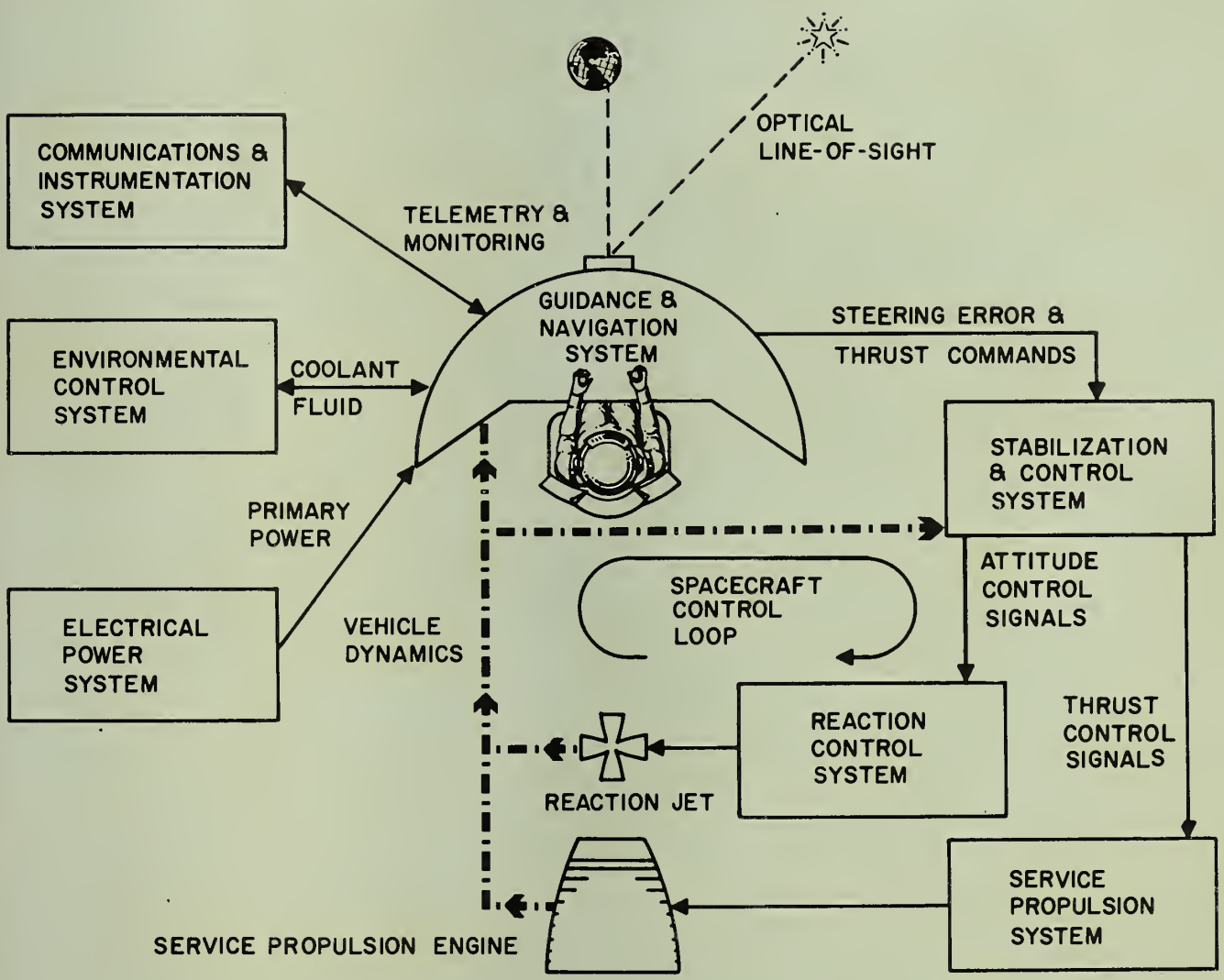


Figure 1-2. Guidance and Navigation System Interface

The stabilization and control system consists of a rate gyro package, an attitude gyro accelerometer package, electrical control assemblies, attitude gyro coupler unit and various displays and controls. The stabilization control can hold the spacecraft attitude to a local vertical by using orbital rates or to a specific attitude by using reference gyros mounted to the spacecraft body. Information about attitude and attitude rate of change of the spacecraft is displayed to the flight crew.

Interface signals from the G&N system to the stabilization and control system consist of attitude control signals, thrust commands, mode control and attitude data for display.

1.2.1.2 Service Propulsion System. The service propulsion system (SPS) provides the thrust capability to change the spacecraft's velocity. The system is normally operated by the G&N system through the stabilization control system, but can be operated directly in emergencies.

The service propulsion system is utilized for mission abort, midcourse velocity corrections and orbital injections. The system is located in the service module and consists of helium, fuel and oxidizer storage tanks, a gimbaled thrust chamber, propellent control valves and distribution equipment. The service propulsion system operates on a helium-pressurized hypergolic propellant and is capable of developing 21,900 pounds of thrust. The gimbal mechanism allows the thrust chamber to be displaced 0 $\pm 6^{o}$ in pitch and 4 $\pm 8^{o}$ in yaw.

1.2.1.3 Reaction Control Systems. Two reaction control systems (RCS) are utilized for attitude control and stabilization of the spacecraft. The systems also can be operated by the G&N system through the stabilization control system. One reaction control system is required for the command module and another for the service module. Each system consists of helium, fuel and oxidizer tanks, propellent control valves, fixed thrust chambers and distribution equipment.

The reaction control system of the command module consists of two independent, and equally capable, pressurized reaction jet subsystems. The two subsystems are operated simultaneously and provide three-axis control of the command module. In event one reaction jet subsystem fails, the remaining reaction jet subsystem is capable of providing the control necessary for safe entry. The reaction jet subsystem provides four engine nozzles for each type of maneuver - roll, pitch and yaw. Each of the 12 engines develops a nominal thrust of 100 pounds and they exhaust through ports flared into the skin of the command module. The engines are located in the aft equipment and forward parachute compartments of the command module.

The service module reaction control system consists of four equally capable hypergolic propellent pressurized reaction jet subsystems. The subsystems are located in the forward section of the service module and are mounted 90^{o} apart. Each subsystem has four engine nozzles. Eight of the 16 nozzles are used for roll control, four for pitch and four for yaw. Each nozzle provides a nominal thrust of 100 pounds.

1.2.1.4 Electrical Power System. The primary power required to operate the G&N system is supplied by a hydrox fuel cell in the service module and is used during all mission phases except entry and recovery. Three zinc-silver oxide storage batteries in the command module furnish power during entry and recovery.

The hydrox fuel cell contains three independent modules, operating in parallel and capable of producing a 27 to 31 volt dc output which is converted by a solid state inverter into 115 volt, 400 cycle power, and together these are used for normal G&N system operation. In case of an emergency, any two modules could meet all power requirements. The modules utilize hydrogen and oxygen as the reactants and potassium hydroxide as the electrolyte. The reactants are stored in tanks that are part of the cryogenic gas storage system which also furnishes oxygen to the environmental control system. The water formed by operating the fuel cells is collected and delivered to the environmental control system as potable water.

Auxiliary electrical power is provided by the three batteries in the command module. Two of these batteries supply supplementary power during peak loads on the fuel cell. The third battery is isolated from the electrical power system and is used only for post-landing loads. A solid state battery charger is provided to recharge any of the three batteries after normal or emergency discharge.

1.2.1.5 Environmental Control System. An environmental control system (ECS) is used to sustain life in space. The system provides breathable atmosphere, acceptable temperatures, food and water, waste disposal and radiation protection. The Apollo environmental control system is essentially a storage type in which the life support elements (breathable gasses, water, food, etc.) are stored and used as needed, and the waste products collected and stored for disposal. However, some features of a regenerative system in which usable material is extracted from the metabolic waste are used in the Apollo environmental control system, especially in the conservation of water.

The environmental control system provides an atmosphere of 100 percent oxygen at approximately 5 psia. Cabin temperature is maintained between 70 and 80°F. and relative humidity between 50 and 60 percent. In addition, a water-glycol coolant fluid is circulated about the temperature sensitive components of the G&N system and other spacecraft systems for thermal stability. In the event of cabin decompression, the crew pressure suits supply a conditioned oxygen atmosphere of 3.5 psia.

1.2.1.6 Communication and Instrumentation System. The Apollo communication and instrumentation system (C&IS) provides voice, television and telemetry communications with the earth and voice communications between crew members. A television system permits ground viewing of external and remote sections of the spacecraft during flight. Telemetry data can be stored when direct communication with the earth is not possible because of the location of earth communication facilities or because the spacecraft is behind the moon. The earth stations can determine spacecraft position and transmit this information to the crew to supplement information obtained from onboard navigational systems. Critical signals of the G&N system are conditioned and supplied to pulse code modulated (PCM) telemetry equipment for transmission to ground stations. Data transmitted from earth stations can be loaded into the G&N system.

1.2.2 ASTRONAUT INTERFACES. The astronaut is an active and controlling part of the G&N system. He is able to monitor information to and from the G&N system and can manually duplicate G&N system control functions. The astronaut activities are classified into the following five types:

a. Take Optical Sighting: The astronauts identify and select celestial objects on which optical sightings are taken. The sightings are used to align the inertial reference and determine spacecraft position.

b. Monitor System Performance: Mode, condition, and failure lights are monitored by the astronauts to determine system status. As calculations are performed by the computer, the results are displayed for astronaut evaluation and verification with ground calculated data.

c. Load Data: Data is loaded into the computer through the computer keyboard by the astronaut. The data consists of such information as star selection, positional data and system angles.

d. Select Mode of Operation: The astronaut, by means of the displays and controls, can select the equipment modes of operation for the different spacecraft systems required to perform a particular function. In some cases, the sequencing of modes is controlled by the computer. The major mode or program being performed by the computer can be selected by the astronaut or initiated internally by the computer.

e. Provide System Backup: In case of G&N system failure, the astronaut provides manual control of the spacecraft and performs those functions normally performed by the G&N system.

1.3 G&N SUBSYSTEMS

The G&N system is divided into three major subsystems: inertial (ISS), optical (OSS) and computer (CSS). The G&N system is designed so that each subsystem can be operated independently during an emergency or backup mode. Therefore, the failure of one subsystem will not place the entire G&N system out of commission. The three subsystems, or combinations of subsystems, with assistance from the astronaut can perform the following functions:

a. Periodically establish an inertial reference which is used for measurements and computations.

b. Align the inertial reference by precise optical sightings.

c. Calculate the position and velocity of the spacecraft by optical navigation and inertial guidance.

d. Generate attitude error signals and thrust commands necessary to maintain the required spacecraft trajectory.

e. Provide the astronaut with a display of data which indicates the status of the guidance and navigation problem.

1.3.1 G&N SYSTEM EQUIPMENT.

The G&N system equipment (figure 1-3) consists of a navigation base (NB), inertial measurement unit (IMU), optical assembly, power and servo assembly (PSA), Apollo guidance computer (AGC), display and control panel, and coupling display units (CDU's).

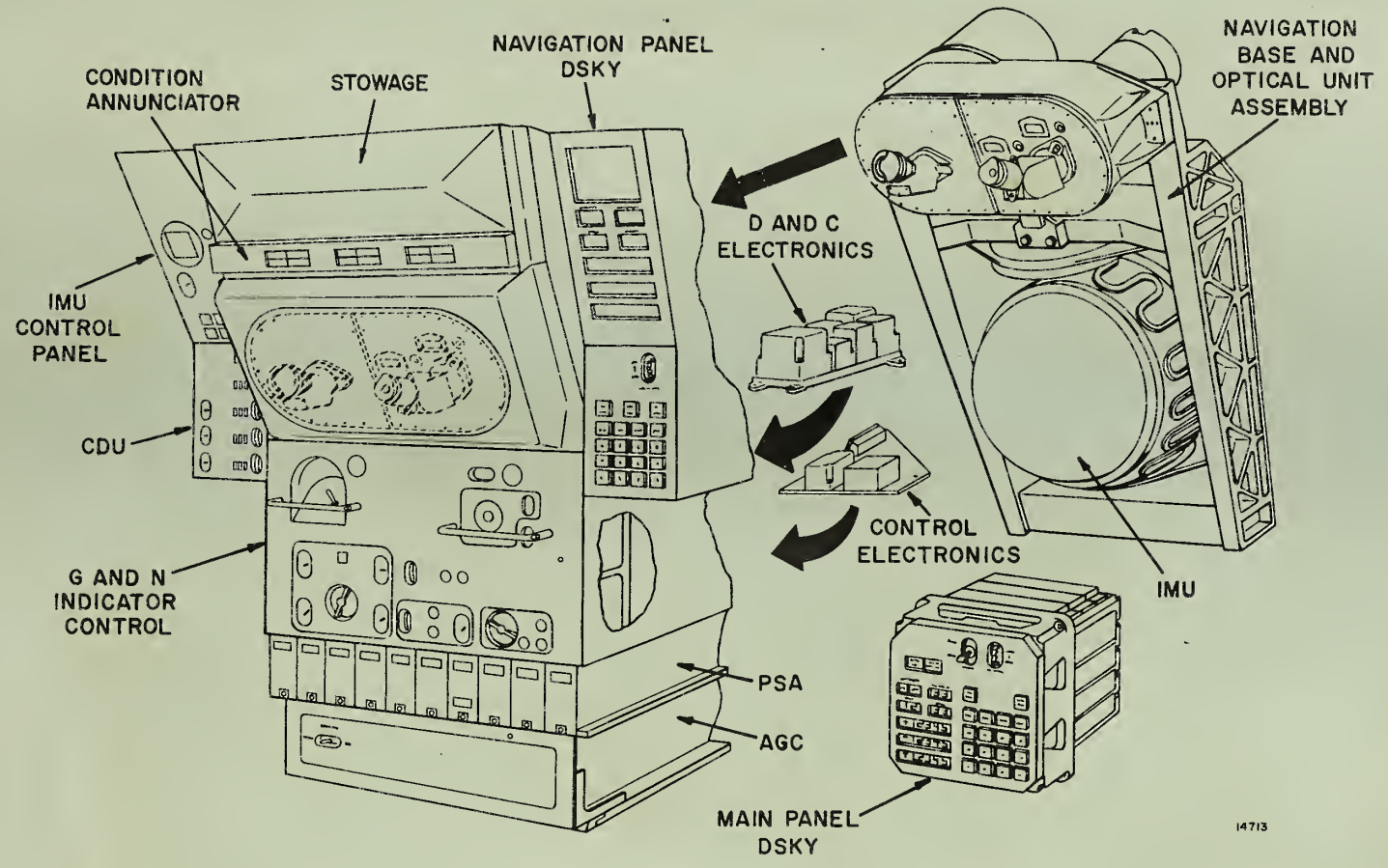


Figure 1-3. Guidance and Navigation Equipment

Figure 1-4 shows the G&N system equipment installed in the spacecraft. The navigation base is mounted to the spacecraft sidewall and used as a holding fixture for the IMU and optical assembly. The IMU and optical assembly are attached and precisely aligned to the navigation base. The display and control panel comprises the front of the G&N structure and contains several individual panels. These panels are located so that the astronaut can view and manually operate them from a standing position. The CDU's are also mounted in the display and control panel. The PSA, which contains power supplies, amplifiers and miscellaneous electronics, is located on a shelf below the navigation base. The PSA consists of ten trays which plug into a PSA junction box. The AGC is located on a shelf below the PSA and consists of one tray which plugs into an AGC junction box.

The following paragraphs present a brief functional description of the three G&N subsystems. Figure 1-5 illustrates the signal flow and interface between the subsystems.

1.3.2 INERTIAL SUBSYSTEM. The inertial subsystem consists of the IMU mounted on the navigation base, three CDU's, portions of the PSA, and portions of the lower display and control panel.

The inertial subsystem is used in spacecraft guidance to determine the direction and magnitude of the required velocity correction applied to the spacecraft. To conserve fuel, velocity corrections are kept to a minimum and are applied only periodically. Therefore, electrical power also can be conserved by limiting the use of the inertial subsystem to about 20 percent of the flight time.

The inertial subsystem performs three major functions: (1) measures changes in spacecraft attitude, (2) assists in generating steering commands and (3) measures spacecraft velocity changes due to thrust. To accomplish these functions, the IMU provides an inertial reference consisting of a stable member gimbaled in three degrees of freedom and stabilized by three integrating gyros. Each time the inertial subsystem is energized, the stable member must be aligned with respect to a predetermined reference. When the inertial subsystem is operated prior to launch, the stable member is aligned through a gyro compassing routine and, during flight, it is aligned by sighting the optical instruments on celestial objects. If the inertial subsystem is operated over a prolonged period of time, realignment may be necessary since the gyros which maintain the space referenced stable member may drift and cause an error in flight calculations.

Once the inertial subsystem is energized and aligned, any rotational motion of the spacecraft will be about the gimbaled stable member, which remains rotationally fixed in space. Resolvers, mounted on the gimbal axes, act as angular sensing devices and measure the attitude of the spacecraft with respect to the stable member. These angular measurements are displayed to the astronauts by the CDU's and angular changes are sent to the AGC.

The required gimbal angles to change the spacecraft attitude are calculated in the AGC and compared with the actual gimbal angles. Any difference between the actual and calculated angles causes an attitude error signal to be generated in the inertial subsystem. The error signal is sent to the stabilization control system to correct the spacecraft attitude.

Acceleration of the spacecraft is sensed by three pendulous accelerometers mounted on the stable member with their input axes orthogonal. The resultant signals from the accelerometers are supplied to the AGC which then calculates the total velocity.

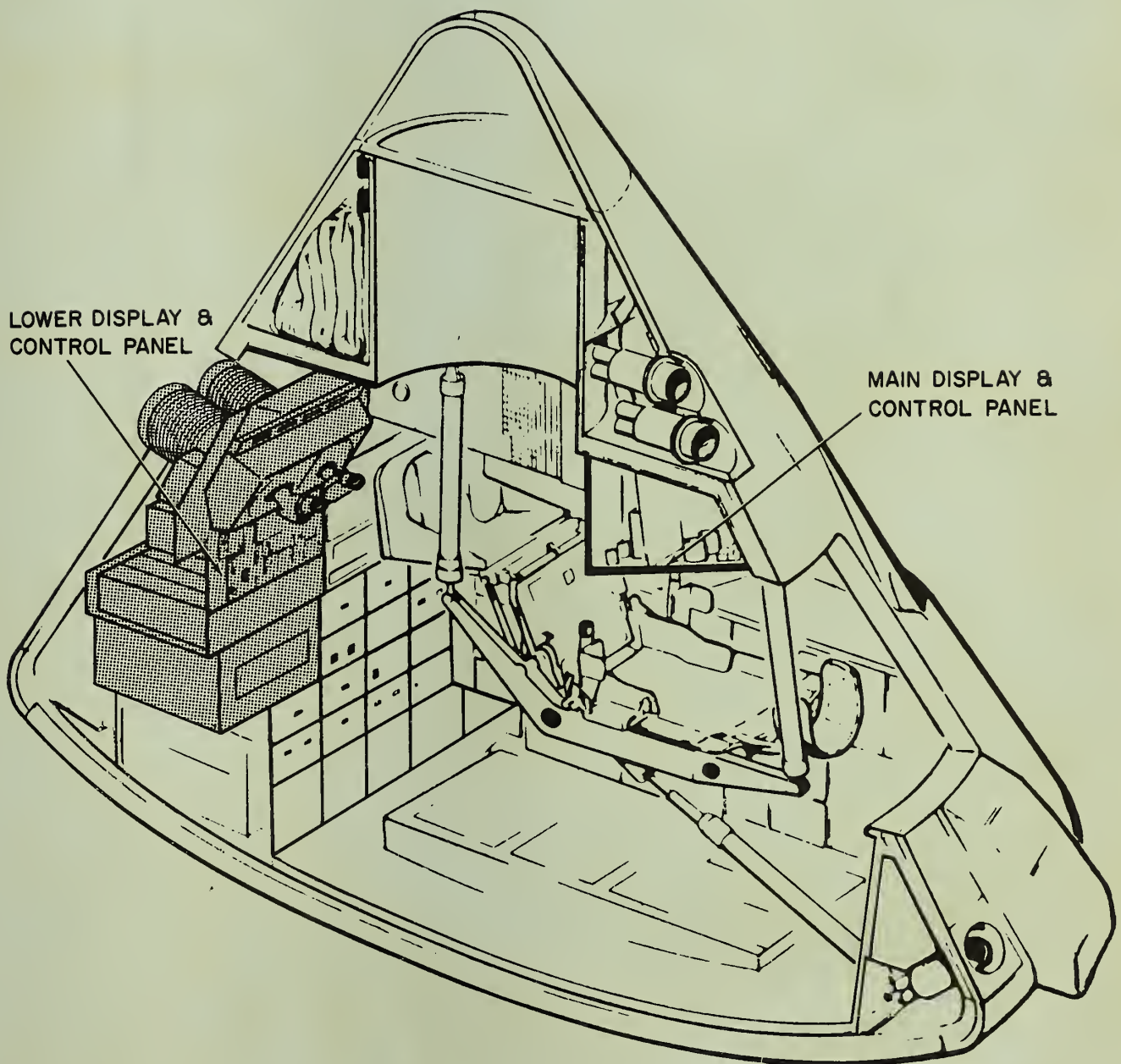


Figure 1-4. Location of Guidance and Navigation Equipment in the Spacecraft

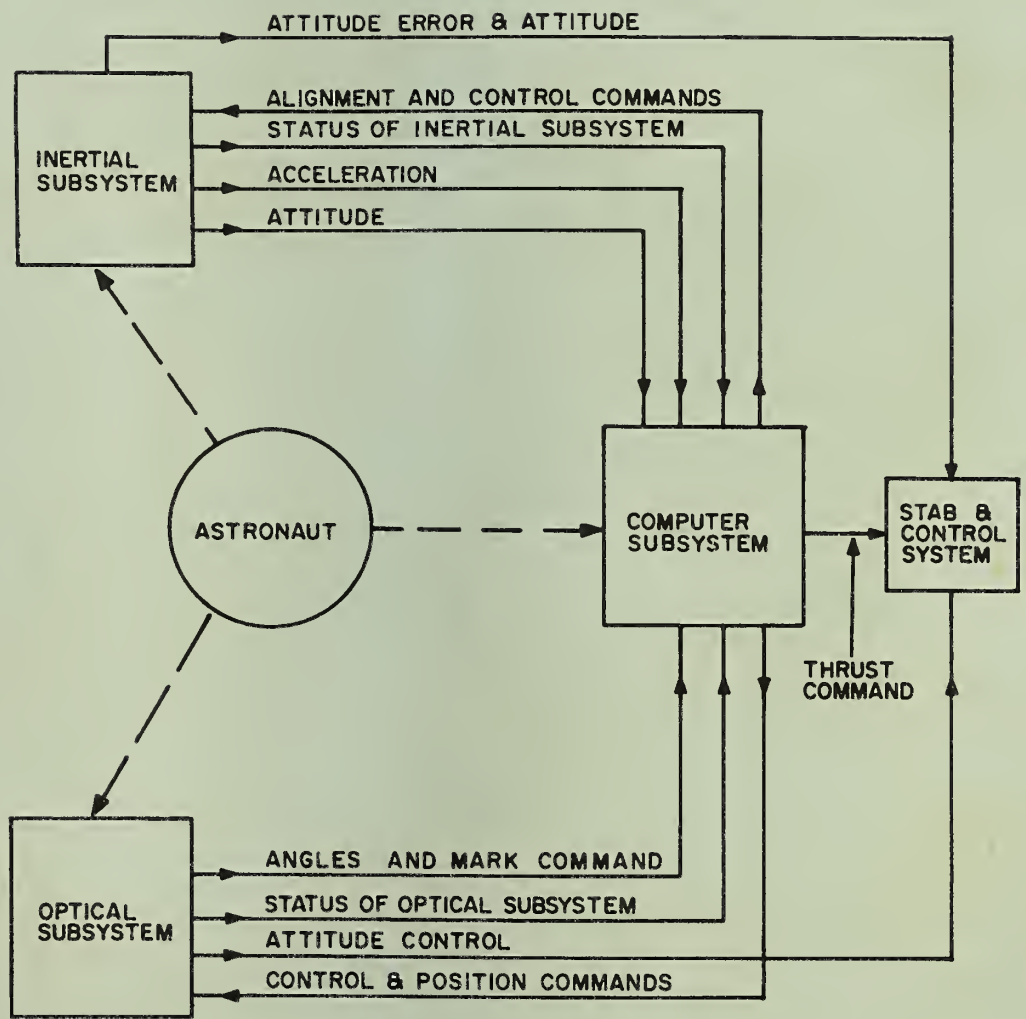


Figure 1-5. Guidance and Navigation Subsystem Data Flow

The modes of operation of the inertial subsystem can be initiated manually by the astronaut, automatically by the AGC or by astronaut selection of computer program through the computer keyboard. The status or mode of operation is displayed on the display and control panels and supplied to the computer.

1.3.3 OPTICAL SUBSYSTEM. The optical subsystem consists of the optical assembly mounted on the navigation base, two CDU's and portions of the PSA and display and control panel.

The optical subsystem is used to determine the position and orientation of the spacecraft in space. This is accomplished through the use of a catalog of stars stored in the AGC and schedule of measurements is determined before launch and is base on an optimum plan.

The optical subsystem performs two major functions: (1) provides the AGC with data obtained by measuring angles between lines of sight to celestial objects, and (2) provides measurements for establishing the inertial reference.

The optical subsystem contains a sextant and telescope. The sextant is a high magnification and dual line-of-sight device used for precision angular measurements. The telescope has a wide field of view, one line-of-sight and is used for coarse acquisition of stars and landmarks and orbital tracking of landmarks.

The optical instruments are located side by side on the navigation base. The astronaut makes observations by sighting through one of two eyepieces located on the display and control panel. The modes of operation of the optical subsystem are indicated on the display and control panel and are supplied to the AGC. A manual control stick on the front of the display and control panel is used by the astronaut to position the optical lines-of-sight. Since the optical instrument's field of view is limited, controls are also provided by which the astronaut can maneuver the entire spacecraft to point the optical instrument in any desired direction. The astronaut initiates a timing mark which causes the AGC to record both optical angles and the time at the instant the sextant is properly pointed for a measurement.

1.3.4 COMPUTER SUBSYSTEM. The computer subsystem consists of the Apollo guidance computer and portions of the display and control panels.

The computer subsystem is used to perform space flight data handling and computations. The AGC is a general purpose digital computer employing a core memory, parallel operations and a built-in self-check capability.

Programs are stored in the AGC and selected to control and solve flight equations. The selection of programs can be controlled by automatic sequencing or manually by the astronaut.

The computer subsystem performs five major functions: (1) calculates steering signals and engine discretes necessary to keep the spacecraft on the required trajectory, (2) positions the stable member in the IMU to acoordinate system defined by precise optical measurements, (3) positions the optical unit to celestial objects, (4) conducts limited malfunction isolation of the G&N system by monitoring the level and rate of system signals and (5) supplies pertinent spacecraft condition information to the display and control panel.

Using information from navigation fixes, the AGC computes deviations from the required trajectory and calculates the necessary corrective attitude and thrust commands. The velocity corrections are controlled by the computer subsystem by processing incremental velocity from the inertial subsystem. Velocity corrections are not made continuously, but rather are initiated at predetermined check points in the flight. The technique of check point velocity corrections reduces fuel consumption, since the engines are used only when a significant correction in velocity is required. The AGC also uses information from celestial measurements to align the stable member in the IMU to a defined coordinate system.

Malfunctions in the G&N system are detected by the AGC by monitoring critical signals and rates. Lamps on the display and control panel light to indicate malfunctions.

Lamps on the display and control panel indicate the program being solved by the AGC or the results of calculations. Selection of a computer program or insertion of data into the AGC can be done by the astronaut with a keyboard on the display and control panel or by uplink data through the communication and instrumentation system from the ground station.

1.4 G&N SYSTEM FUNCTIONS AND RELATION TO MISSION PHASES

There are nine major G&N system functions associated with the Apollo lunar orbit mission phases: (1) prelaunch IMU alignment, (2) guidance monitor, (3) orbital navigation, (4) inflight IMU alignment, (5) injection, (6) midcourse navigation, (7) midcourse correction, (8) entry and (9) attitude control. These nine functions are used during the ten mission phases described in figure 1-6. Table 1-1 tabulates the G&N system functions during each mission phase. The following is a brief description of each function,

1.4.1 PRELAUNCH IMU ALIGNMENT.

During prelaunch alignment, the IMU stable member is vertically erected and aligned in azimuth. The stable member is then held to this earth reference through a gyro compassing routine in the computer. Initial azimuth is determined by sighting on a ground target with the optics prior to closeout of the command module. (See figure 1-7.)

1.4.2 GUIDANCE MONITOR.

The G&N system monitors the SIV-B guidance during earth ascent and translunar injection. At launch, the IMU is switched from an earth reference (gyro compassing) to a space reference frame (inertially stabilized). The astronaut then uses the G&N system to monitor the spacecraft flight profile.

1.4.3 ORBITAL NAVIGATION.

During earth and lunar orbit, the astronaut checks the orbital trajectory and the alignment of the IMU by means of optical sightings. The astronaut takes sightings by identifying and tracking landmarks with the optical instrument. The computer records optical and IMU gimbal angles and calculates the orbital trajectory. (See figure 1-8.)

1.4.4 INFLIGHT IMU ALIGNMENT.

IMU alignment will be performed during the following mission phases: (1) earth orbit, (2) translunar coast, (3) lunar orbit, and (4) transearth coast. IMU alignment in flight is accomplished by means of optical sightings. The astronaut takes star sightings and the computer records the optical and IMU gimbal angles. The computer then calculates and applies torquing commands necessary to align the IMU. (See figure 1-9.)

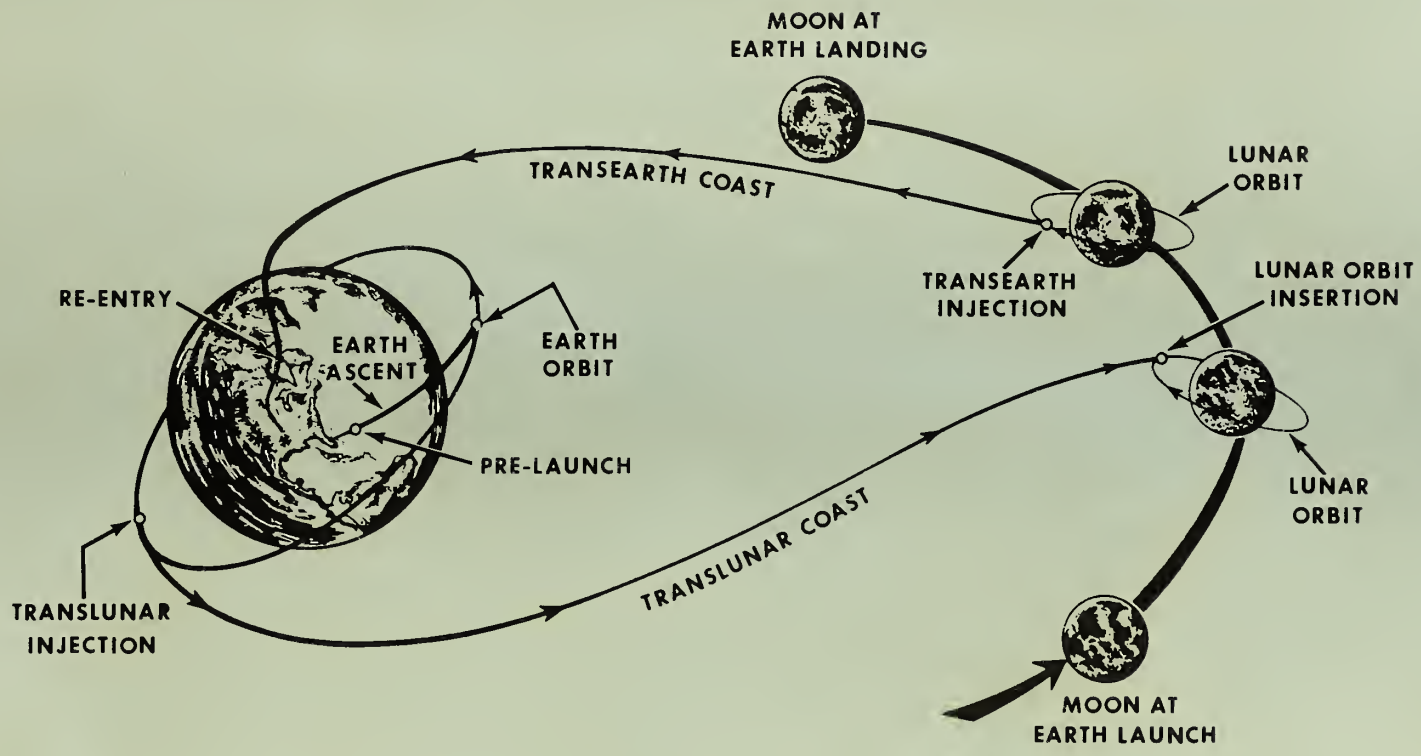


Figure 1-6. Mission Phases Required for a Lunar Orbit

LUNAR ORBIT MISSION PHASES	PRELAUNCH IMU ALIGNMENT	GUIDANCE MONITOR	ORBITAL DETERMINATION	INFLIGHT IMU ALIGNMENT	INJECTION	MIDCOURSE NAVIGATION	MIDCOURSE CORRECTION	ENTRY	ATTITUDE CONTROL
PRELAUNCH	X								
EARTH ASCENT		X							
EARTH ORBIT			X	X					
TRANSLUNAR INJECTION		X							
TRANSLUNAR COAST				X		X	X		X
LUNAR ORBIT INSERTION					X				
LUNAR ORBIT			X	X					
TRANSEARTH INJECTION					X				
TRANSEARTH COAST				X		X	X		X
ENTRY								X	

Table 1-1. G & N System Functions per Mission Phase

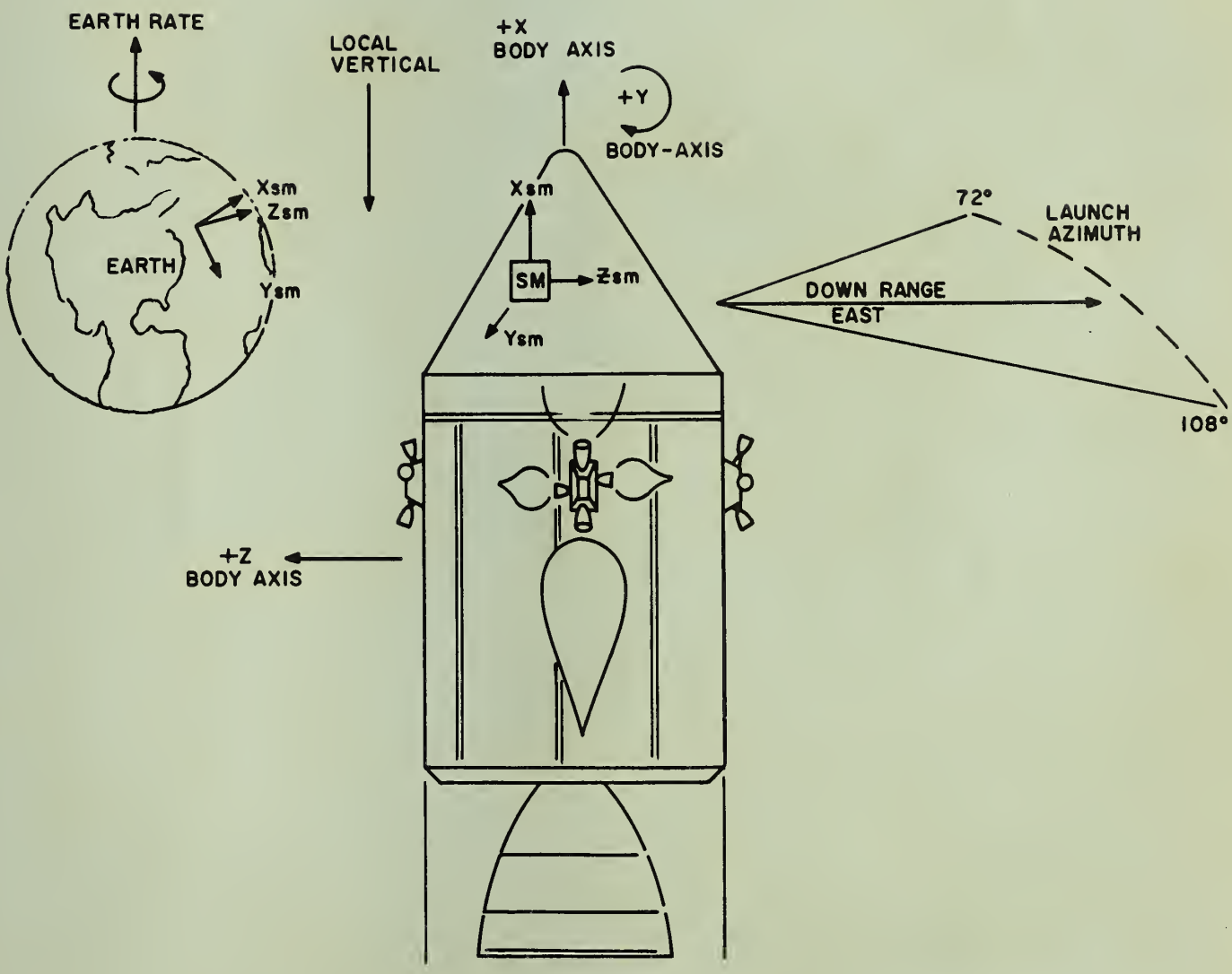


Figure 1-7. Prelaunch Alignment

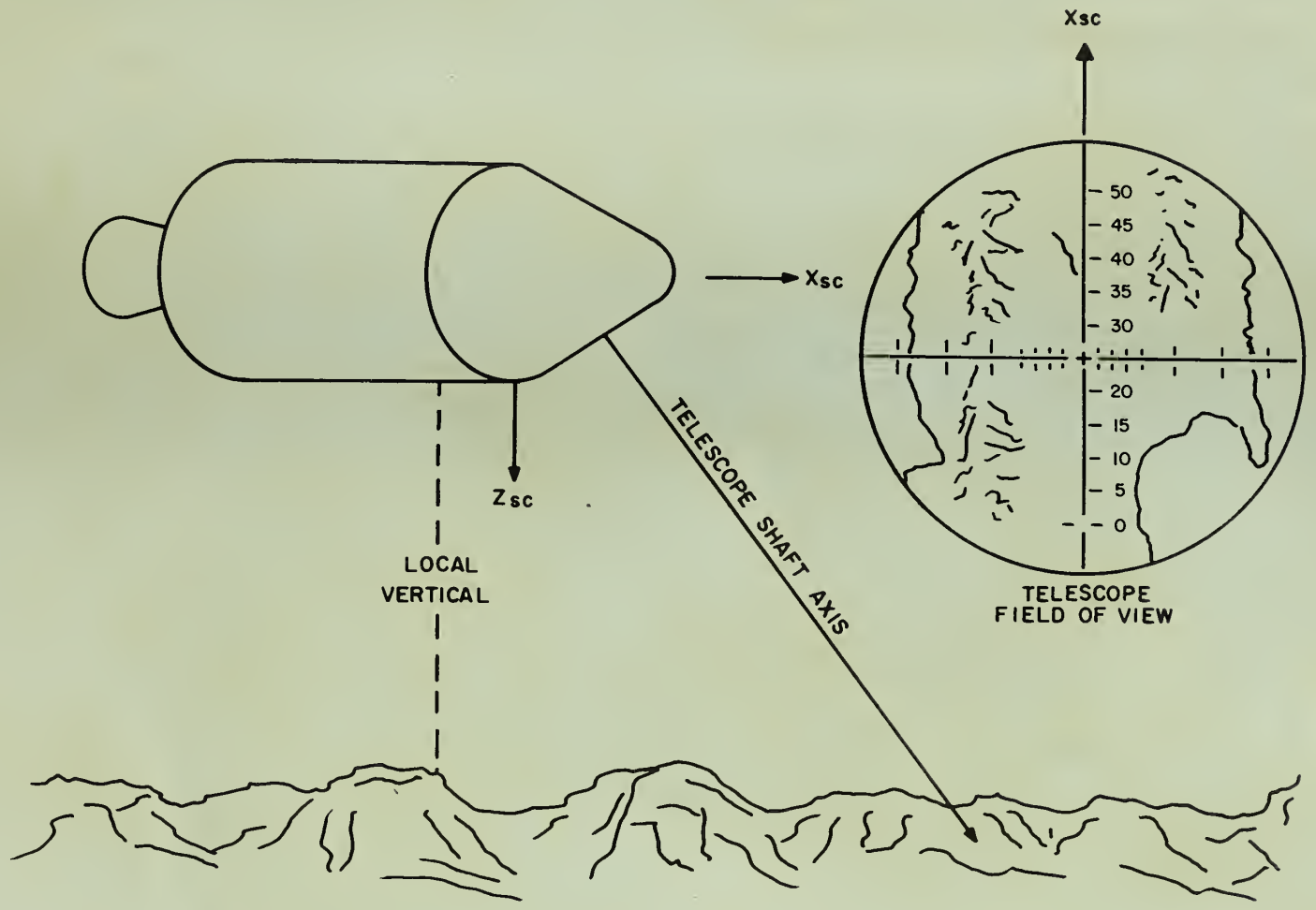


Figure 1-8. Orbital Navigation Sighting

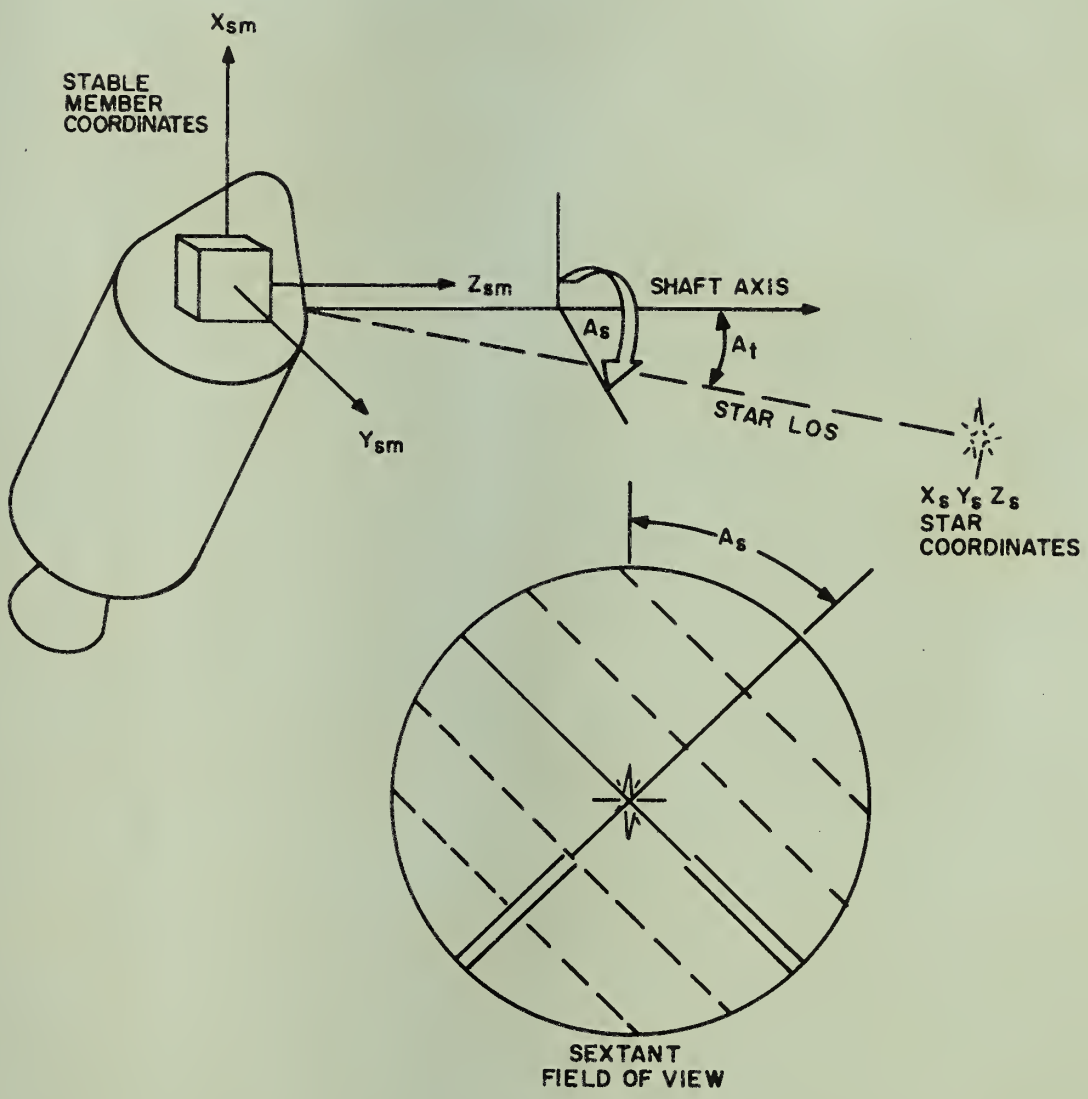


Figure 1-9. IMU Alignment Measurement

1.4.5 INJECTION. This function is performed at lunar orbit insertion and transearth injection. The G&N system places the spacecraft into the proper orientation (spacecraft X axis along the calculated thrust vector) and controls and monitors the thrusting of the spacecraft.

(NOTE: The SIV-B guidance system is primary control for translunar injection.)

1.4.6 MIDCOURSE NAVIGATION. This G&N function is performed many times during the translunar and transearth mission phases. Midcourse navigation is accomplished by taking star-landmark optical sightings. The computer records the optical angles and the time of sighting. Spacecraft position and velocity can then be updated by the computer. (See figures 1-10 and 1-11.)

1.4.7 MIDCOURSE CORRECTION. Approximately three midcourse corrections are performed during the translunar and transearth coast phases of the mission. The computer, after calculating the spacecraft position and velocity from a midcourse navigation sighting, determines the need for a midcourse correction. This is done by comparing the actual trajectory to the required trajectory. If a midcourse correction is necessary, the computer calculates the thrust vector and the velocity change needed, repositions the spacecraft and controls the thrusting of the SPS.

1.4.8 ENTRY. This G&N function is performed during entry into the atmosphere. The G&N system controls the flight path of the command module. The computer determines the proper trajectory and steers the command module along this trajectory. Steering is accomplished by rolling the command module about the navigation base X axis. This changes the lift to drag ratio of the command module, and thereby varies the trajectory.

1.4.9 ATTITUDE CONTROL. This G&N function is used during the translunar and transearth coast phases when the ISS is activiated. The ISS then provides the inertial reference to maintain the spacecraft attitude.

1.5 SUMMARY

The G&N system performs two basic functions: optical navigation and inertial guidance. Optical navigation is accomplished by using a scanning telescope and a sextant. The scanning telescope is used to acquire the celestial object and the sextant is used to accurately measure the angles to these objects. The angles are inserted into a computer which performs the calculations necessary for space navigation.

Inertial guidance is accomplished by the use of an inertially stabilized platform. Three stabilization gyros mounted on the platform and a three degree of freedom gimbaling system provide the inertial stabilization. Three accelerometers, also mounted on the platform, provide the computer with changes in velocity. These changes in velocity are accumulated in the computer. The computer, using these velocity changes, time and certain constants, then calculates the spacecraft position in space. The stable platform of the inertial measurement unit is also used for an inertial reference in space. From this reference, spacecraft attitude can be controlled.

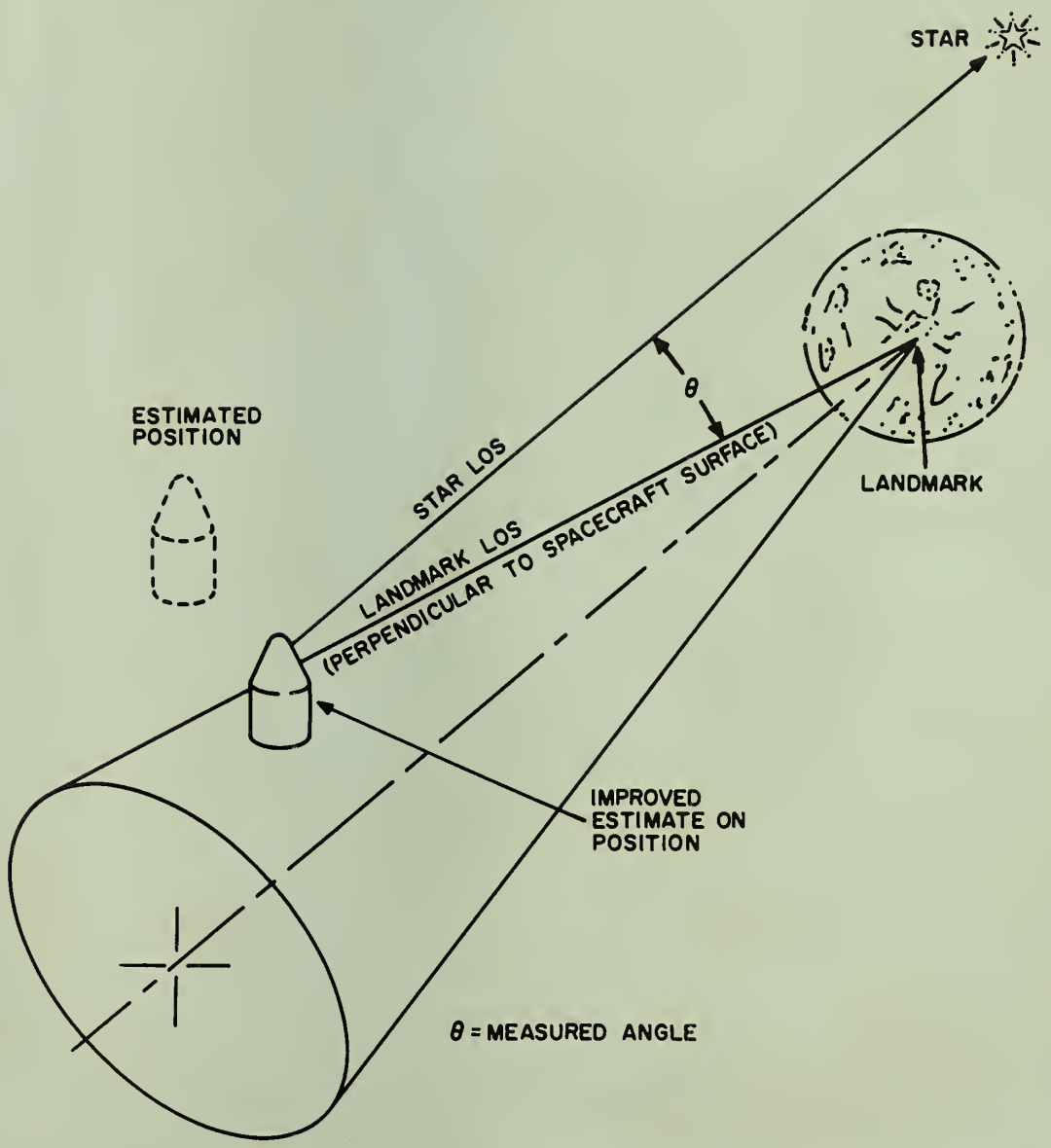


Figure 1-10. Midcourse Position Determination

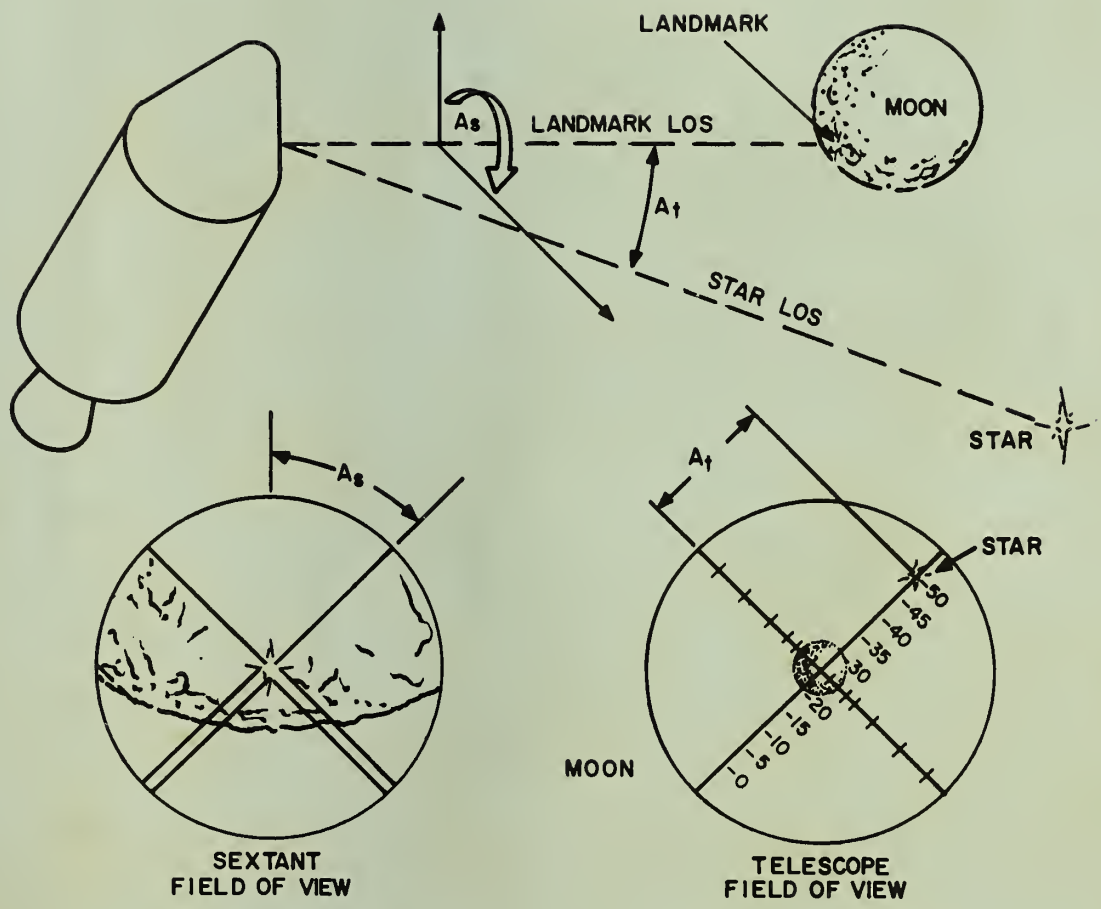


Figure 1-11. Midcourse Navigational Measurement

The G&N system interfaces with the astronaut and six basic spacecraft systems: the Electrical Power System (EPS), the Environmental Control System (ECS), the Communications and Instrumentation System (C&IS), the Stabilization Control System (SCS), the Reaction Control System (RCS) and the Service Propulsion System (SPS). The G&N system provides steering and thrusting commands to the SCS which, in turn, routes these commands to the RCS for attitude control and to the SPS for thrust and steering control. The G&N system also provides system information to the C&IS for transmission to the ground stations.

The astronaut:

a. Loads data into the computer.

b. Monitors the systems operation.

c. Can control the mode selection of the system.

d. Provides system backup.

e. Takes optical sightings.

The G&N system consists of seven major components. These components are listed below:

a. Navigation Base (NB)

b. Inertial Measurement Unit (IMU)

c. Optical Unit

d. Coupling Display Units (CDU's)

e. Power and Servo Assembly (PSA)

f. Display and Control Panels

g. Apollo Guidance Computer (AGC)

The G&N system equipment is divided into three subsystems: inertial subsystem (ISS), optical subsystem (OSS) and computer subsystem (CSS).

The G&N system is required to perform nine functions during a lunar orbit mission. These functions and their relationship with the Apollo mission phases for a lunar orbit mission are listed below:

a. Prelaunch IMU alignment - performed prior to final countdown.

b. Guidance monitor - performed during launch and translunar injection.

c. Orbital determination - performed during earth and lunar orbit.

d. Inflight IMU alignment - performed during earth orbit, translunar coast, lunar orbit and transearth coast.

e. Injection - performed during lunar orbit injection and transearth injection.

f. Midcourse navigation - performed during translunar and transearth coast.

g. Midcourse correction - performed during translunar and transearth coast.

h. Entry - performed during earth entry.

i. Attitude control - performed during translunar and transearth coast when the ISS is activated.

REVIEW QUESTIONS FOR SECTION I

1. The G&N system performs two basic functions: optical navigation and inertial guidance. Briefly explain how these functions are accomplished.

   a.

   b.

2. The G&N system interfaces with six major spacecraft systems: EPS, ECS, SCS, RCS, SPS and C&IS. Briefly explain the purpose of each system as related to the G&N system.

   a. EPS

   b. ECS

   c. SCS

   d. RCS

   e. SPS

   f. C&IS

3. The G&N system consists of seven major components. List these components.

   a.

   b.

c.

d.

e.

f.

g.

4. The G&N system is divided into three subsystems. List the subsystems.

a.

b.

c.

SECTION II

INTRODUCTION TO THE INERTIAL SUBSYSTEM

INTRODUCTION

This section describes the inertial subsystem hardware, classifies the inertial subystem into functional blocks and describes the functional blocks.

2.1 ISS PURPOSE

The inertial subsystem of the G&N system maintains an inertial reference and senses instantaneously any thrust applied to the spacecraft. The capacity to sense acceleration is used during major thrusting maneuvers. The functions of the inertial subsystem -- attitude control and acceleration measurement -- are performed primarily when thrust is applied to the spacecraft. The inertial subsystem is turned on and off as required during the flight. The optical subsystem is used to take sightings on celestial objects; these sightings are used in calculating spacecraft position and velocity and in aligning the inertial measurement unit (IMU) during flight.

In preparation for the Apollo mission, the optimum guidance equations are selected and the required constants are stored in the Apollo guidance computer (AGC), thus dependence on a reference trajectory is kept to a minimum.

The inertial subsystem measures acceleration along the axes of the IMU stable member coordinate system and supplies incremental velocity data to the AGC. To determine spacecraft position and velocity, the components of velocity due to gravitational field accelerations are added to the velocity acquired as a result of thrusting (acceleration measured by the accelerometer loops). Using the resultant total velocity and the last known position and velocity, the AGC calculates the present position and velocity of the spacecraft. The position and velocity data are used during spacecraft velocity correction to determine when the proper trajectory has been obtained and when thrusting can be stopped.

The inertial subsystem can be used to control spacecraft attitude. The attitude of the spacecraft, with respect to the stable member, is determined by means of resolvers which measure the gimbal angles. The difference between the actual orientation of the spacecraft with respect to the IMU stable member and the orientation commanded by the navigator or the AGC results in an attitude error signal which can be applied to the stabilization and control system (SCS).

Alignment of the stable member in flight is necessary because of gyro drift and on-off cycling of the inertial subsystem. Two star sightings are needed for coarse alignment of the IMU and two sightings for fine alignment. For coarse and fine IMU alignment, the optical instruments are sighted alternately at two stars. The AGC records the optical angles and time (when MARK COMMAND is issued) and calculates the signals required to align the IMU stable member.

2.2 ISS EQUIPMENT

The inertial subsystem consists of the following equipment (figure 2-1):

a. Navigation Base (NB)

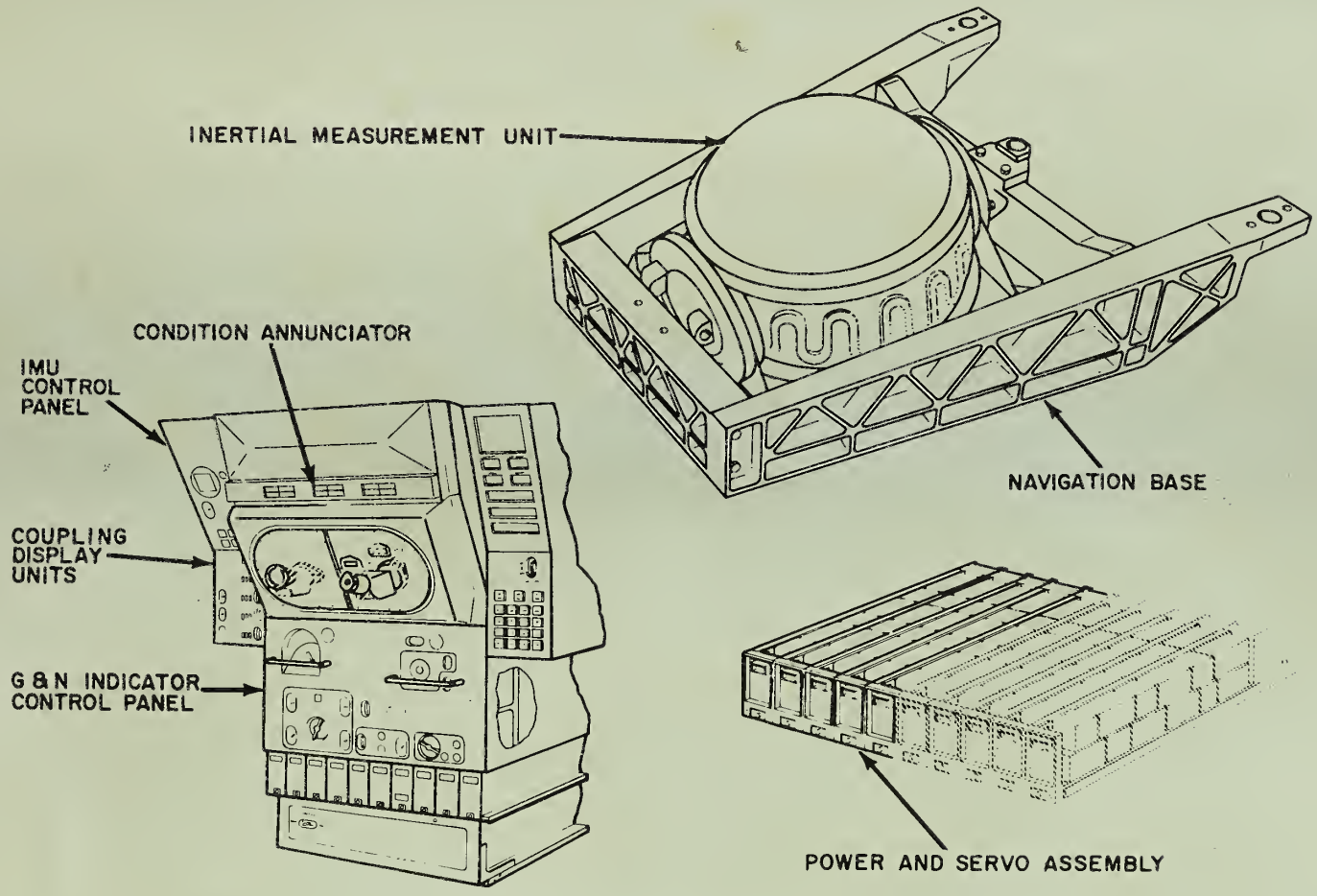


Figure 2-1. Inertial Subsystem Equipment

b. Inertial Measurement Unit (IMU)

c. Coupling Display Unit (CDU) (three required)

d. Power and Servo Assembly (PSA) (portions)

e. Display and Control Electronics

f. IMU Control Panel

g. G&N Indicator Control Panel

2.3 ISS FUNCTIONAL BLOCKS

For the purpose of explanation, the inertial subsystem equipment is divided into 15 functional blocks as shown in figure 2-2. The functional blocks are described briefly to show their interrelationship and then are described in detail in sections III through VIII of this study guide.

2.3.1 NAVIGATION BASE. The navigation base provides a rigid support for the IMU and optical assembly in the spacecraft. The IMU and optical assembly are precisely aligned on the navigation base.

2.3.2 INERTIAL MEASUREMENT UNIT STRUCTURE. The IMU structure consists of the stable member, gimbaled for three degrees of freedom, with respect to the navigation base. The three gimbals allow the stable member to remain nonrotating in space.

The orientation of the stable member, with respect to the navigation base, is measured by resolvers on the gimbal shafts. The resolver gimbal angle output signals are supplied to the CDU's by mode switching. The CDU's can repeat the IMU gimbal angles, which can then be supplied to the AGC by encoders in the CDU's.

Nine inertial components are located in the IMU: three (3) 25 inertial reference integrating gyros (25 IRIG's) and three (3) angular differentiating accelerometers (ADA's) are used in the stabilization loop to sense changes in the orientation of the stable member; and three (3) 16 pulsed integrating pendulums (16 PIP's) are used in the accelerometer loops to sense changes in velocity of the spacecraft.

The temperature of these inertial components is critical and is controlled by the temperature control circuit. The middle and outer gimbals and gimbal case are spherical in shape. The gimbal case contains integral coolant passages and provides hermetic sealing of the unit. A spotlight and windows in the G&N indicator control panel are used for inspection of the IMU for possible coolant leaks.

2.3.3 TEMPERATURE CONTROL AND INDICATOR CIRCUITS. The temperature of the inertial components is held within specified limits by heating elements and temperature control sensors. The circuit has four modes of operation: proportional, auto-override, emergency and backup. The switching between modes and the testing of the circuit calibration is accomplished by controls located on the G&N indicator control panel. To assist in temperature regulation, two blowers, located between the outer gimbal and gimbal case, circulate air through the outer gimbal to pass heat from the middle gimbal to the cooled outer gimbal case. In case of a failure in the temperature control circuit, the temperature no-go lamps on the lower display and control panel light.

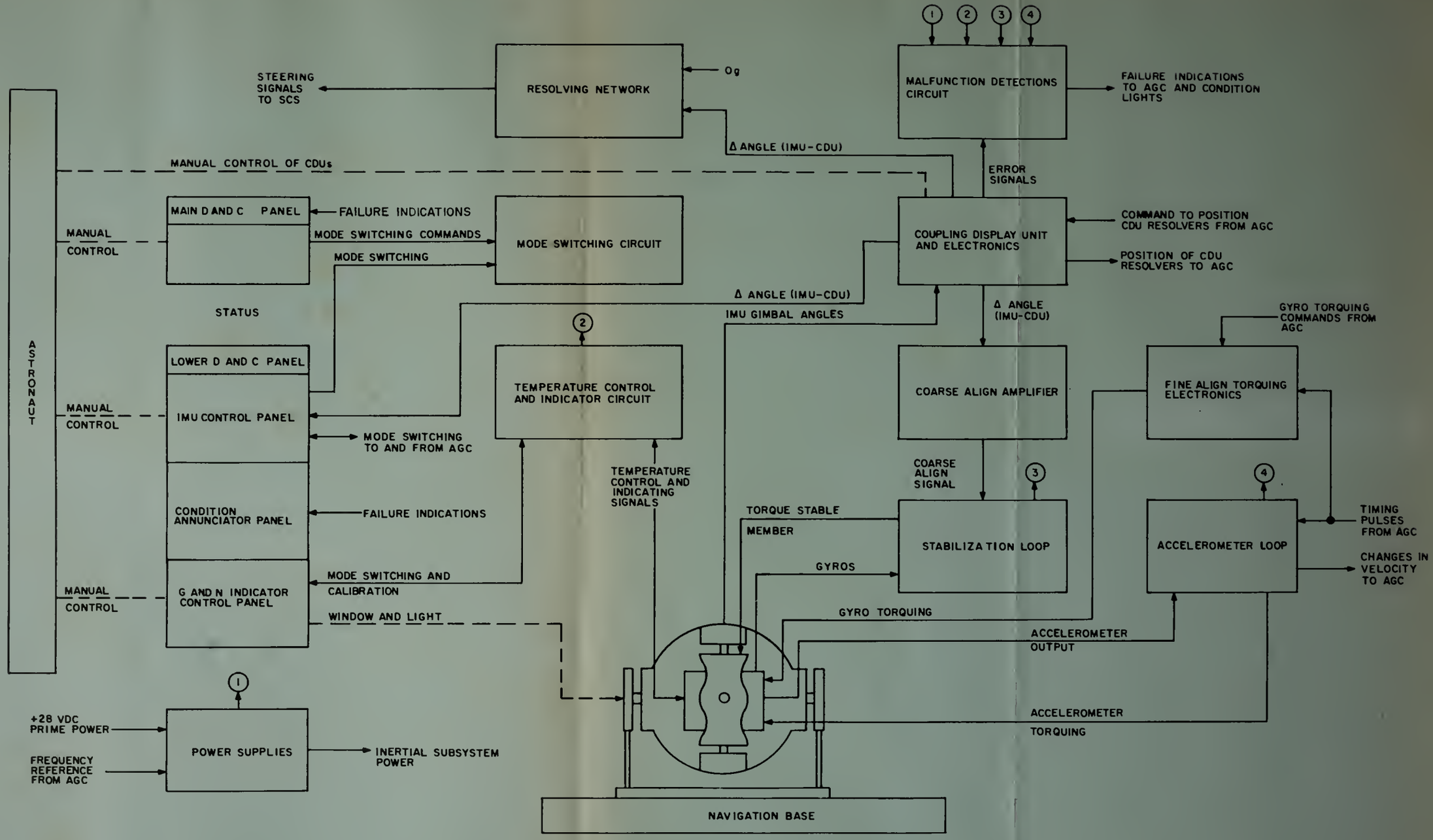


Figure 2-2. Inertial Subsystem Interface

2.3.4 STABILIZATION LOOP. The stabilization loop holds the stable member inertial space referenced to a given coordinate system by isolating the stable member from roll, pitch and yaw motions of the spacecraft. The stable member serves two purposes in the system: (1) acts as a reference for measuring the attitude of the spacecraft and (2) holds the three accelerometers (used in space for measuring acceleration due to thrust) in a fixed coordinate system.

When the stabilization loop holds the stable member inertial referenced, the 25 IRIG's on the stable member and ADA's on the stable member and middle gimbal generate error signals to indicate any change in the orientation of the stable member with respect to inertial space. The error signals are amplified by the servo amplifiers in the PSA and are supplied to the IMU gimbal torque motors, which reposition the stable member.

When the stabilization loop is energized, the stable member is referenced to the spacecraft by the coarse align loops. The stable member must then be aligned to the desired orientation. The alignment is done in two steps, coarse align and fine align. The coarse align is done first and is accomplished by injecting coarse align coarse align signals into the stabilization loop servo amplifiers. The fine align is accomplished by injecting a fine align signal from the AGC into the torque ducosyn of each of the 25 IRIG's. During prelaunch, the stable member is held earth-referenced by supplying the 25 IRIG's with the appropriate torquing signals.

2.3.5 COARSE ALIGN AMPLIFIERS. The coarse align amplifiers are used to amplify and demodulate signals which represent the IMU gimbal angles commanded by the CDU's. During coarse alignment, the IMU is slaved to the CDU's so the alignment is completed when the Δ angle (IMU-CDU) equals 0 ± 1.5 degrees. The outputs of the coarse align amplifiers are supplied to the servo amplifiers in the stabilization loops which, in turn, coarsely align the IMU stable member.

2.3.6 FINE ALIGN TORQUING ELECTRONICS. The fine align torquing electronics is used for fine alignment of the stable member. The electronics contain current switches which are turned off and on by torquing commands and timing pulses from the AGC. Using data obtained from optical sightings, the AGC determines the number of command pulses required. The outputs of the current switches are in digital form and are supplied to the torque ducosyns of the 25 IRIG's.

2.3.7 ACCELEROMETER LOOPS. The accelerometer loops sense changes in acceleration due to thrust or drag forces applied to the spacecraft and provide change in velocity information to the AGC. The loops consist of three mutually perpendicular 16 PIP's on the stable member and associated electronics in the PSA. As acceleration is applied along the input axes of the 16 PIP's, signals are generated and used by the accelerometer loop electronics to generate digital feedback signals which act to restrain the 16 PIP pendulums. Incremental velocity, in the form of pulses, is supplied to the AGC and used in calculating velocity and position data. Timing pulses are supplied from the AGC to the accelerometer loop electronics which are used in the development of torquing signals for the accelerometer.

2.3.8 COUPLING DISPLAY UNITS AND ELECTRONICS. The CDU's couple the IMU to the AGC and generate steering and alignment signals. The inertial subsystem contains three CDU's, one for each IMU gimbal. Each CDU contains resolvers, which are positioned either manually by the astronaut or automatically by the AGC. One of the major signals generated by the CDU's is the Δ angle (IMU-CDU) signal which is proportional to the angular difference between the IMU gimbal and CDU resolver positions. This signal can be used to control the position of the IMU or the CDU's to display spacecraft attitude error or to develop attitude error signals for steering during thrusting maneuvers or for spacecraft attitude control. Relays are used to make the CDU connections necessary for operation in the different inertial subsystem modes. The CDU inputs and their functions are as follows:

a. IMU gimbal angle signals: indicate the angles of the inner, middle and outer gimbals.

b. Digital signals from the AGC: position the inner, middle and outer CDU resolvers.

c. Mode control signals: operate the relays in the CDU electronics so that different modes of operation can be entered.

d. CDU manual control: allows the CDU resolvers to be positioned manually during the manual CDU mode.

The CDU outputs and their functions are as follows:

a. Digital signals to the AGC: indicate changes in position of the CDU resolvers.

b. Δ angle (IMU-CDU) signal: represents the difference between the IMU gimbal angles and the CDU resolver angles. This signal is supplied to the resolver network for attitude control, to the flight director's attitude indicator, to the IMU control panel for display and to the coarse align amplifer for IMU torquing.

2.3.9 RESOLVING NETWORK. The resolving network transforms the Δ angle (IMU-CDU) signal into navigation base and spacecraft axes and supplies the resultant signals to the stabilization and control system. A resolver mounted on the outer gimbal axis and a fixed resolver are used in the resolver network.

2.3.10 LOWER DISPLAY AND CONTROL PANEL. The inertial subsystem display and control panels and their functions are as follows:

a. The IMU control panel: controls and indicates the mode in which the inertial subsystem is operating and displays the Δ angle (IMU-CDU) signals on a meter.

b. The G&N indicator control panel: indicates IMU temperature control system mode of operation, provides a means of testing the temperature control circuits and contains windows for visual inspection of the IMU.

c. The condition annunciator consists of condition lights which provide the navigator with subsystem status and detected subsystem errors.

2.3.11 MAIN DISPLAY AND CONTROL PANEL. Status of the inertial subsystem is supplied to the main display and control panel from the lower display and control panel so that the astronaut can observe the subsystem conditions while reclining in his couch. Mode and power switching of the inertial subsystem is also implemented from the main display and control panel.

2.3.12 POWER SUPPLIES. The following power supplies, packaged in the PSA, are required to operate the inertial subsystem:

a. Pulse torque dc supply.

b. 800 cps IMU and CDU supply.

c. 3.2 kc ducosyn supply.

d. 3.2 kc temperature control reference.

e. -28 vdc supply.

f. 25.6 kc encoder excitation supply.

The power supplies operate on 28 volt dc prime power and are synchronized by pulses from the AGC. Local oscillators in the power supplies allow them to operate independent of the AGC. The outputs of the power supplies are monitored by the malfunction detection circuits.

2.3.13 MALFUNCTION DETECTION CIRCUITS. The malfunction detection circuits monitor the power supplies, temperature control and indicator circuits, stabilization loop electronics, accelerometer loop electronics and CDU electronics. When a malfunction occurs, the malfunction detection circuits produce a failure signal which is sent to the condition indicators on the master caution panel of the main display and control, the condition annunciator on the lower display and control panel and to the AGC.

2.3.14 MODE SWITCHING CIRCUIT. The mode switching circuit contains the relays and logic circuits used to make the connections required in the selection of the different inertial subsystem modes.

2.4 SUMMARY

The ISS maintains an inertial reference from which spacecraft attitude and velocity changes are measured. The ISS has the capability of controlling spacecraft attitude and velocity changes. The ISS consists of:

a. Navigation Base (NB)

b. Inertial Measurement Unit (IMU)

c. Coupling Display Units (CDU's) (three)

d. Power and Servo Assembly (PSA)

e. Lower Display and Control Electronics

f. IMU Control Panel

g. G&N Indicator Control Panel

The IMU consists of a stable member with three degrees of freedom. Mounted on the IMU stable member are: three stabilization gyros (25 IRIG's), three accelerometers (16 PIP's), one ADA and certain critical preamplifiers. Three coupling display units monitor the IMU gimbal angles and provide the angles to the AGC and the astronaut. The power and servo assembly (PSA) contains the support electronics for the ISS.

REVIEW QUESTIONS FOR SECTION II

1. What are the two basic functions of the ISS?

2. The IMU gimbal angles are transferred to the AGC through what major component?

3. What is the function of the coarse align electronics?

SECTION III

DESCRIPTION AND MECHANIZATION OF THE INERTIAL MEASUREMENT UNIT

INTRODUCTION

This section describes the construction and components of the Inertial Measurement Unit. It describes the purposes of the various components and briefly discusses the circuits and loops contained within the IMU.

3.1 IMU GIMBAL ASSEMBLIES

The Inertial Measurement Unit (IMU) is a gimballed, three-degree-of-freedom gyroscopically stabilized device whose primary functions are:

a. To maintain an orthogonal, inertially referenced coordinate system for spacecraft attitude control and measurement, and . . . . . .

b. To maintain three accelerometers in this coordinate system for accurate measurement of spacecraft velocity changes.

The IMU consists of three gimbals, of which the inner gimbal is the Stable Member (SM), gimbal mounted electronic packages, and six inter-gimbal assemblies. These are contained within the gimbal case or support structure.

3.1.1 STABLE MEMBER. The stable member or inner gimbal is supported by the middle gimbal and is free to rotate 360 degrees about the inner gimbal axis. The stable member (figure 3-1) is machined from a solid block of cold-pressed and sintered beryllium. Holes are bored in the block for mounting three 25 IRIG's (inertial reference integrating gyros), and three 16 PIP's (pulsed integrating pendulums). Another inertial instrument, an angular differentiating accelerometer (ADA) is mounted on the inner gimbal along with gimbal mounted electronics (GME) modules. These modules include three IRIG preamplifiers in one module assembly, three PIP preamplifiers in three separate modules, one ADA preamplifier in a single module and three PIP suspension capacitor assemblies in three separate modules.

3.1.2 INTER-GIMBAL ASSEMBLY. An inter-gimbal assembly (figure 3-3) is attached to each end of the stable member and to the middle gimbal to connect these two units and to define the inner gimbal axis. A duplex pair of low-preload ball bearings is fixed to, or floated on a stub shaft within the inter-gimbal assembly. The inter-gimbal assemblies also house the torque motors and resolvers used for gyro error resolution and angular data transmission. The stable member power inputs and signal inputs and outputs are routed through a 40-contact slip ring assembly on each end of the inner gimbal axis as shown in figure 3-4. Angular data transmission is accomplished by a

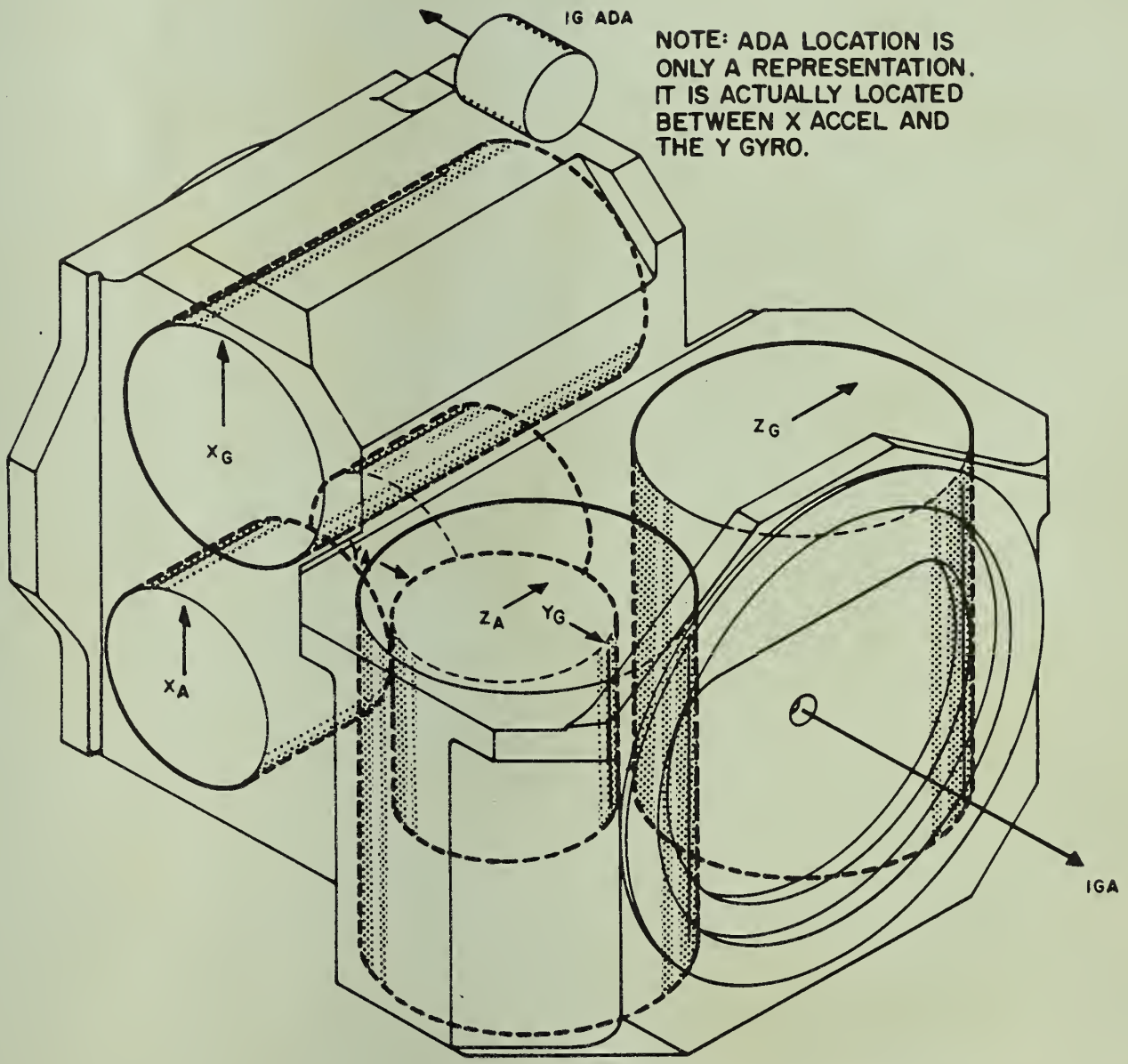


Figure 3-1. Stable Member

single speed (1X) coarse and a sixteen speed (16X) fine transmitter resolver mounted on opposite ends of the inner gimbal axis (IGA). These resolvers supply 800 cps signals (proportional to the sine and cosine of the inner gimbal angle) to the coupling display unit (CDU). A gyro error resolver is also mounted on the positive end of the inner gimbal axis and is used in the stabilization loop to transform gyro error into gimbal axis errors. The two dc torque motors are approximately six inches in diameter and utilize permanent magnet stators. These motors which are electrically in parallel are used in the stabilization loop to position the stable member.

3.1.3 MIDDLE GIMBAL. The spherical middle gimbal is assembled from two hemispherically shaped sections to allow for separation. The hemispheres are of aluminum alloy. The flanges used for assembly of the gimbal are dip brazed to the hemispheres. Prior to brazing, the hemispheres are formed to provide stiffening ribs. An inter-gimbal assembly is attached to each end of the middle gimbal and to the outer gimbal to connect the middle and outer gimbals and to define the middle gimbal axis. The inter-gimbal assemblies permit 360 degrees of freedom. Each inter-gimbal assembly contains ball bearings, a dc torque motor, a 40-contact slip ring assembly for routing electrical inputs and outputs, and a gimbal angle resolver. A 16X fine resolver is at one end and a 1X coarse resolver is used at the opposite end of the assembly. Other components mounted on the middle gimbal includes two ADA's, one for the middle gimbal and one for the outer gimbal, and two ADA preamplifiers in separate modules. A switch also is included on the middle gimbal axis to signal the astronauts when the middle gimbal angle exceeds plus or minus 60 degrees.

3.1.4 OUTER GIMBAL. The general configuration, fabrication and assembly of the outer gimbal is similar to the middle gimbal. An inter-gimbal assembly is attached to each end of the outer gimbal and defines the outer gimbal axis. The inter-gimbal assembly provides 360 degrees of freedom for the outer gimbal. Each inter-gimbal assembly contains ball bearings, a dc torque motor and a 50-contact slip ring assembly for routing electrical inputs and outputs. A 16X fine gimbal angle resolver is mounted on one assembly; a 1X coarse gimbal angle resolver and the pitch-yaw resolver are mounted on the other assembly. The pitch-yaw resolver transforms steering error signals from the gimbal CDU's to the navigation base coordinates. Other components on the outer gimbal include two axial flow blowers, which circulate air over the middle and support gimbals, and the blower speed control module. Also on the outer gimbal is a 28-volt dc regulator module for the temperature control system.

3.1.5 GIMBAL CASE. The gimbal case also is spherical and fabricated of aluminum alloy. The gimbal case consists of a center section containing integral coolant passages and provides connectors to attach the IMU to the spacecraft water-glycol coolant system as shown in figure 3-2. The mounting flanges and hardware of the center section are used to attach the IMU to the navigation base. Each end of the center section includes a cover over the inter-gimbal assembly. The covers provide a total of four electrical connections to the IMU. The support gimbal is completed by the addition of a spherical section to the top and bottom of the center section to hermetically seal the IMU. A precision resolver alignment module also is attached to the gimbal case.

3.2 AXES

The stabilization loop operation and the spacecraft error mechanization is based on nine sets of axes and four angles used in mechanizing the inertial subsystem. Each set of axes is a right-hand orthogonal coordinate system with positive rotation defined by the advancing of a right-hand screw. Figure 3-14 shows the relationship of the nine sets of axes. Figures 3-5 through 3-13 define the various sets of axes. Figures 3-15 through 3-17 define the angles.

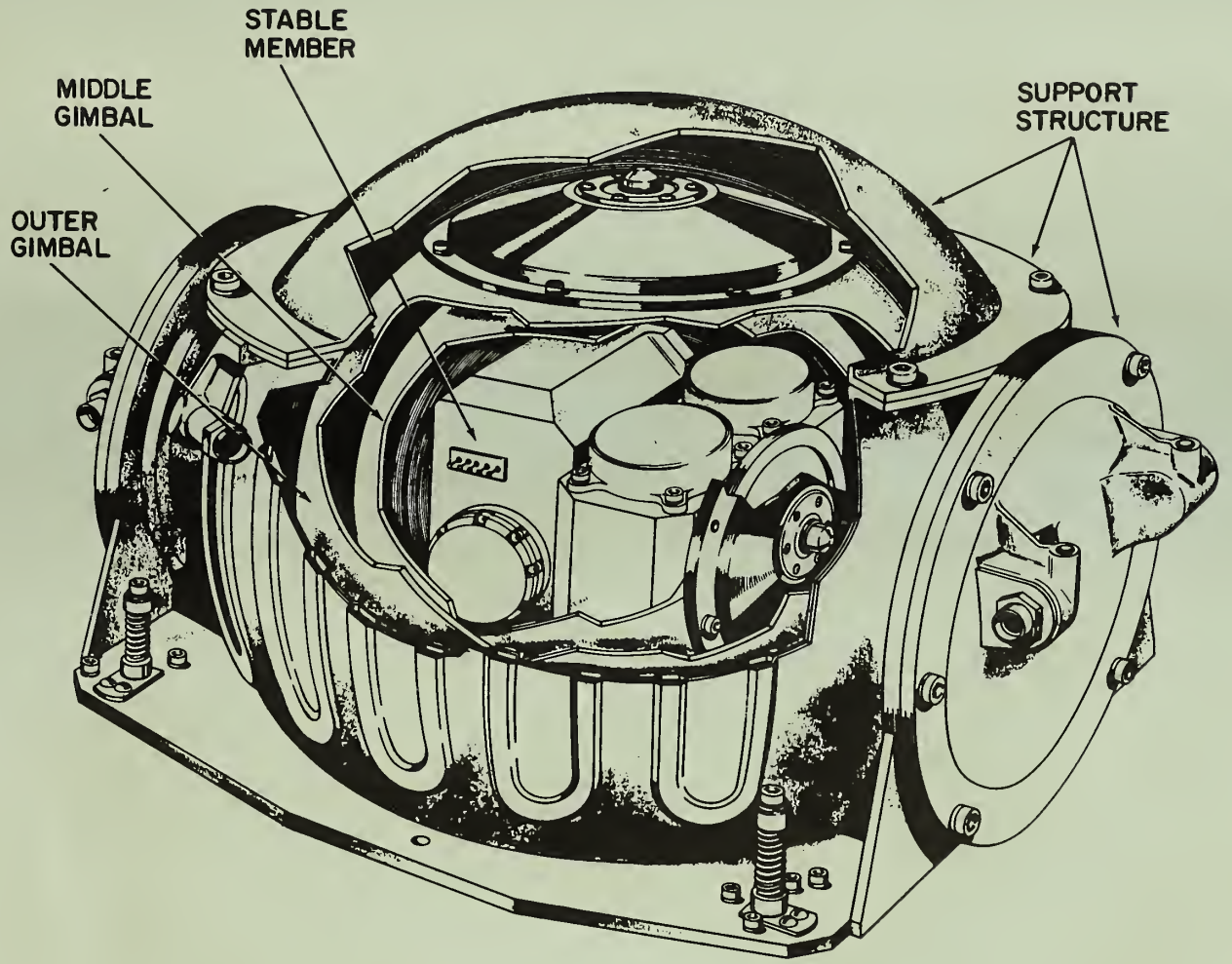


Figure 3-2. Support Structure and IMU Gimbals

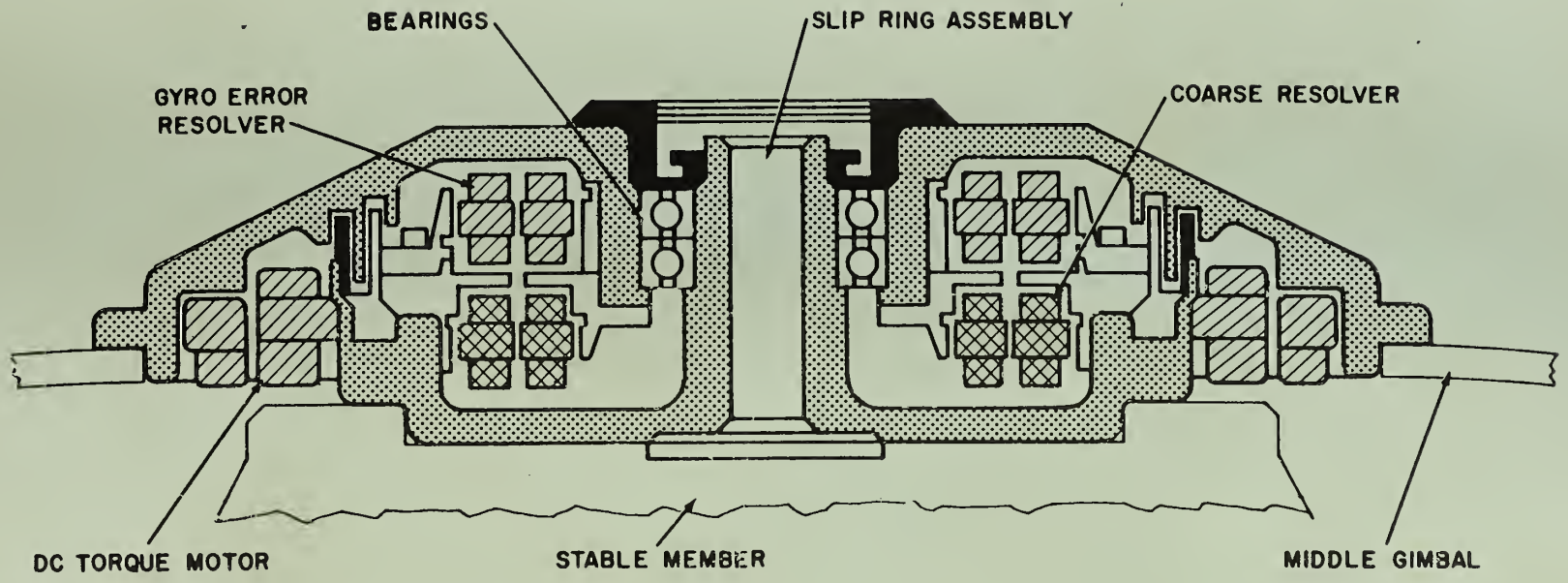


Figure 3-3. Intergimbal Assembly

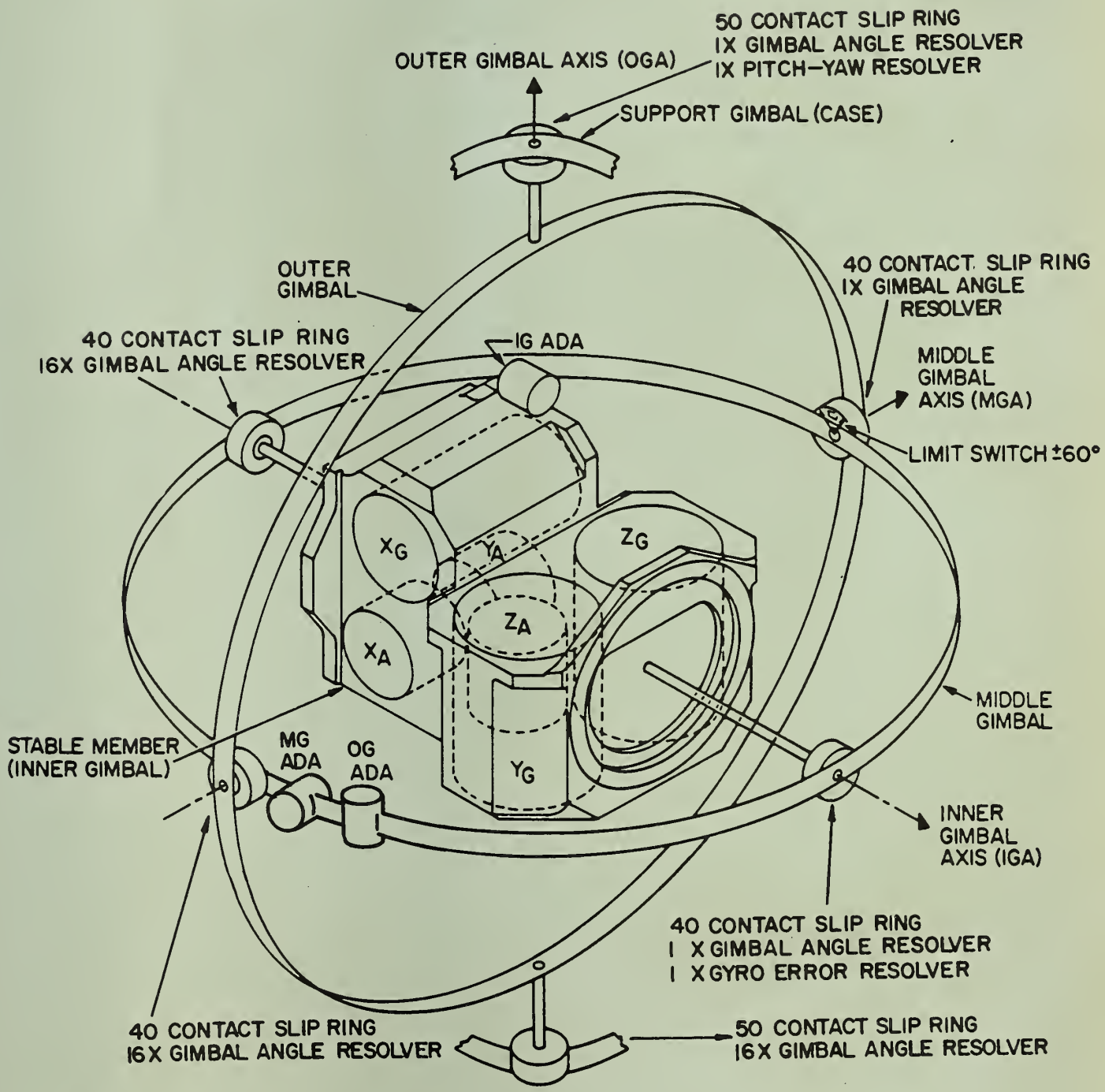
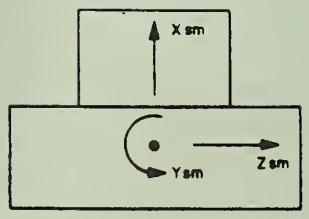
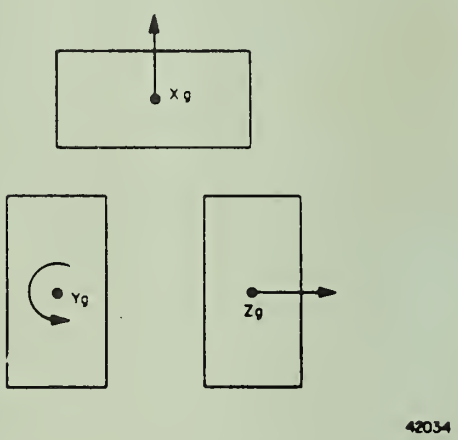


Figure 3-4. IMU Gimbal Assembly and Gimbal Axes



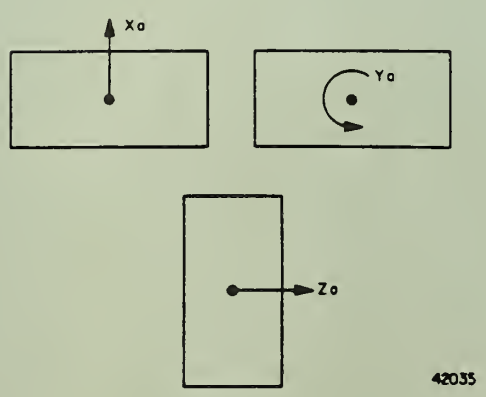
The stable member axes are aligned in a right-hand orthogonal coordinate system. They are used as a reference to align the inertial components and to define the inertial axes during flight.

Figure 3-5. Stable Member Axes



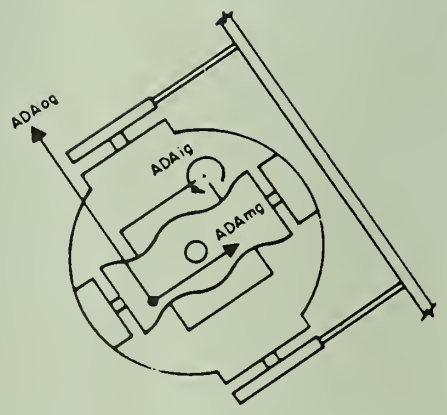
The 25 IRIG axes define the positive input axis of the gyros and are fixed parallel with respect to the stable member axes.

Figure 3-6. 25 IRIG Axes



The 16 PIP axes define the positive input axis of the accelerometer and are fixed parallel with respect to the stable member axes.

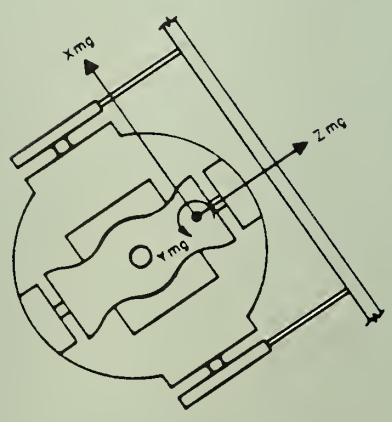
Figure 3-7. 16 PIP Axes



42036

The inner gimbal ADA axis is fixed parallel to the Y axis while the middle and outer gimbal ADA axes are fixed parallel to the Z and X middle gimbal axes, respectively.

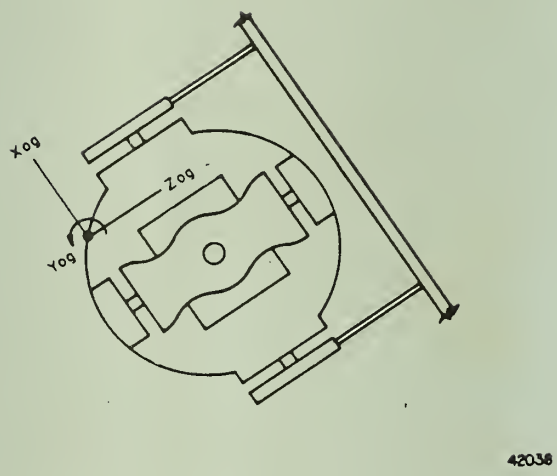
Figure 3-8. ADA Axes



42037

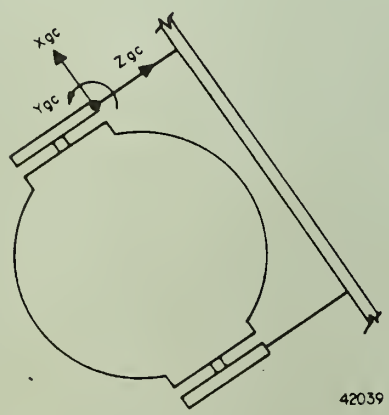
The middle gimbal axes are aligned in a right-hand orthogonal coordinate system. The axes are fixed to the movable middle gimbal. If the inner gimbal angle is set to zero, the axes are then parallel with the stable member axes. During the re-entry phase, this would be the position of inner gimbal alignment. During other phases of the mission, the stable member would be at a gimbal angle of 33 degrees from the middle gimbal X axis.

Figure 3-9. Middle Gimbal Axes



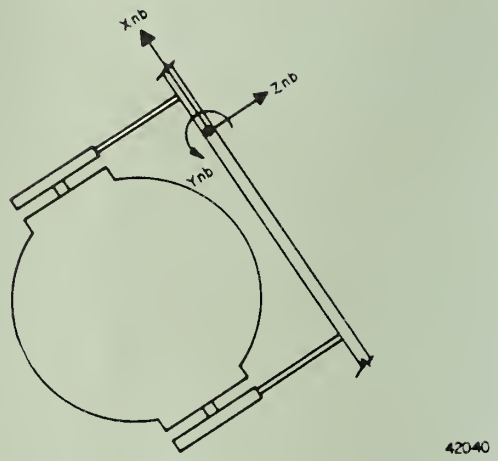
The outer gimbal axes are aligned in a right-hand orthogonal coordinate system. The axes are fixed to the movable outer gimbal. If the inner and middle gimbal angles are set to zero, the axes are then parallel with the stable member axes.

Figure 3-10. Outer Gimbal Axes



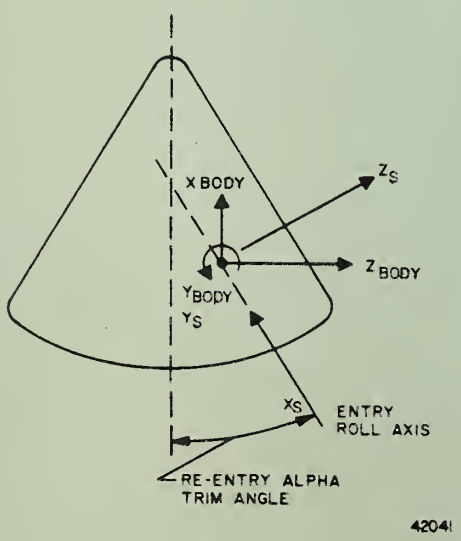
The gimbal case axes are orthogonal and fixed to the spacecraft. These axes are utilized as a reference frame when mounting the IMU to the navigation base. When all gimbal angles are set to zero, the axes are parallel with the stable member axes.

Figure 3-11. Gimbal Case Axes



The navigation base axes are orthogonal and fixed to the spacecraft. The gimbal case axes are aligned parallel with the navigation base axes during assembly. The navigation base axes are used as a reference frame for navigation.

Figure 3-12. Navigation Base Axes



The spacecraft body axes are orthogonal and fixed to the spacecraft at the center of gravity. Y body is parallel to Y_{nb}, while X body and Z body are displaced from the X_{nb} and Z_{nb} by the reentry alpha trim angle which is approximately 33 degrees. Stability axes are represented by X_S, Y_S, Z_S. Angular rotation of spacecraft:

1. Rotation about X body is roll with the angle defined as ϕ (Phi).

2. Rotation about Y body is pitch with the angle defined as θ (Theta).

3. Rotation about Z body is yaw with the angle defined as Ψ (Psi).

Figure 3-13. Spacecraft Axes

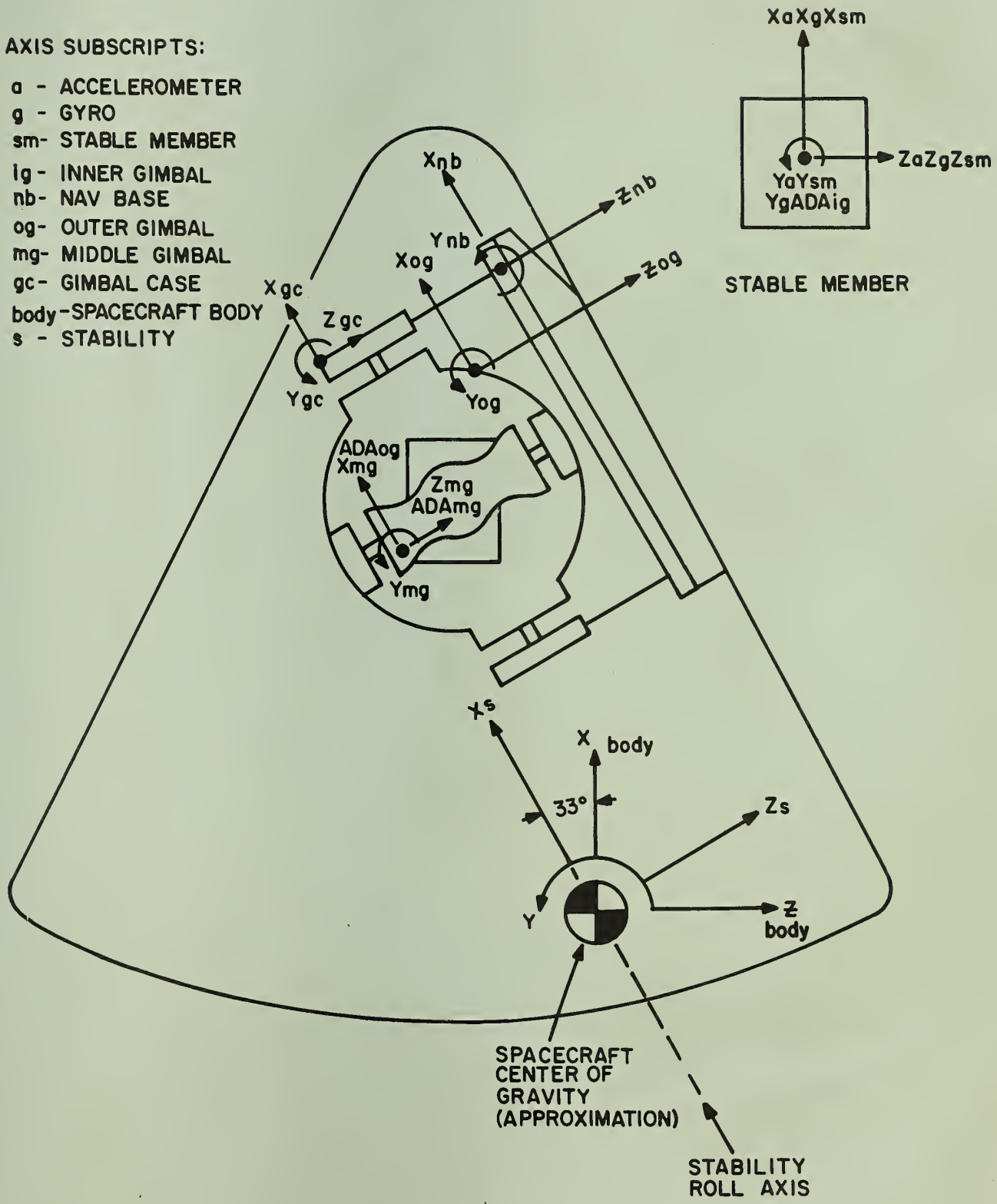
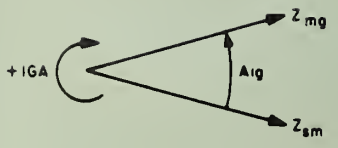
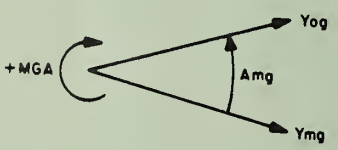


Figure 3-14. Spacecraft, IMU and Nav-Base Axes



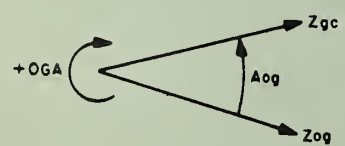
The positive inner gimbal angle is defined as the angle from the stable member Z axis to the middle gimbal Z axis as measured counterclockwise from the stable member. (As viewed from the positive Y inner gimbal axis.)

Figure 3-15. Inner Gimbal Angle



The positive middle gimbal angle is defined as the angle measured counterclockwise from the Y middle gimbal axis to the Y outer gimbal axis. (As seen from the positive Z middle gimbal axis.)

Figure 3-16. Middle Gimbal Angle



The positive outer gimbal angle is defined as the angle measured counterclockwise from the Z outer gimbal axis to the Z gimbal case axis. (As seen from the positive X outer gimbal axis.)

Figure 3-17. Outer Gimbal Angle

3.3 STABILIZATION LOOP

The purpose of three stabilization loops is to maintain the stable member and its three 16 PIP accelerometers fixed with respect to inertial space. This stable, non-rotating platform is used as the reference to maintain the orientation of the accelerometers with respect to the inertial frame of reference and is also used as an attitude reference for the spacecraft.

3.3.1 STABILIZATION LOOP OPERATION. The stabilization loop has three 25 IRIG's which sense rotational changes in the orientation of the stable member and three ADA's which sense rotational rate changes. The input axes of the 25 IRIG's and ADA's are orientated as described in figure 3-14. The gyro and the ADA error signals are generated whenever the stable member is rotated with respect to inertial space. The error signals are amplified, resolved if necessary, and supplied to the gimbal torque motors which drive the stable member back to its original position to reduce the error to zero. The path of the error signal originating at the gyros and terminating at the torque motors is shown in figure 3-18.

The 25 IRIG output is a 3,200 cps error signal which is proportional to the rotation of the gyro about its input axis. The ADA produces a dc output in response to rotational motion of the accelerometer case with respect to its input axis. Each output is amplified by one of the six preamplifiers which are part of the gimbal mounted electronics. The amplification is required to achieve a high signal-to-noise ratio through the gimbal slip rings. The Y gyro error signal, $E(Y_g)$, then passes directly to the phase sensitive demodulator (DEMOD) located in the power and servo assembly (PSA) while the X gyro error signal, $E(X_g)$, and the Z gyro error signal, $E(Z_g)$, are resolved about the inner gimbal angle by the gyro error resolver. Resolution is required because motion of the spacecraft about the stable member will displace the X and Z gyro input axes away from the outer and middle gimbal torque motor axes. Figure 3-19 shows the configuration of the gyro and gimbal axes and the mechanization of the resolver which transforms the gyro errors to gimbal errors. A similar problem of resolution exists with respect to the middle gimbal angle and misalignment of the outer gimbal torque motor axis with respect to the X gyro input axis. This misalignment is not mechanized by a resolver because the middle gimbal angle is kept small. The three phase sensitive demodulators convert the 3,200 cps gyro error signals to positive dc or negative dc signals with the polarity being determined by the phase. The gimbal error signals and the filtered ADA signals are summed in the gimbal servo amplifier. The use of the ADA in the circuit provides a method of stabilizing the loop by extending the bandwidth without presenting the severe noise and stability problems encountered when passive circuit equalizers (lead-lag networks) are used. The outputs of the gimbal servo amplifiers drive the two gimbal torque motors located at each gimbal axis. The torque motors drive the gimbals to complete the stabilization servo loop.

The initial orientation of the stable member can be changed in either the coarse or fine alignment mode. Signals to reposition the gimbals are injected into the gimbal servo amplifiers during the coarse alignment mode and into the gyros during fine alignment mode. These modes of operation are described in Section V.

3.3.2 STABILIZATION LOOP MECHANIZATION. The purpose of the stabilization loop is to maintain the Stable Member aligned with respect to an inertial frame of reference defined by its inertial components, the three IRIG gyros. Any drift of the platform is sensed by these IRIG's and is manifested by a precessional movement of the float of the affected unit. This float displacement results in an output from the IRIG signal microsyn

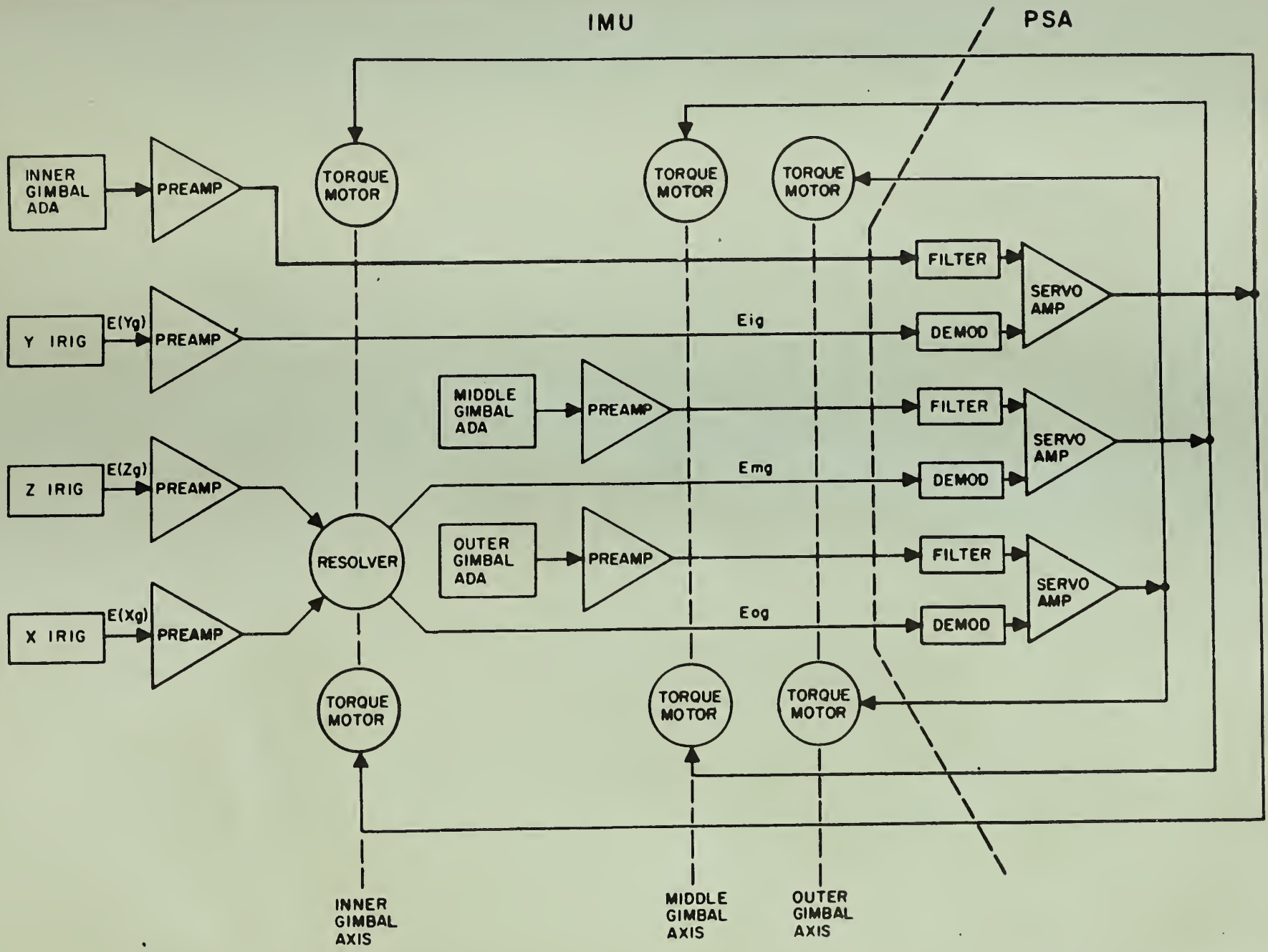
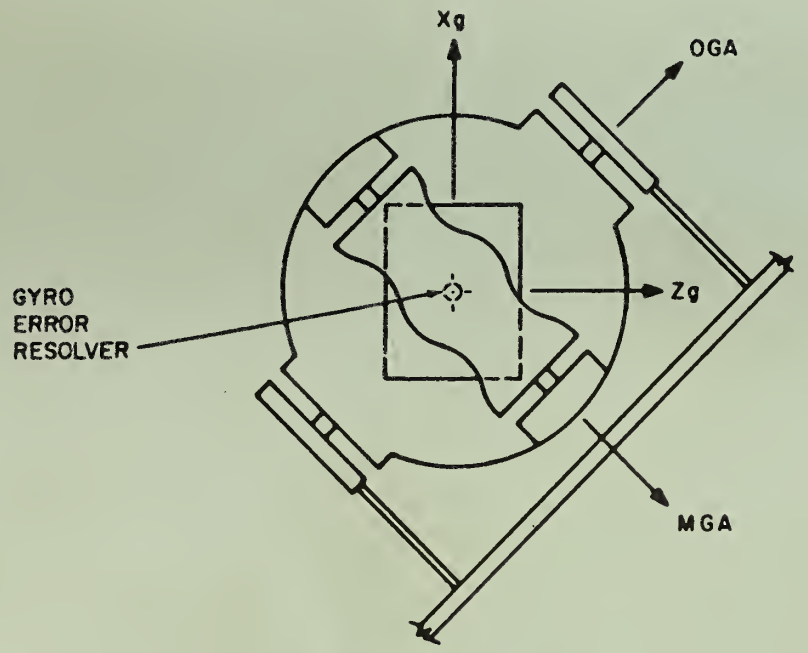


Figure 3-18. Stabilization Loop



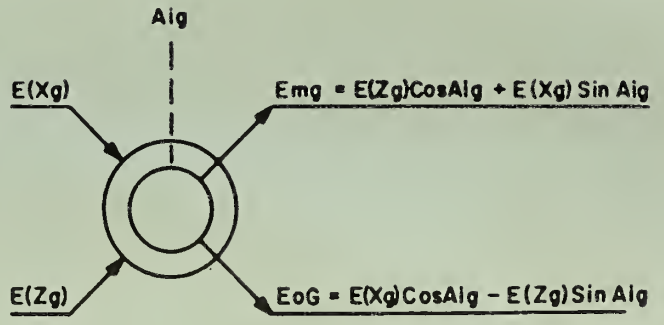


Figure 3-19. Gyro Error Resolver

which is then preamplified and sent to the gimbal servo amplifier. The servo amplifier current output is fed to the appropriate torque motors to restore the stable member to its original reference position. As the stable member is returned to its reference, the movement sensed by the IRIG is opposite in direction but equal in magnitude to the disturbance input and results in a precessional movement of the float. Due to precession, the float returns to its former null position. Since no output is then present from the signal microsyn, the loop is nulled and no further drive signals are applied until another disturbance is introduced into the system.

The components which make up the three stabilization loops are identical with two exceptions. First, the resistances used in series with the torque motor to provide current feedback to the gimbal servo amplifier differ to account for the difference in gimbal inertia. Second, a resolver is required in the middle and outer gimbal loop. This gyro error resolver is shown in figure 3-18. A description of the major components of the stabilization loop follows.

3.3.2.1 25 Inertial Reference Integrating Gyro. The stabilization gyros used in the IMU are the 25 IRIG's. This gyro is a fluid and magnetically suspended, single-degree-of-freedom gyro. It is one of the 25 series of inertial instruments. The 25 designation in the name denotes the case diameter in tenths of inches.

The Apollo 25 IRIG is constructed like other conventional single-degree-of-freedom gyros. See figure 3-20. The gyroscopic wheel assembly spins on preloaded ball bearings. It is enclosed in a sealed, spherical beryllium float. The wheel assembly is driven by a hysteresis synchronous motor in an atmosphere of helium to prevent rusting of the ferrous parts. The helium in the float is at a pressure of one-half atmosphere. The helium also serves to provide good heat transfer within the float. The motor requires 28 volt, 800 cps, two-phase power. The space between the float and outer case is filled with a "suspension and damping fluid", polybromotrifluorethylene. This fluid is maintained at the same density as the float, thereby "suspending" the float with respect to the case and removing the pressure between the float pivot and bearing. The fluid density is kept equal to the density of the float by maintaining the gyro and its fluid at the proper temperature. Two thermistors are submerged in the fluid to indicate fluid temperature.

This fluid also has the effect of damping the float oscillations with respect to the case. The space immediately surrounding the float is entirely filled with fluid. A large part of the non-functional space within the gyro case is consumed by damping blocks which control the damping gap and thereby assists in the control of the damping coefficient.

The Apollo 25 IRIG utilizes ducosyns for signal and torque generation. A ducosyn consists of a separate magnetic suspension assembly and a separate transducer microsyn mounted as a single coaxial-coplanar unit. The ducosyn contains two separate stators mounted to the case and two separate rotors mounted on a common ring on the float assembly. The inside suspension stator assembly consists of eight outwardly projecting poles which are wound and excited to provide magnetic suspension. The outer microsyn stator assembly consists of eight inwardly projecting poles which are wound and used to generate either output signals or torque. The outer rotor is the transducer rotor and consists of four unwound salient poles projecting outward. The inner rotor is the magnetic suspension rotor which is cylindrical and unwound. In the 25 IRIG, the signal generator ducosyn is mounted on the

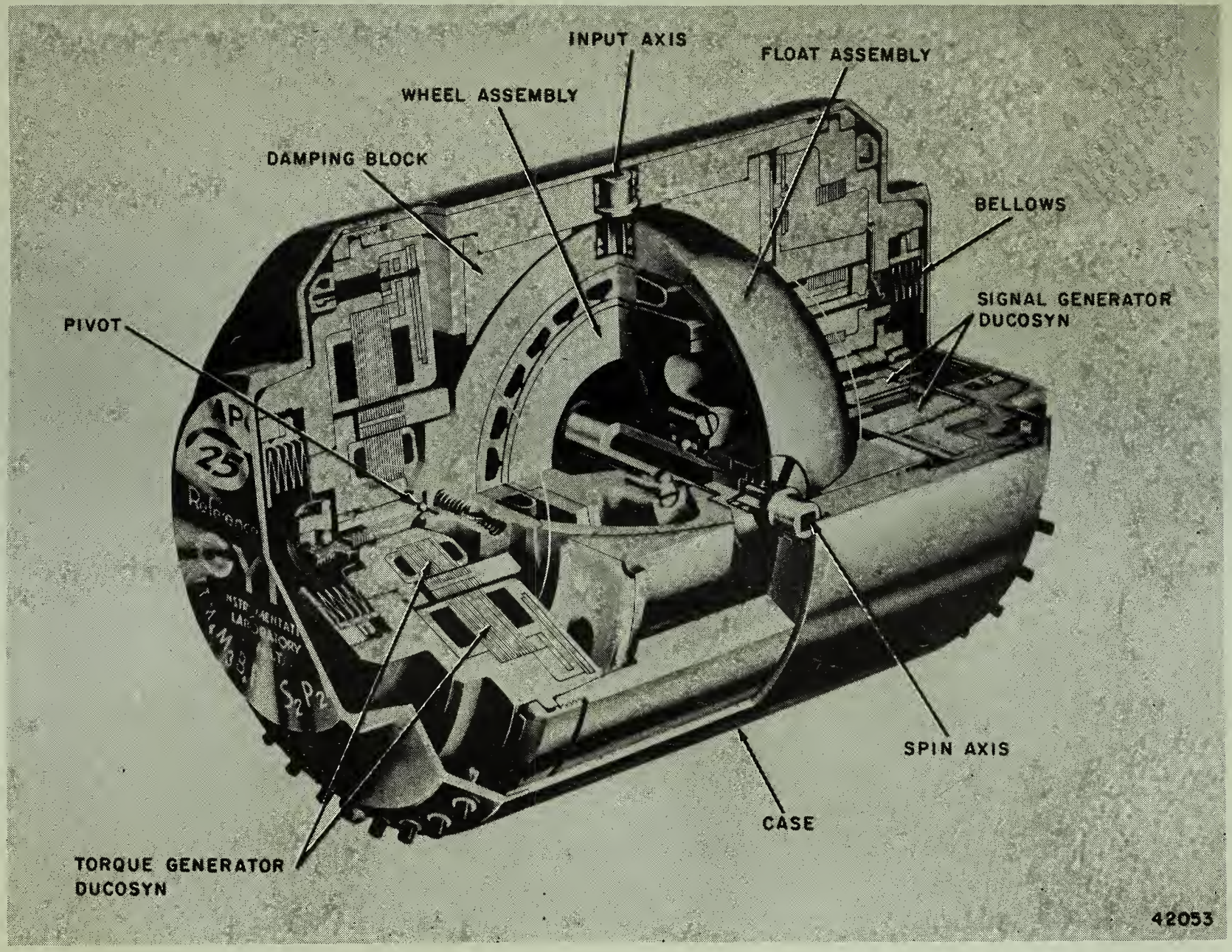


Figure 3-20. 25 IRIG (Generalized Pictorial Schematic)

positive output axis end of the float to provide magnetic suspension and to serve as a transducer to provide an electrical analog signal proportional to the position of the float. A torque generator ducosyn is mounted on the negative output axis end of the float to provide magnetic suspension and to serve as a transducer to convert an electrical error signal into a torque about the output axis. The 25 IRIG magnetic suspension and the primary of the signal generator require a 2 volt, 3,200 cps, single-phase excitation. In addition to the magnetic and fluid suspension, the 25 IRIG also has a set of pivots and bearings on the output axis. In this gyro, the pivots are part of the float assembly. Both the pivots and bearings are made of tungsten carbide. It should be noted that under normal environmental conditions, the pivots of the gyro never touch the bearing.

Figures 3-21 and 3-22 illustrate the signal and torque ducosyn of the 25 IRIG. The signal ducosyn secondary has a center tap output capability however this is not used. The output signal of the signal ducosyn is an amplitude modulated suppressed carrier 3,200 cps signal. The scale factor of which is approximately 12 millivolts per milliradian of float displacement.

During final 25 IRIG assembly, a pre-alignment package is added to the signal generator end of the case. This package contains the magnetic suspension capacitors, padding resistors, thermistors, a main heater and an auxiliary heater. Addition of this package makes the gyro a partially pre-aligned gyro. When the gyro is placed in the stable member, a heater is added to the torque generator end.

3.3.2.2 Angular Differentiating Accelerometer. The ADA (figure 3-23) is a fluid-damped torsional pendulum. The pendulum consists of a rotor in a damping fluid and suspended by two torsion wires along the input axis. The rotor is suspended so that the rotation of the outer case about the axis of the torsion wire causes the pick-off coils in the rotor to move through the eight flux paths from the permanent magnets located on the case. The movement of the pick-off coils in the magnetic field induces a voltage in the coils. The magnitude of the induced voltages will depend on the angular displacement of the rotor about is input axis. When there is no relative motion between the pick-off coils and the magnets, there is no output from the ADA. When the motion of the case is below the natural frequency of the pendulum, the rotor will move and attempt to follow the case. However, as long as the rate of case acceleration is increasing, the rotor will fall farther and farther behind the case causing relative motion between the pick-off coils and the magnitude field. As soon as the angular acceleration of the case becomes constant the rotor will maintain a new fixed position with respect to the case due to the torque resulting from the twisting of the torsion wires. There will no longer be an output signal since the relative motion has ceased. Therefore, for case motion below the natural frequency, the suspension wire exerts primary control over the rotor motion providing an output signal proportional to the rate of change of acceleration.

For input signals above the natural frequency of the rotor, the inertia of the rotor causes the rotor to remain stationary while the case rotates about it. The relative motion between the case and the rotor results entirely from movement of the case. Therefore, for case motion above the natural frequency of the pendulum, the output signal is proportional to the angular velocity about the input axis.

The cylindrical shaped ADA is approximately 3/4-inch in diameter and 3/4-inch in length. Eight pairs of permanent magnets are located around the rotor and mounted to the case. The pick-off coils are limited to 15 degrees of motion due to a stop on the rotor. The output signal is carried from the rotor to the terminals by the fine-wire, friction-free suspension system. To provide the necessary

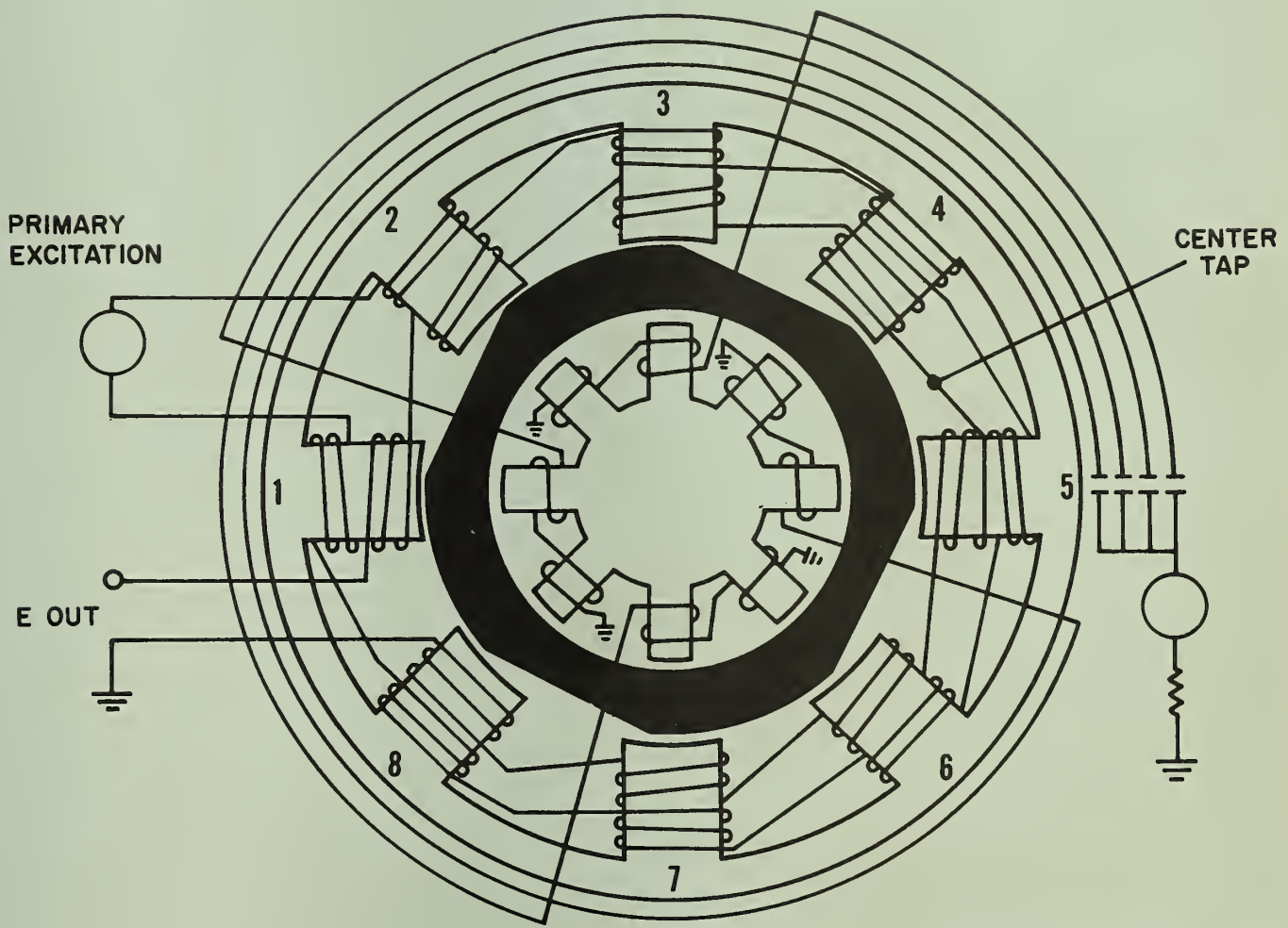


Figure 3-21. Signal Ducosyn

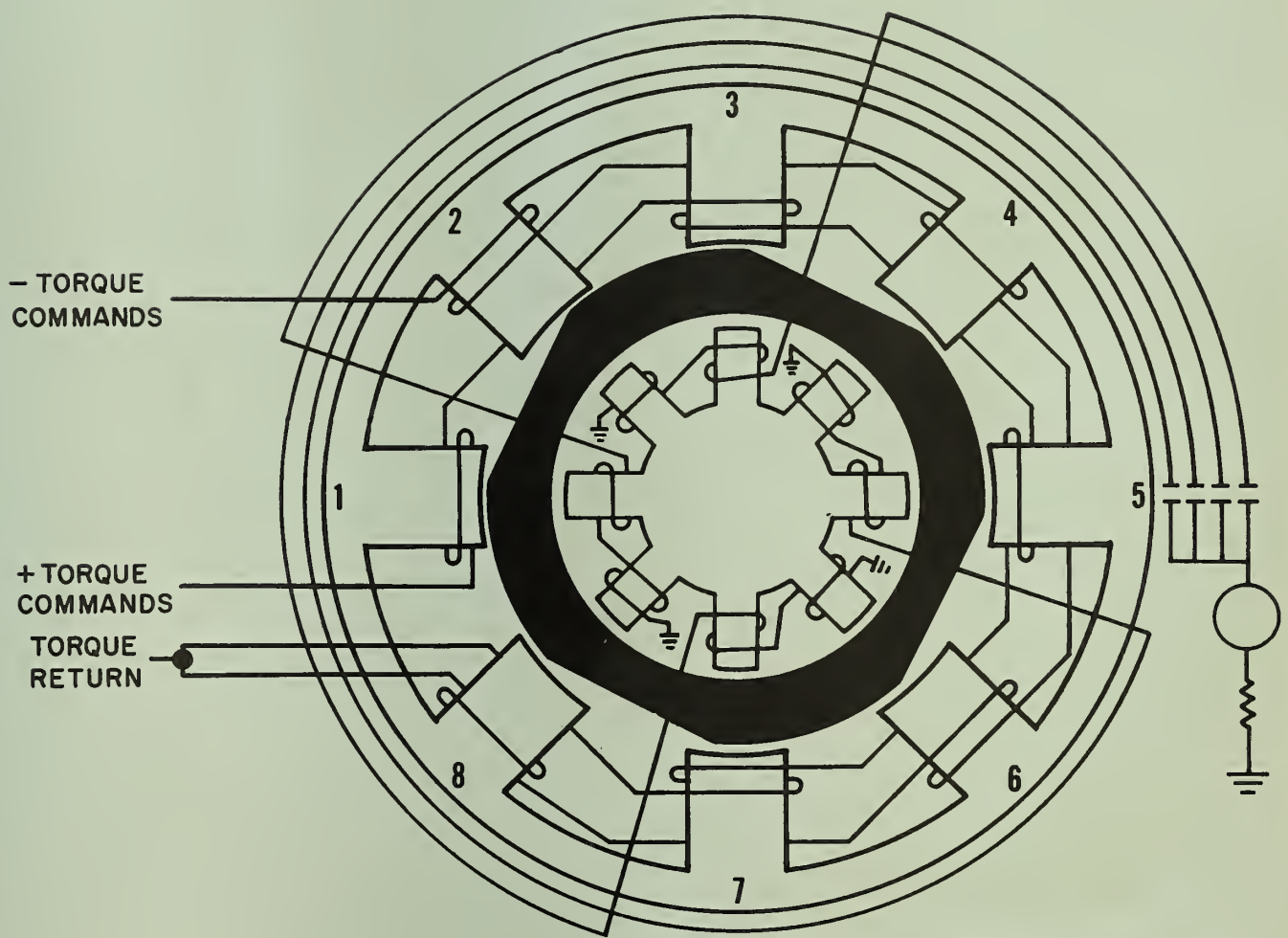


Figure 3-22. Torque Ducosyn

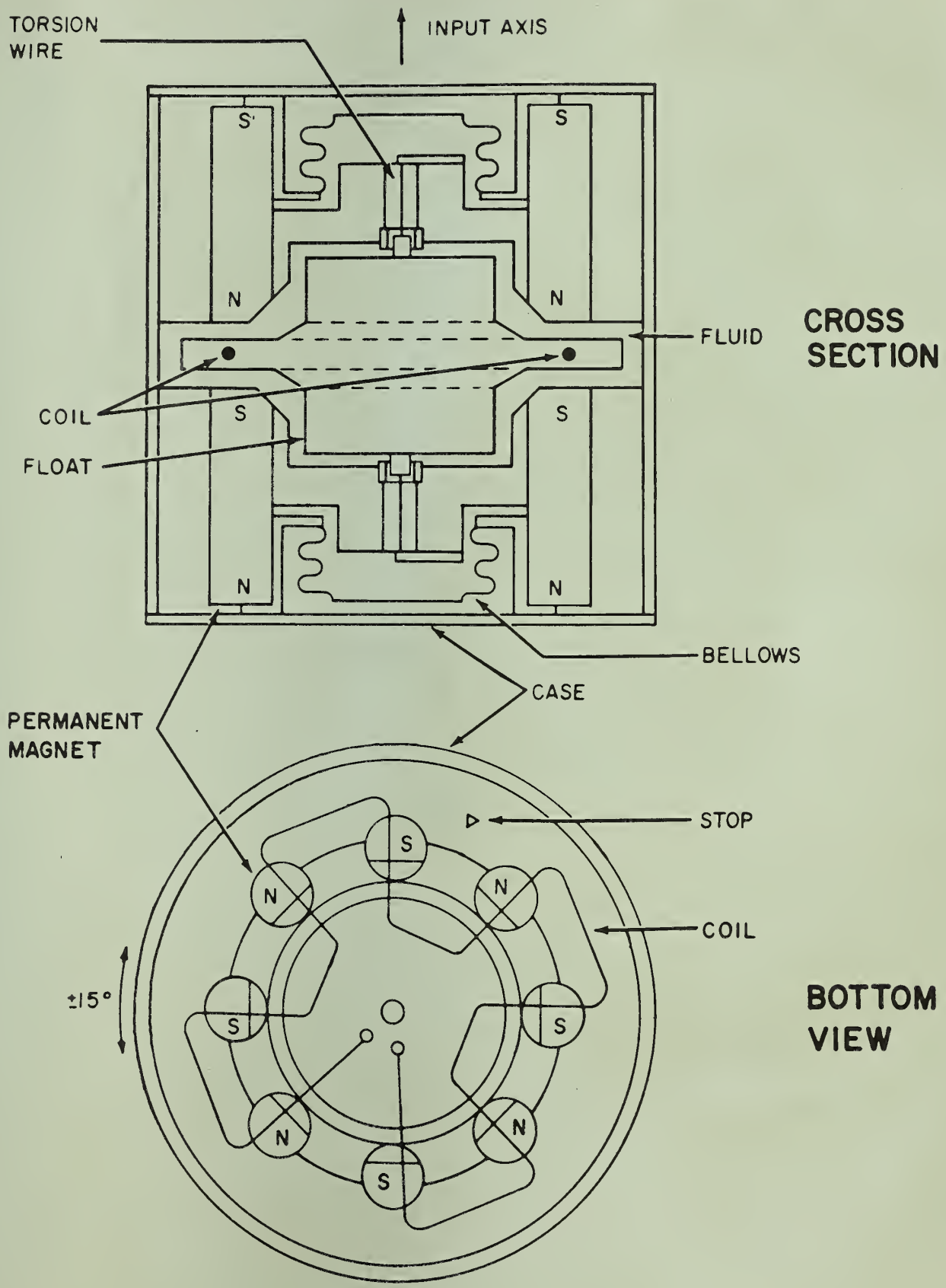


Figure 3-23. Angular Differentiating Accelerometer

damping and resistance to high g loading, the ADA rotor is floated in a high density floatation and damping fluid. The rotor is balanced to insure that the centers of mass rotation and buoyancy coincide so that the ADA is insensitive to linear accelerations. The fluid used for floatation requires an operating temperature of 82 degrees F. to 137 degrees F. to keep the ADA characteristics within tolerances. Since variations in temperature cause the fluid to expand or contract, bellows are located at each end of the case to allow the fluid to expand so ADA parts will not be strained.

The ADA output voltage is a DC voltage, the polarity of which is dependent upon the direction of the input motion. The scale factor or input-output relationship of the ADA is .525 millivolts per degree per second; however, this relates only to the relative motion of the pendulum to the case.

3.3.2.3 ADA Preamplifier. The ADA preamplifier is a DC amplifier that employs a feedback to reduce the gain at low frequencies. The feedback also provides the preamplifier with DC stability, low amplifier drift and a symmetrical output. One ADA preamplifier is packaged in a single module and mounted on the stable number. The other two preamplifiers are packaged in a common module and mounted on the middle gimbal.

The DC gain of the ADA preamplifier is 62 ±3%, and its saturation outputs are +20 and -18 volts with +.32 and -.29 volt inputs, respectively.

3.3.2.4 25 IRIG Preamplifier. The gyro error signal is amplified by the preamplifier to achieve a high signal-to-noise ratio in transmission of the error signal through the gimbal slip rings to the stabilization amplifier in the PSA. The IRIG preamplifier is an AC amplifier with transformer-coupled input and output. The gain of the preamplifier is approximately 180 volts-per-volt. There are three preamplifiers, all mounted in a single module on the stable member as a part of the gimbal mounted electronics.

3.3.2.5 Gimbal Servo Amplifier. The gimbal servo amplifier sums the signals from the 25 IRIG, ADA and an output current sampling resistor. The output of the amplifier, due to the current sampling resistor, acts as a constant current source driving the torque motors. Three gimbal servo amplifiers are required. All are packaged in identical modules in the PSA. An ADA filter and a 25 IRIG demodulator are also mounted in each module. The ADA filter provides DC decoupling between the ADA preamplifier and the stabilization amplifier. It also provides high signal attenuation for frequencies at which the gimbals may resonate. The 25 IRIG demodulator changes the 3,200 cps gyro error signal into a DC signal for use in the gimbal servo amplifier. The demodulator is a full-wave, bridge-type followed by a first order filter. A feedback network is utilized in the stabilization amplifier to provide the desired dynamic characteristics for stabilization loop operation. The amplifier gain for each stabilization loop is selected by the connection to the module. Refer to figure 3-24.

3.3.2.6 Torque Motors. Two DC torque motors are used for driving each gimbal. Located in the intergimbal assembly, these torque motors will each supply 1.3 foot pounds per ampere of current.

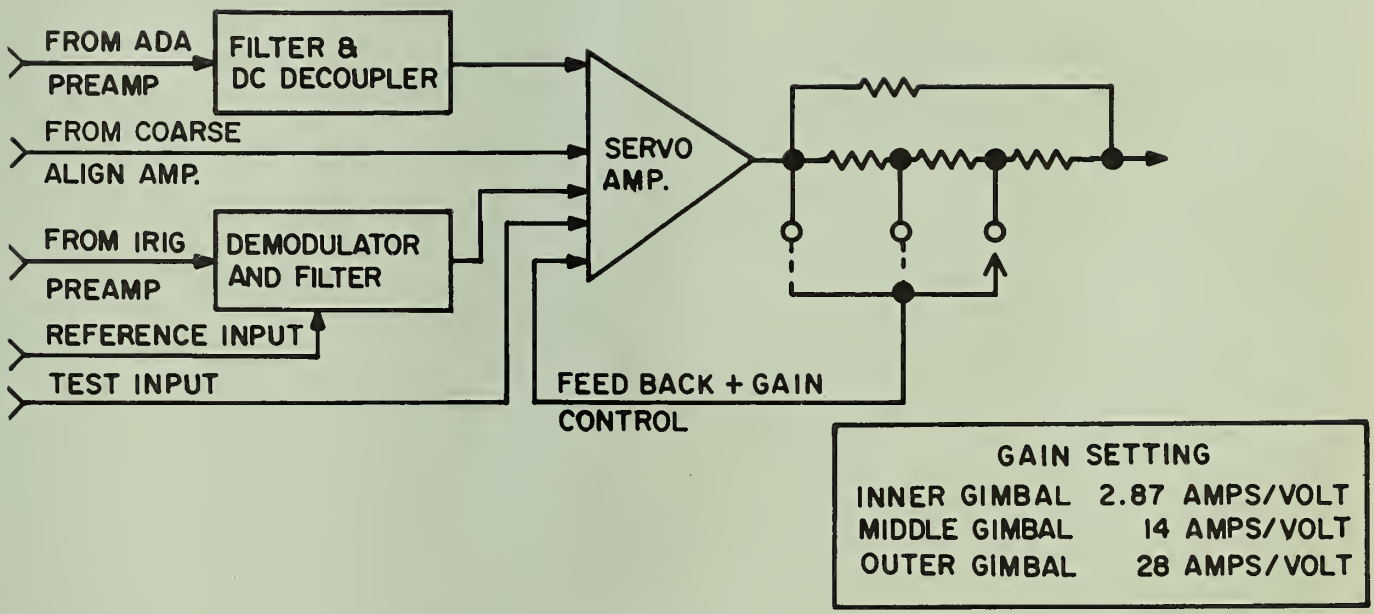


Figure 3-24. Gimbal Servo Amplifier

3.4 GYRO TORQUING OPERATION

The purpose of the gyro torquing loop is to allow the introduction of external loop control driving signals into the stabilization loops during closed loop conditions. By purposely introducing a torque to the IRIG floats, it is possible to cause the IMU gimbals to drive to new positions. This permits fine alignment of the stable member with a great degree of positioning accuracy.

Figure 3-27 shows the complete gyro torquing loop. When gyro torquing is required during the ISS fine align mode, the computer sends a train of TM pulses to the ternary current switch. Along with the torque command pulse train, the computer sends a train of reset pulses to control the pulse width of the T pulses applied to the gyro. Figure 3-28 shows the timing of the pulses throughout the gyro torquing loop. Note that whenever the gyro does not draw the 120 MA torquing current, the dummy current switch does; thereby, presenting a constant load to the constant current source.

3.4.1 TERNARY CURRENT SWITCH. The ternary current switch (figure 3-25) will convert plus and minus torque commands (TM) received from the AGC into DC current pulses for use in fine alignment of the stable member. During prelaunch operation, these pulses compensate the 25 IRIG's for earth rotation.

The +TM input pulse to the ternary current switch is applied to a flip-flop or bistable multivibrator which biases the +T current switch to an on condition. With the +T current switch on, a constant dc signal is passed through the +T current switch as a 120 milliampere nominal signal. The flip-flop remains in a set condition once a +TM pulse has been received until the flip-flop is reset by a gyro reset pulse received from the AGC. In the reset condition, the outputs from the flip-flops are applied through an "and" gate to activate a dummy current switch which passes a constant DC signal.

The current fed to the gyro torque microsyn is modified by the equalizing network of the calibration circuit and applied to the microsyn. The torque currents and dummy current are then summed at the input to the current monitoring resistor which permits the measurement of the loop current. The ground return is supplied through the scale factor resistor which is also used as a current sensor for the differential amplifier. The differential amplifier has a 6 volt precision voltage input reference and by comparing the reference with the scale factor resistor voltage, it is able to accurately control the current control amplifier to supply the exact 120 MA current.

The purpose of the dummy current switch is to provide a constant load on the constant current supply. This enables the supply to maintain a well regulated current, free of transients, to the IRIG torque generator through the calibration circuit.

3.4.2 CALIBRATION MODULE. The calibration module (figure 3-26) provides a compensation network to make the torque generator winding appear as a resistive load to the +T of -T current pulses. The +T, 120-milliampere, DC pulse is applied to the odd numbered 25 IRIG torque generator windings and the -T, 120 milliampere, DC pulse is applied to the even numbered 25 IRIG torque generator windings. When no error signal is present, the dummy current switch current is required to complete the current control loop for a no-torque condition. The 120 milliamp current is regulated by the DC differential amplifier which samples the voltage of the calibration module and compares it with the output of the precision voltage reference (PVR). It also conditions each gyro

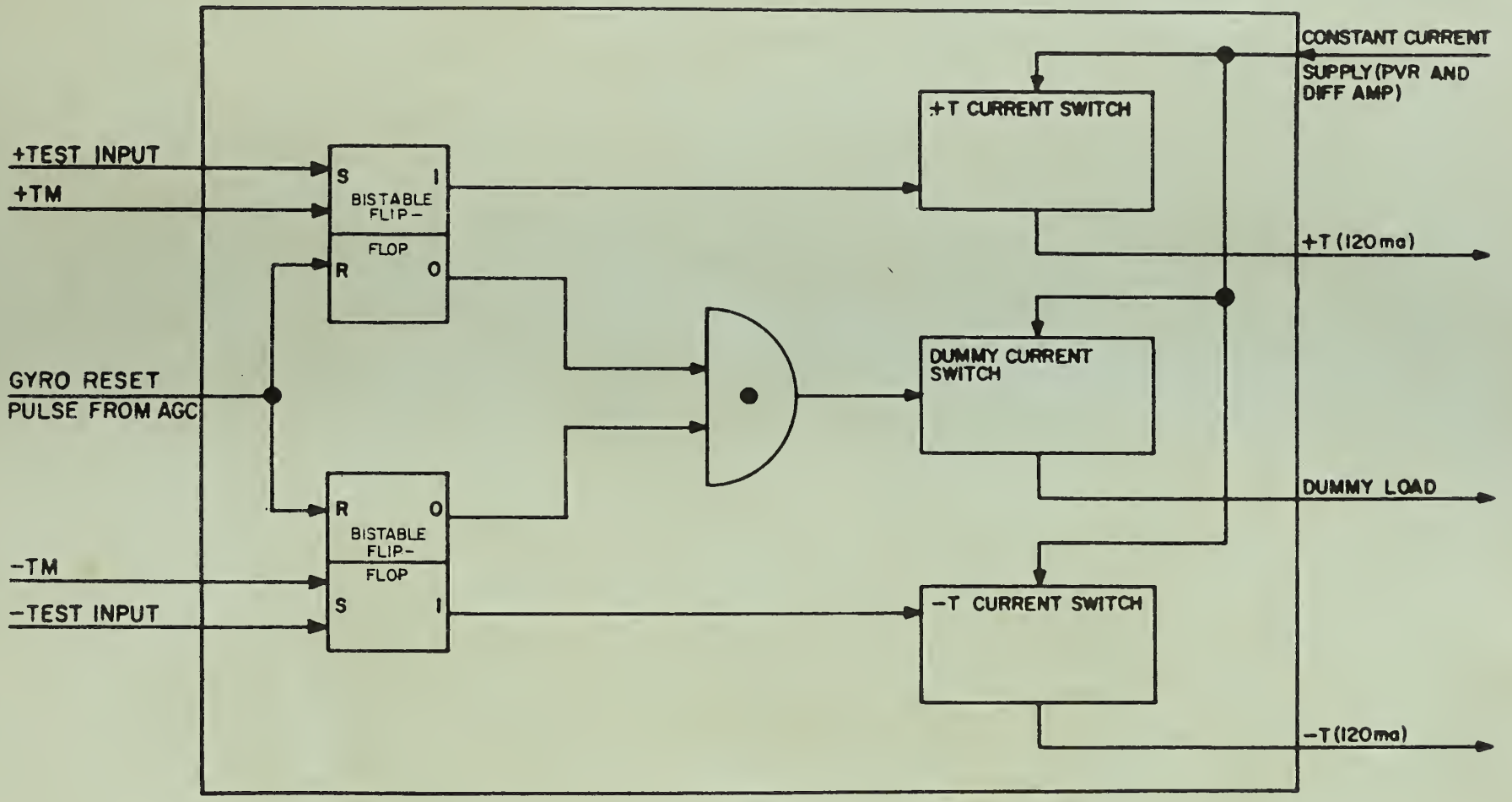


Figure 3-25. Ternary Current Switch, Block Diagram

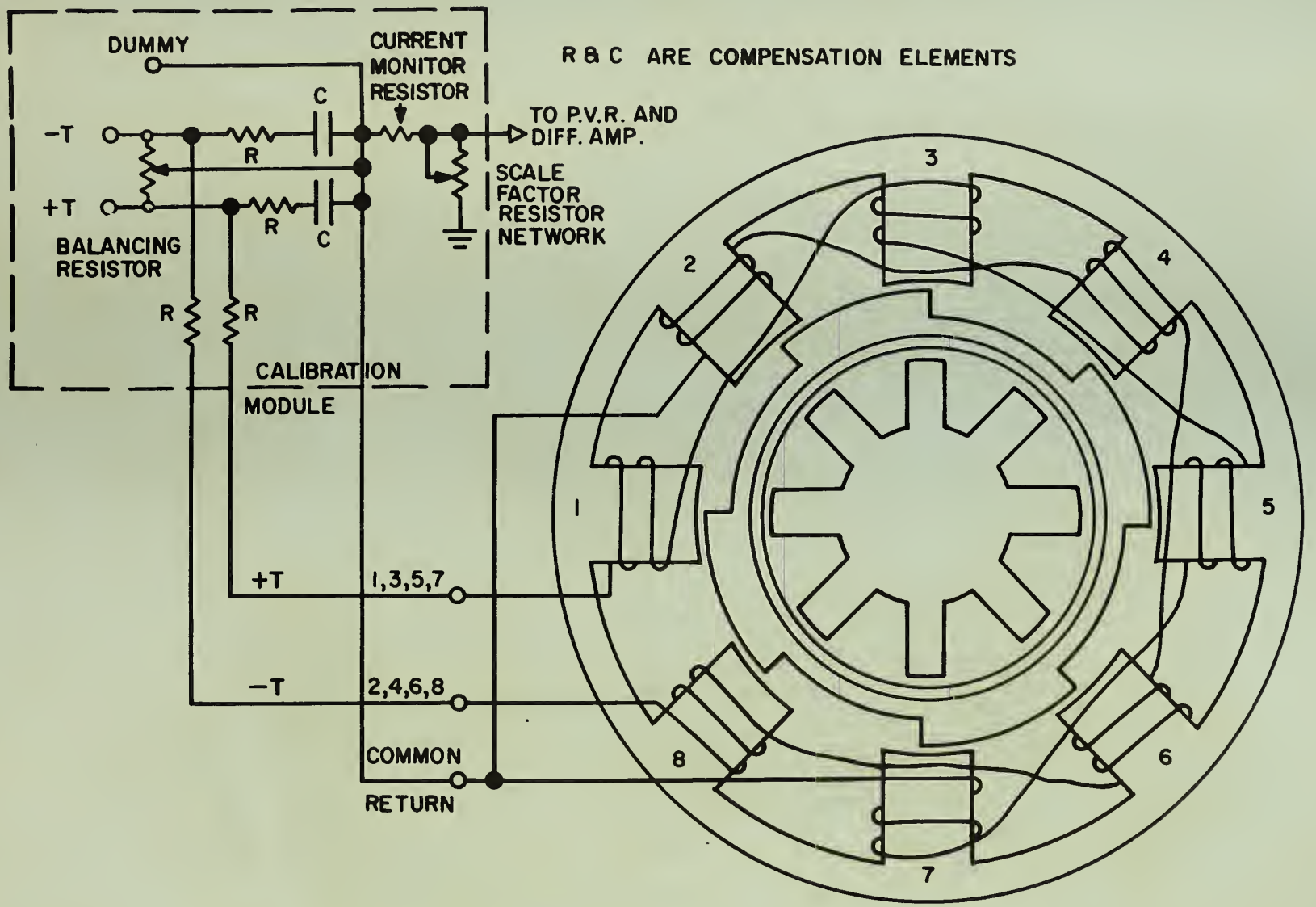


Figure 3-26. Calibration Circuit

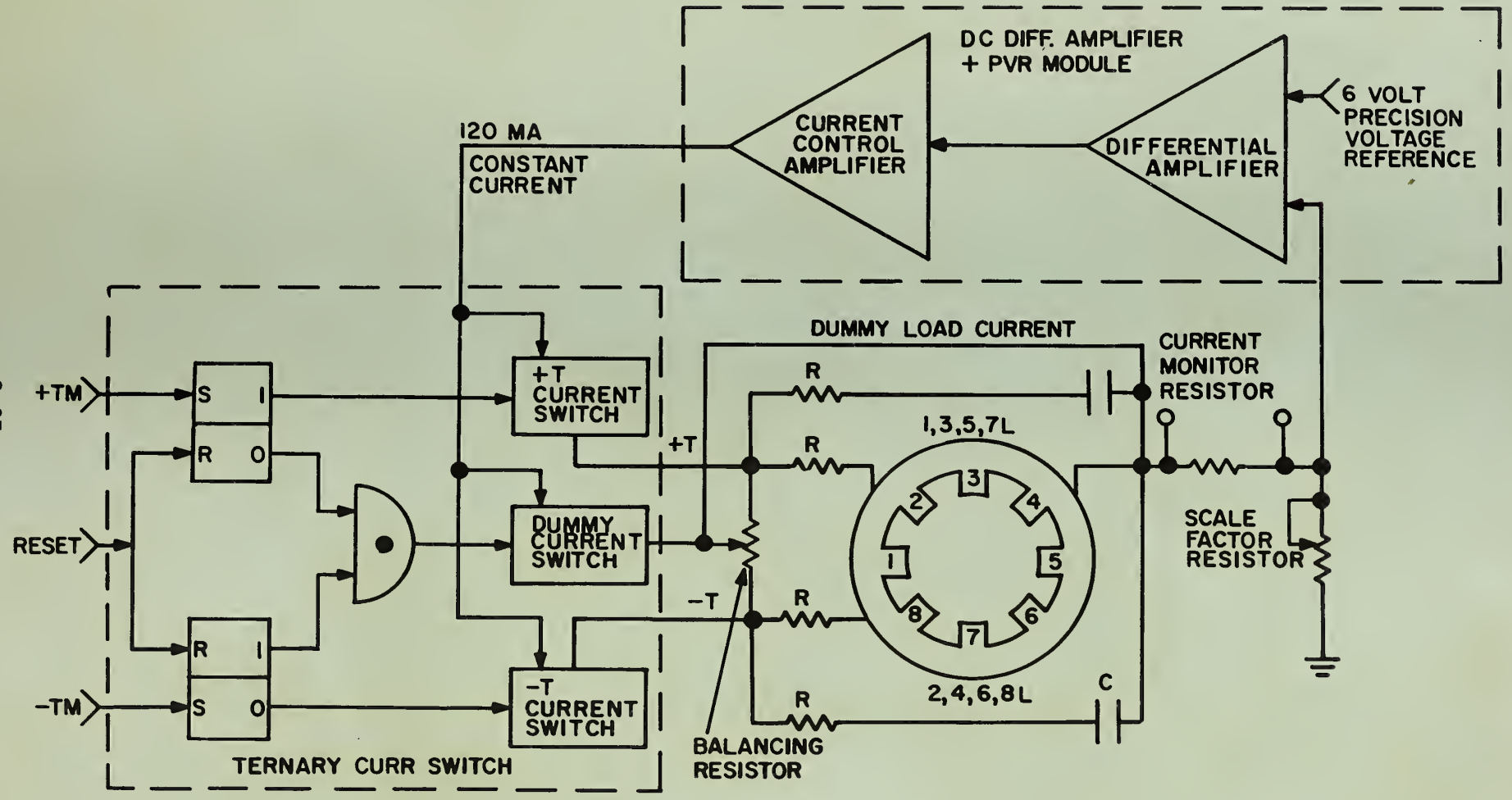


Figure 3-27. Torquing Loop, (IRIG)

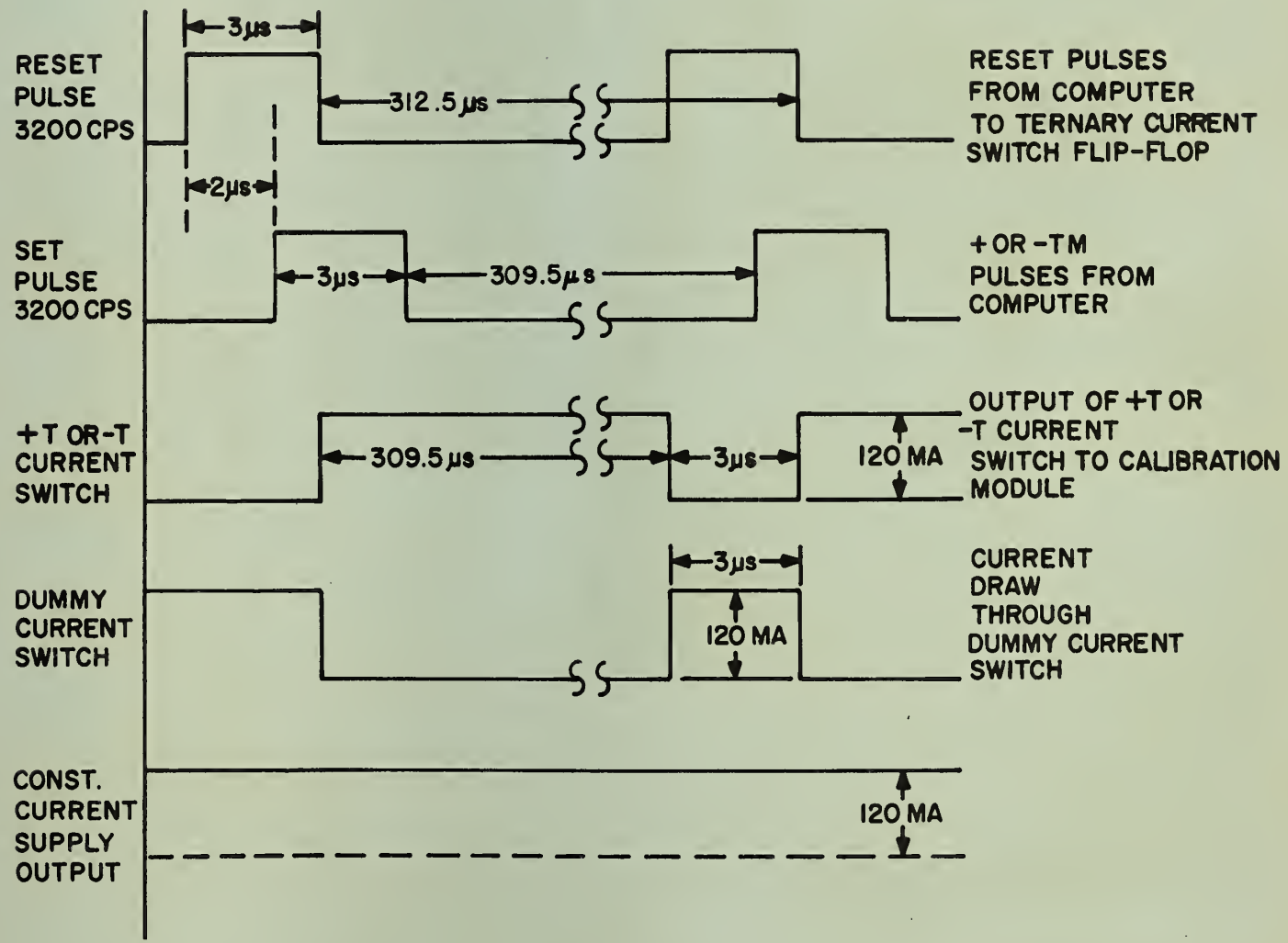


Figure 3-28. IRIG Torquing Loop Pulse Relationship

to have precisely the same scale factor as every other gyro so that circuit compensation is unnecessary with a gyro or computer change.

3.5 ACCELEROMETER LOOP

The purpose of the three accelerometer loops is to measure the acceleration of the stable member along three mutually perpendicular axes and to integrate this data to determine velocity. The velocity data is utilized by the AGC to compute the spacecraft trajectory.

3.5.1 ACCELEROMETER LOOP OPERATION. The accelerometer loops have three 16 PIP's which are used to sense linear acceleration of the stable member. The input axes of the 16 PIP's are oriented as described in figure 3-14. Velocity outputs of the PIPA loops to the computer are generated whenever the stable member is accelerated due to thrust applied to the spacecraft or when the guidance and navigation system is subjected to gravitational forces while on earth. The output signals are checked to determine the direction of the acceleration so torquing signals can be generated to torque the 16 PIP's back to null. While this process is occurring, signals, representative of incremental velocity changes, are generated by the loop and sent to the AGC. A typical accelerometer loop data flow is shown in figure 3-29.

The 16 PIP signal generator ducosyn outputs are 3,200 cps error signals which are proportional to the rotation of the pendulum about its output axis. The two outputs are amplified by the preamplifier and the AC differential amplifier. The amplified signals are then transmitted to the interrogator which also receives the interrogator pulse and the switching pulse from the AGC. These inputs are used to generate the plus torque command, the minus torque command and the data pulse.

The signals generated by the interrogator are then applied to the binary current switch. The plus and minus torque commands are used to turn on the plus and minus current switches. The data pulse is used to generate the positive (P) and negative (N) velocity pulses which are sent to the forward-backward counter. The output of the binary current switch is sent to the calibration module and then to the PIP torque generator ducosyn where a torque is developed which will move the pendulum back toward null. A feedback signal from the calibration module to the DC amplifier and the precision voltage reference is used to regulate the torquing current supplied by the binary current switch. The positive and negative pulses are subtracted in the forward-backward counter to determine the difference. During normal accelerometer loop operation when no acceleration is being sensed, an equal number of positive and negative pulses are generated. When an acceleration is sensed, more of one type of pulse will be generated. This unbalance produces either plus ΔV or minus ΔV pulses which are sent to the AGC and accumulated as spacecraft velocity changes.

3.5.2 ACCELEROMETER LOOP MECHANIZATION. The components which make up the three accelerometer loops are identical. A description of the major components of an accelerometer loop follow.

3.5.2.1 16 PIP. (Refer to figure 3-30.) The 16 PIP is used in the IMU as an acceleration sensitive device. When fixed in its associated accelerometer loop, the 16 PIP becomes an integrating accelerometer. The 16 PIP is basically a pendulum-type device consisting of a cylinder with a pendulous mass unbalance (pendulous float) pivoted with respect to a case. The axis of the pivots defines the output axis (OA). The space between the pendulous float and the case is filled with fluid. A signal generator ducosyn is mounted on the positive end of the output axis

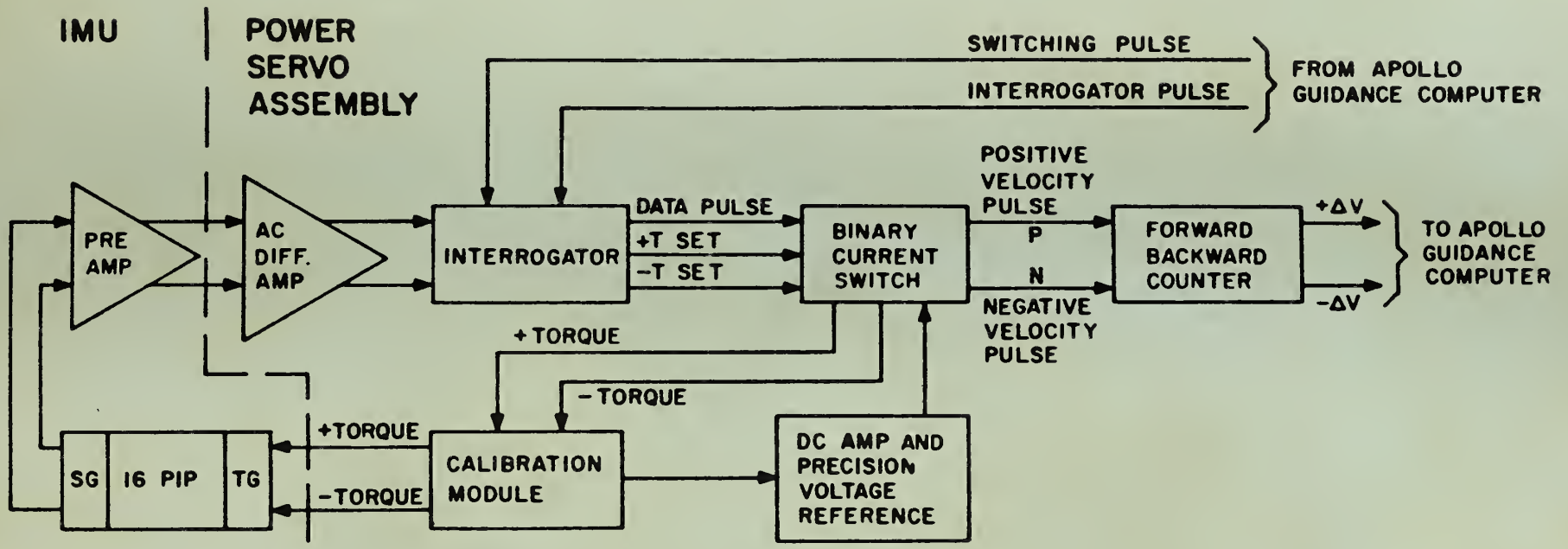


Figure 3-29. Accelerometer Loop

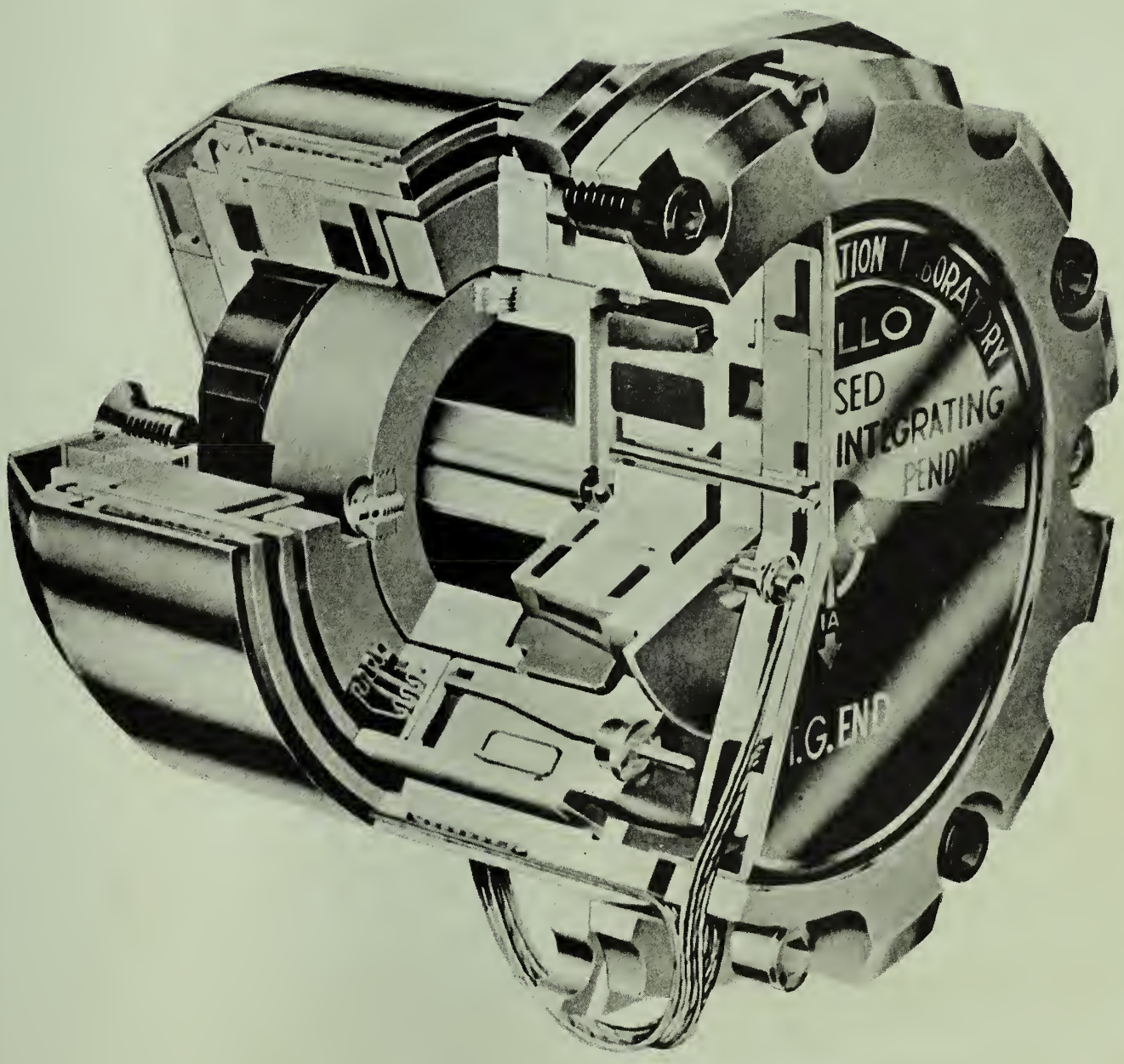


Figure 3-30. 16 PIP

to provide magnetic suspension of the float. The torque generator ducosyn also acts as a transducer to convert torque signals, in the form of electrical pulses, into mechanical torque about the output axis. A 2-volt rms, 3,200 cps, single-phase excitation is required for the 16 PIP magnetic suspension and primary of the signal generator.

The float body is a cylinder of beryllium which is fitted to a shaft on which the float pivots. The rotors of the ducosyns are mounted on the ends of the float body. The complete float assembly is placed in the main housing assembly and the space serves as both a fluid suspension of the float and as a viscous damping for the fluid. The main housing contains a bellows assembly to take up the expansions and contractions of the fluid during heating. The end housings of the 16 PIP contain the ducosyn stators and the pivot bearing. The magnetic suspension units have tapered stator poles and a tapered rotor so that magnetic suspension forces will be developed in both the axial and radial directions. The main housing assembly is completely covered by a case which provides magnetic shielding and a hermetic seal of the unit. Heating coils are placed between the main housing and case to heat the suspension fluid to the proper temperature. All electrical signals for the 16 PIP are routed through the torque generator end of the case.

With an acceleration being sensed along the input axis of the 16 PIP, the float rotates from the null position. This rotation is sensed by the signal generator ducosyns. The reference excitation voltage of the signal generator is snychronized with the AGC clock which is the reference for all system and loop timing.

The output of the secondary of the signal generator ducosyn consists of two amplitude-modulated, supressed-carrier signals, one of zero phase and the other of π phase. These two 180-degree out-of-phase signals are phase shifted 45 degrees from the reference excitation by the effect of a resistor in series with the primary winding and amplified by a preamplifier mounted on the stable member.

3.5.2.2 AC Differential Amplifier. The amplifier zero and π phase signals from the preamplifier are applied as separate inputs to the AC differential amplifier. The inputs are then summed, amplified and sent to a phase splitter. The two resulting signals are then sent to the interrogator.

3.5.2.3 Interrogator. The interrogator analyzes the AC differential amplifier outputs to determine the direction of 16 PIP float movement and to generate appropriate torquing commands. Refer to figure 3-32 for a block diagram of the interrogator.

The two amplified AC signals from the AC differential amplifier go to two Schmitt triggers where they are demodulated. One trigger is driven by the zero phase signal while the other is driven by the π phase signal. When the thresholds of the triggers are exceeded, the voltage levels switch abruptly from a zero voltage to some positive voltage value. The input signals are timed so that only one trigger can be positive at a time. The outputs of the triggers are pulse trains separated in phase from each other by 180 degrees. The width of the pulses is determined by the time during which the voltage driving the Schmitt trigger exceeds the threshold level.

Interrogator pulses (IP) are also being received by the Interrogator. The interrogator pulses consist of pulses three microseconds in width, occurring at 3,200 cps and timed to occur 135 degrees after the positive zero crossing of the reference excitation. With this phasing, the interrogator pulses occur at the 90 degree peaks of the zero phase or π phase input signals. The interrogator pulse therefore occurs in the middle of the +T trigger pulses if the pendulum angle is positive and in the middle of the -T trigger pulses if the pendulum angle is negative. The trigger pulses and the differentiated interrogator pulses are "anded" by a summing circuit and a threshold amplifier and inverted and sent to a bistable multivibrator (flip-flop) circuit. The leading edges of these pulses are used to set or reset the flip-flop, A + T pulse setting the flip-flop and a -T pulse causing a reset. A set voltage or a reset voltage will always be present out of the flip-flop. The outputs of the bistable multivibrator are sent to two "and" circuits which are also driven by the switching pulses. The switching pulses consist of a train of clock-driven 3,200 cps pulses timed to occur two microseconds after the leading edges of the interrogator pulses. The outputs of the "and" circuits are called the T+ set pulse and the T- set pulse. The other output of the interrogator, the data pulse, is formed by the differentiation of the trailing edge of the interrogator pulse. The pulse chart of figure 3-31 shows the relationship of the inputs and outputs of the interrogator.

3.5.2.4 Binary Current Switch. The binary current switch utilizes the outputs of the interrogator to generate 16 PIP torquing current and velocity change pulses. Refer to figure 3-33 for a block diagram of the binary current switch.

The T+ set and T- set pulses furnish the input to a bistable or flip-flop multivibrator which controls the + set and -set sides, respectively. If the flip-flop is already in the + set condition, a succession of T+ set pulses will maintain the set condition. The + set condition will persist until the pendulum angle decreases past zero to an angle sufficiently negative to overcome the threshold of the second Schmitt trigger in the interrogator. At this time, a T- set pulse appears and causes the flip-flop to go at -set condition. The outputs of the flip-flop control the two current switches. If the flip-flop is in a + set state, the + set output is applied to the base of a transistor which closes the path from the + 120 volt supply to the 16 PIP T+ torquing coils. If the flip-flop is in the -set state, the path to the T- torquing coils is closed.

The outputs of the flip-flop also go to two separate "and" gates where they are "anded" with the data pulses. This "anding" produces positive velocity pulses and negative velocity pulses. Each pulse represents an increment of velocity and is defined by the loop scale factor in terms of centimeters-per-second-per-pulse. The positive and negative pulses to go the forward-backward counter.

3.5.2.5 Calibration Module. The calibration module compensates for the inductive load of the 16 PIP torque generator ducosyns and regulates the balance of the plus and minus torques. The calibration module consists of two load compensation networks in parallel with the torquing coils of the 16 PIP. The torquing coils, along with the compensation network, appear as a resistive load to the output of the binary current switch. A variable resistor regulates the amount of torque developed by the torquing coils. Adjustment of this resistor regulates precisely, and thereby balances, the amount of torque developed by the plus and minus torquing coils. This balancing insures that for a given torquing current an equal amount of torque will be developed in either direction. The odd numbered coils

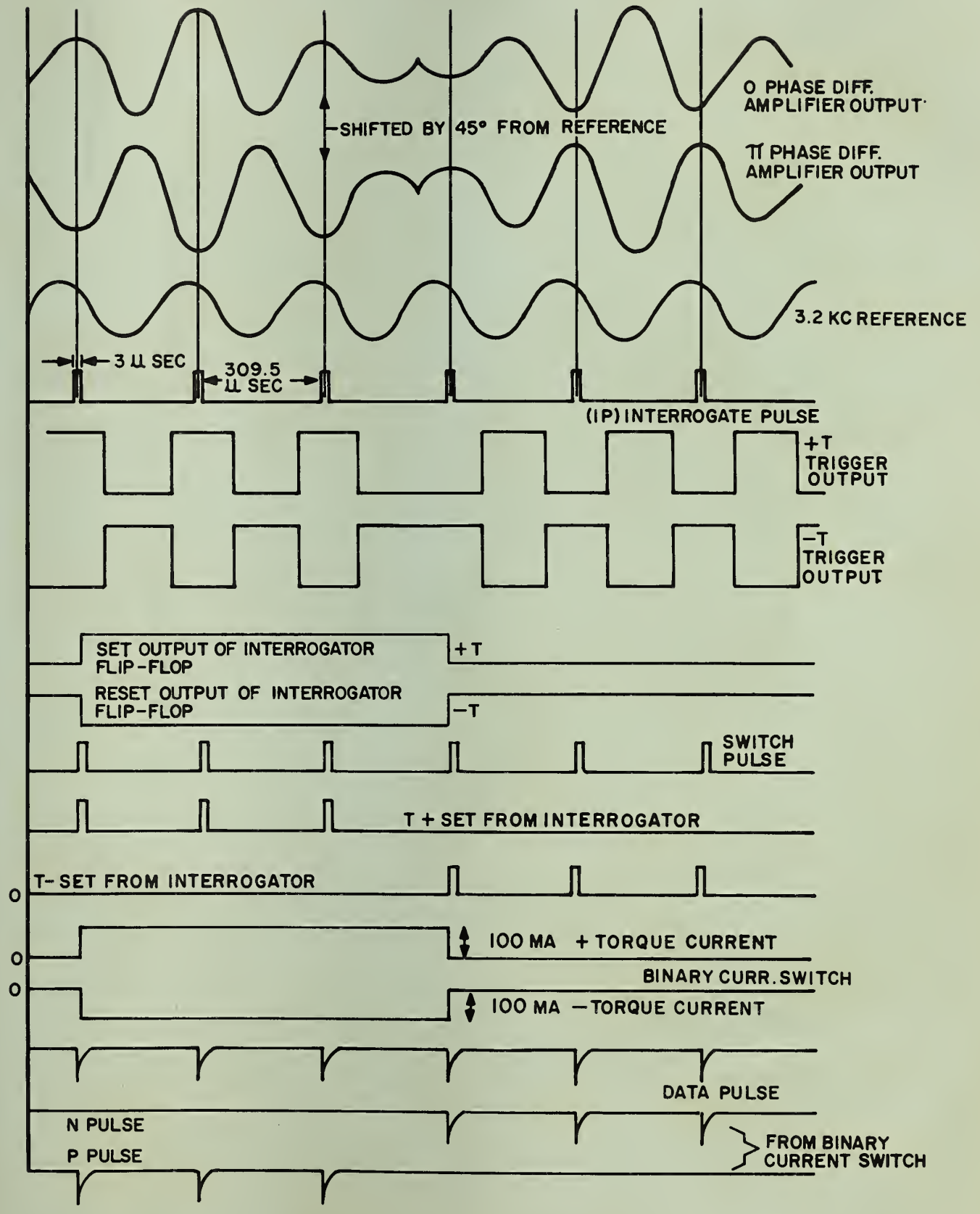


Figure 3-31. Pulse Diagram - PIPA Loop

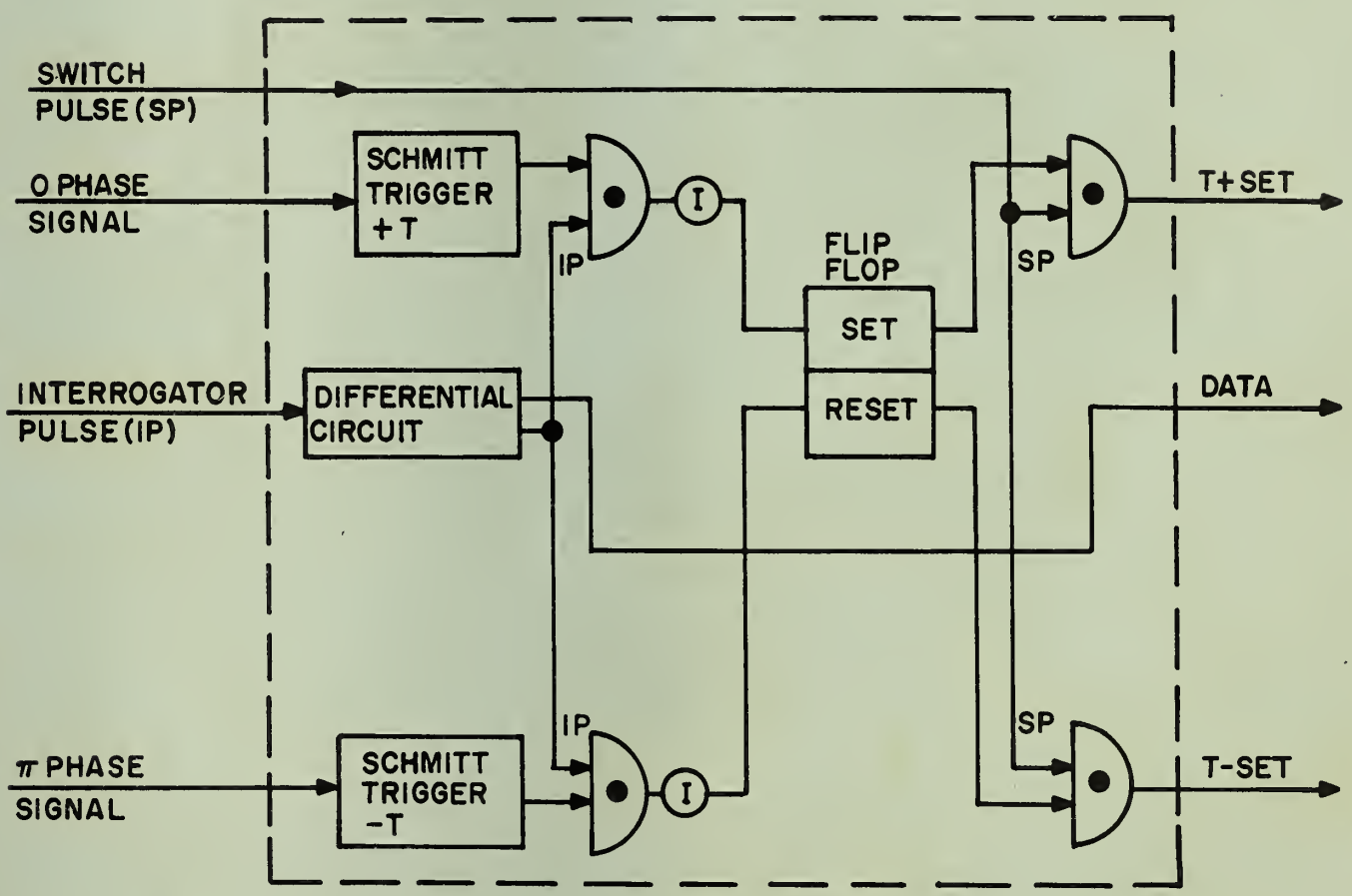


Figure 3-32. Interrogator

of the torque generator ducosyn are excited to develop a plus torque and the even numbered coils are excited to develop a minus torque.

The calibration module also includes a current sampling resistor in series with the torquing coils. A nominal six volts is developed across this resistor due to the torquing current. This calibration module is similar in design and function to the IRIG calibration circuit of figure 3-26.

3.5.2.6 Constant Current Source. The constant current source maintains the current through the torquing coils of the torque generator ducosyn at 100 milliamperes. The constant current source contains a precision voltage reference and a differential amplifier. The precision voltage reference is supplied with regulated 32 volt DC, and through the use of precision circuits, develops an accurate six volts for use as a reference. The six volts developed by the precision voltage reference is compared with the six volts developed across the current sampling resistor in the calibration module. This comparison is made by the DC differential amplifier. Any deviation of the current switch torquing current from 100 milliamperes will develop an error signal output from the DC differential amplifier. This error voltage affects the resistance of transistors which are in series with the 120 volt DC source and the torquing coils. By varying the transistor resistance, the torquing current to the torquing coils can be maintained at 100 milliamperes.

3.5.2.7 Forward-Backward Counter. A PIPA loop may be mechanized to operate in either of two major modes; the ternary or 3-state mode and the binary mode. In the ternary mode, the PIP is torqued only in the presence of an acceleration input and when no input is present, the pendulum remains stationary at the null point. This mode is similar to the IRIG torquing loop in that it has 3 states, plus torque, minus torque and no torque applied. This mode of operation delivers 12 times the velocity resolution of the binary mode. In the Apollo program, the binary mode of operation has been chosen. In this mode, the pendulum is kept continually in motion because current is fed alternately to each torquer. This mode has poorer velocity resolution but can be capable of handling 12 times the maximum input acceleration of the ternary mode. In operation, the PIPA loop is able to handle inputs as high as ±19.1 g's.

The binary mode is further defined as a binary 3-3 mode. The 3-3 refers to the number of torque pulses applied during the pendulum oscillation. It is obvious that since the pendulum is kept constantly in motion, that motion about the pendulum null point must be an oscillatory one. Due to the natural frequency of the loop of approximately 500 cps, the pendulum will oscillate at a submultiple of 3.2 kc which is nearest that frequency. This is 533-1/3 cps and results in 3 pulses to the binary current switch for each side of the pendulum cycle, hence 3-3.

If each of these pulses were sent to the computer, it would mean that during this continuous operation, the computer would receive a constant train of incremental velocity data even though no velocity is being gained by the spacecraft. The purpose of forward-backward counter is to insure that the data sent to the AGC represents an actual gain in velocity and thereby avoid unnecessary processing by the AGC. The forward-backward counter is driven by the positive and negative pulses from the binary current switch. During operation of the PIPA loop with no acceleration input, the loop will operate at a rate of three positive pulses and then three negative pulses. The counter counts forward on the positive pulses and then

backward on the negative pulses. The counter continues this operation and generates no ΔV pulses to the AGC. However, with an acceleration input to the 16 PIP, the loop no longer operates on the 3:3 ratio and the counter exceeds its capacity and provides ΔV pulses to the AGC. Refer to Table 2-1 for a logic table of the forward-backward counter.

Assume the following initial logic value conditions of the complementing flip-flops as a starting point:

$$A = 0, \quad B = 1, \quad C = 0, \quad D = 1$$

If these conditions exist, then the B and D inputs to the #1 and gate are at a logic one and the next +V pulse will be anded with B and D, inverted, and sent to the computer as a $+\Delta V$ pulse. Since none of the flip-flops change state any sequential +V pulses will result in $+\Delta V$ pulses, on a one to one basis.

If at this time a train of negative velocity pulses is present at the counter input, the flip-flops change state for 3 pulses as shown in the truth table of Figure 1-35 to A = 1, B = 0, C = 1, D = 0. This presents a logic one at inputs A and C of and Gate #2, permitting any following sequential -V inputs to result in a $-\Delta V$ output.

The logic table also shows how during zero acceleration with the loop operating in the 3-3 mode, no ΔV pulses are sent to the computer.

To understand the forward-backward counter, it is only necessary to follow a train of pulses and chart the sequence of state changes of the complementing flip-flops. The function of the counter is to issue a ΔV pulse on the 4th and all successive pulses of a train of sequentially received velocity pulses of one direction. If the direction of acceleration reverses, it will require 3 more velocity pulses to clear the counter so that the succeeding pulses will cause a ΔV output of opposite direction.

3.6 SUMMARY

The inertial measurement unit is a three degree-of-freedom gyro stabilized device whose prime function is to maintain a stable member as an inertially referenced platform. This permits accurate use of the platform for attitude measurement in an orthogonal system as well as maintain acceleration sensors in this coordinate system for accurate measurement of spacecraft velocity changes.

Maintenance of the platform in the reference system as well as erection of the platform is accomplished with three stabilization loops. Each of three gimbals is controlled by its own components in a closed servo loop. Initial erection may be accomplished by external inputs to the loops from the computer and/or through the coupling display units which are linked to the IMU through resolver systems. Additional AGC inputs to the gyro torquing loop permit fine positioning of the gimbals.

Velocity changes are measured by the accelerometer loop. This loop contains a pulsed pendulum which is maintained in oscillation about its null point by an external torque signal. The closed servo loop maintaining the null condition supplies the necessary torque to reposition the pendulum whenever an acceleration tends to displace it. In addition, the loop sends pulses to the AGC to indicate the acceleration induced changes in velocity. These pulse quantities are directly proportional to the pendulum restoring torque pulses of the loop.

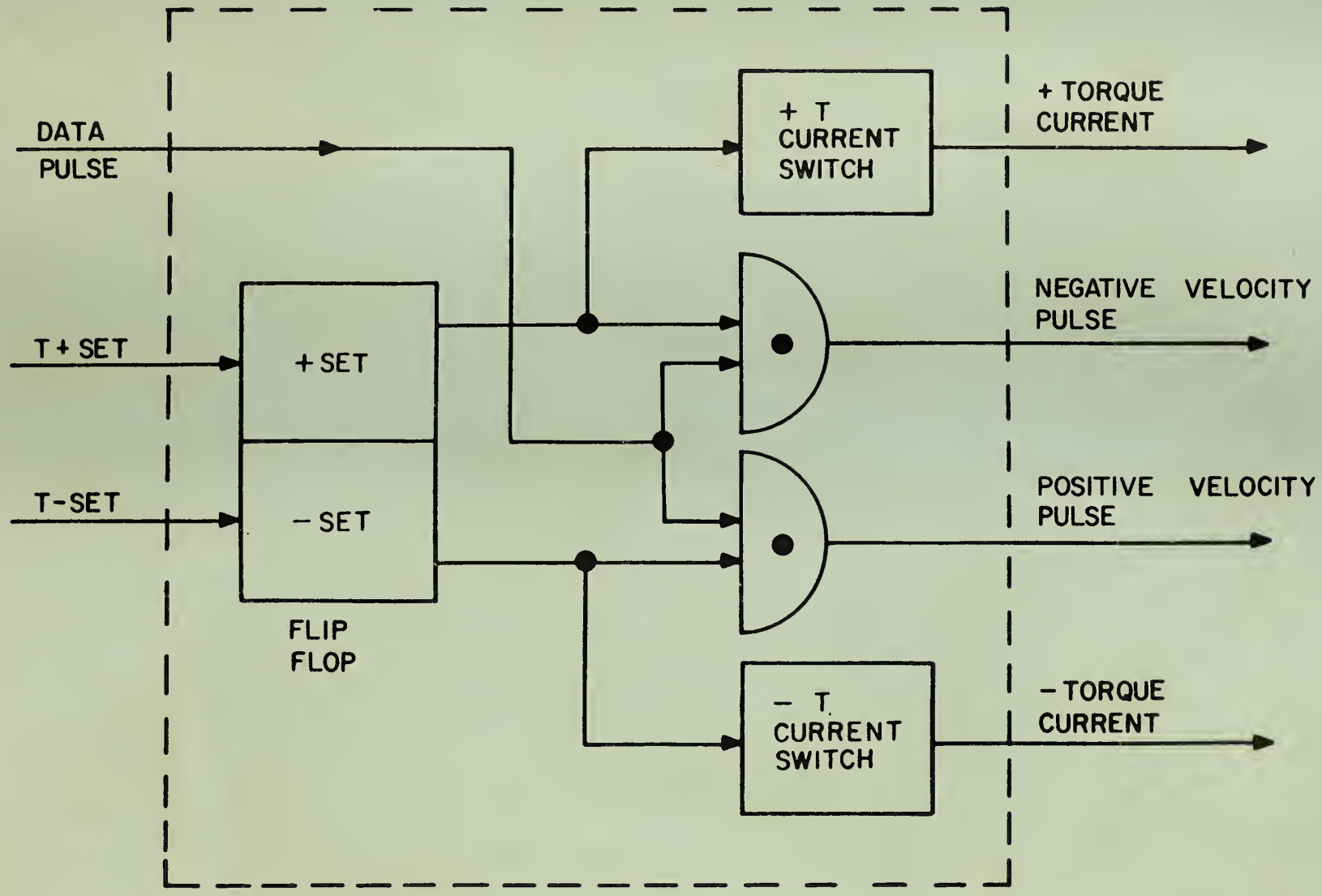


Figure 3-33. Binary Current Switch, Block Diagram

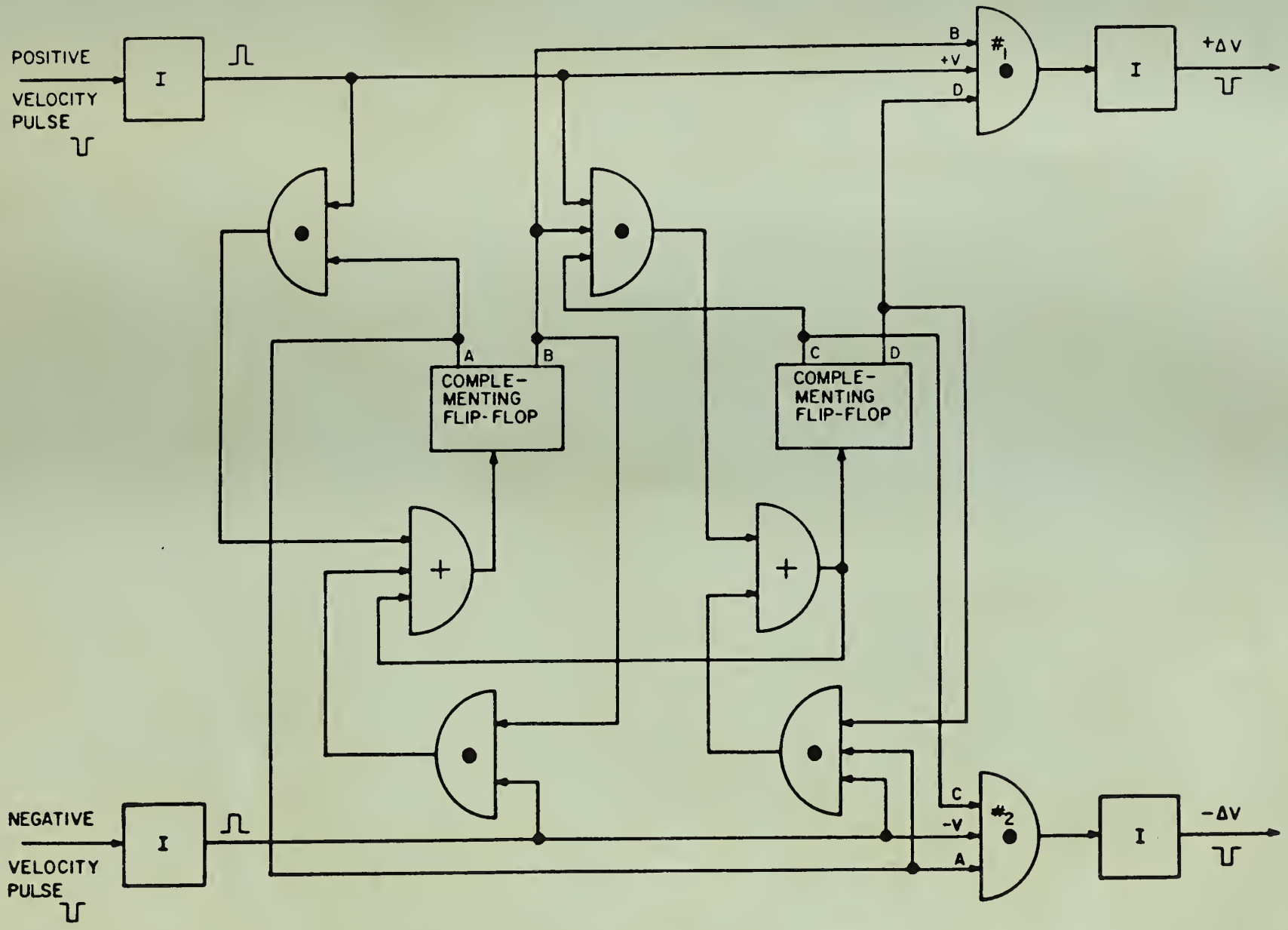


Figure 3-34. Forward-Backward Counter, Logic Diagram

Table 3-1. Logic Table, Forward-Backward Counter

CONDITION	FLIP-FLOP OUTPUTS				OUTPUT TO AGC	SYSTEM INPUTS
	A	B	C	D		
Initial Conditions	0	1	0	1	None	
First + V Input	0	1	0	1	ΔV Pulse Out	Positive Acceleration
Second + V Input	0	1	0	1	ΔV Pulse Out	
Third + V Input	0	1	0	1	ΔV Pulse Out	
First -V Input	1	0	0	1	None	*NOTE: Whenever the C-D outputs change state, it results in an additional state change for the A-B flip-flop.
Second -V Input	* 1	0	1	0		
	0	1				
Third -V Input	1	0	1	0		
First + V Input	0	1	1	0		
Second + V Input	* 0	1	0	1		
	1	0				
Third + V Input	0	1	0	1		
First -V Input	1	0	0	1		
Second -V Input	* 1	0	1	0		Zero Acceleration Operating in 3-3 Mode
	0	1				
Third -V Input	1	0	1	0		
First + V Input	0	1	1	0		
Second + V Input	* 0	1	0	1		
	1	0				
Third + V Input	0	1	0	1		
First -V Input	1	0	0	1		
Second -V Input	* 1	0	1	0		
	0	1				
Third -V Input	1	0	1	0		
First + V Input	0	1	1	0	None	
Second + V Input	* 0	1	0	1	None	
	1	0				
Third + V Input	0	1	0	1	None	
Fourth + V Input	0	1	0	1	ΔV Pulse Out	Positive Acceleration
Fifth + V Input	0	1	0	1	ΔV Pulse Out	
Nth Input	0	1	0	1	ΔV Pulse Out	

REVIEW QUESTIONS FOR SECTION III

1. The following statements are either True or False - indicate which.

T F a. The stable member contains nine inertial sensors.

T F b. The computer receives its ΔV signals from the PIPA loop through the forward-backward counter.

T F c. The ternary current switch supplies torque pulses to keep the PIP oscillating about its null point.

T F d. The IMU gyro error resolver is used to resolve Z and X IRIG outputs about the inner gimbal angle, to the middle and outer gimbal servos.

T F e. The ADA provides an input to the gimbal servo loop in order to extend the loop frequency response and transient handling capability.

2. Draw the inner gimbal servo loop block diagram and describe each block's function.

3. Describe the functional and pendulum construction differences between an ADA and a PIP.

4. Describe the stabilization amplifier inputs and outputs and the difference between the three in the stabilization loops.

5. Describe the purpose of the dummy current switch in the gyro torquing loop.

6. Define the purposes of the IRIG calibration circuit.

7. How is the PIP pendulum kept in oscillation when the PIPA loop is closed?

8. What is the purpose of the forward-backward counter and what should its output be during zero acceleration conditions?

SECTION IV

COUPLING DISPLAY UNIT

INTRODUCTION

In this section of the study guide, the Coupling Display Unit will be described, with emphasis on its operation and the hardware and circuitry associated with its operation. This section also develops and leads into the mechanization of the CDU within the G&N System as a coupling unit between the subsystem components.

4.1 COUPLING DISPLAY UNIT

Five CDU's are required by the G&N System. Three are in the inertial subsystem and two are in the optical subsystem. All five CDU's are physically similar. The three inertial CDU's are identical to each other and may be interchanged. Their operation is similar in both subsystems. They are located below the IMU control panel in the lower display and control area (figure 4-1). The CDU's couple the IMU and the optics to the AGC and they display IMU and optics angular data to the astronaut. The mechanization of the CDU presented in this section is applicable to the inertial subsystem only. Mechanization of the CDU in the optical subsystem is presented in Section X of this study guide.

The CDU outside dimensions are approximately six inches by four and three-fourths inches by one and three-fourths inches. The housing is beryllium. Internally, the mechanical portions of the CDU (figure 4-1a) consist of a combination motor-tachometer, four resolvers, a digital encoder, three display dials and a thumbwheel; all interconnected by a series of stainless steel gears and shafts. The display dials which are visible on the front of the unit provide a six digit readout. A slew switch and thumbwheel are accessible on the front of the unit. The five CDU's are attached to a beryllium frame which is mounted below the IMU control panel in contact with a spacecraft coldplate. An aluminum cover over the front of the group of five CDU's provides access to the controls and dials.

4.2 COUPLING DISPLAY UNIT OPERATION

The function of the CDU is to mechanize the equation $\sin(\theta - \Psi) \quad \sin\theta \cos\Psi - \cos\theta \sin\Psi$. Where θ is the angle of the IMU gimbal or optics and Ψ is the angle of the CDU shaft. A resolver set on the gimbal or optics generates a set of signals equal to 28 volts 800 cps times the sine and times the cosine of the angle (θ) described. This signal set is transmitted to a set of resolvers in the CDU which reflect the CDU shaft angle (Ψ). The CDU resolver takes the sine of θ multiplies it by the cosine of Ψ, and from this subtracts the cos of θ which it has multiplied by the sine of Ψ. This operation can be observed in figure 4-2, where the output of the CDU resolver ($\sin[\theta - \Psi]$) is used to position the CDU shaft until the error $\theta - \Psi$ is equal to zero. At this time the CDU shaft accurately reflects the position of the transmitter resolver.

The CDU is driven either by the thumbwheel or electric motor excited by the output of the motor drive amplifier. The tachometer provides negative electrical feedback, proportional to the shaft speed, to the motor drive amplifier. The slew switch provides an input to the motor drive amplifier to position the CDU when the CDU's are used in the inertial subsystem. The four resolvers are utilized in the ISS for angular data transmission or angular error resolution. The specific resolvers utilized and their functions depend on the mechanization of the subsystem. The digital encoder (figure 4-3) converts the angular motion of the CDU resolvers into a digital signal which can be used by the AGC after being processed by the encoder electronics.

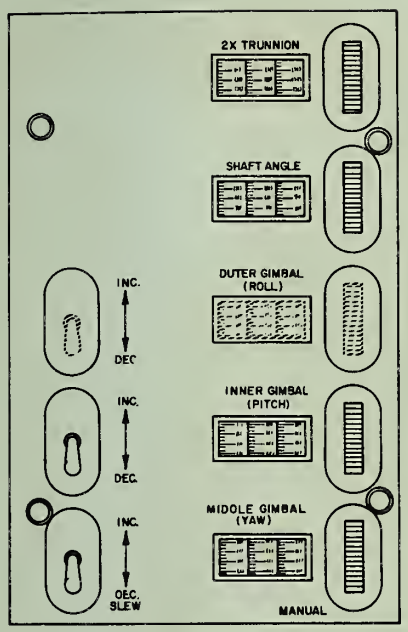


Figure 4-1. Coupling Display Panel

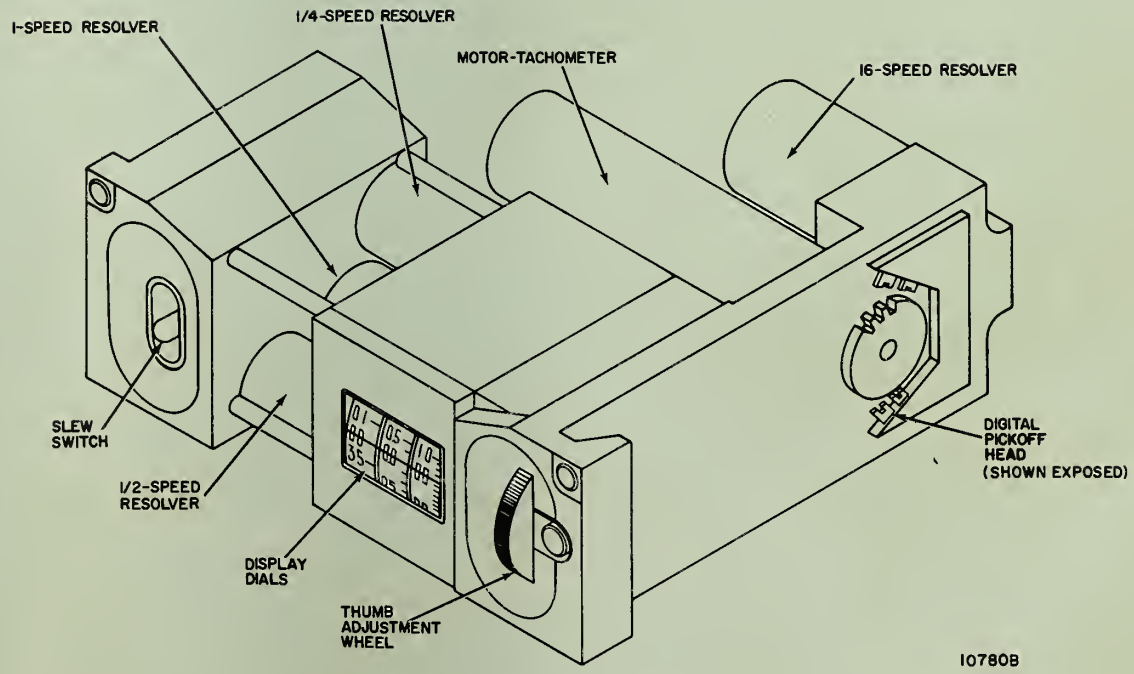


Figure 4-1a. Coupling Display Unit

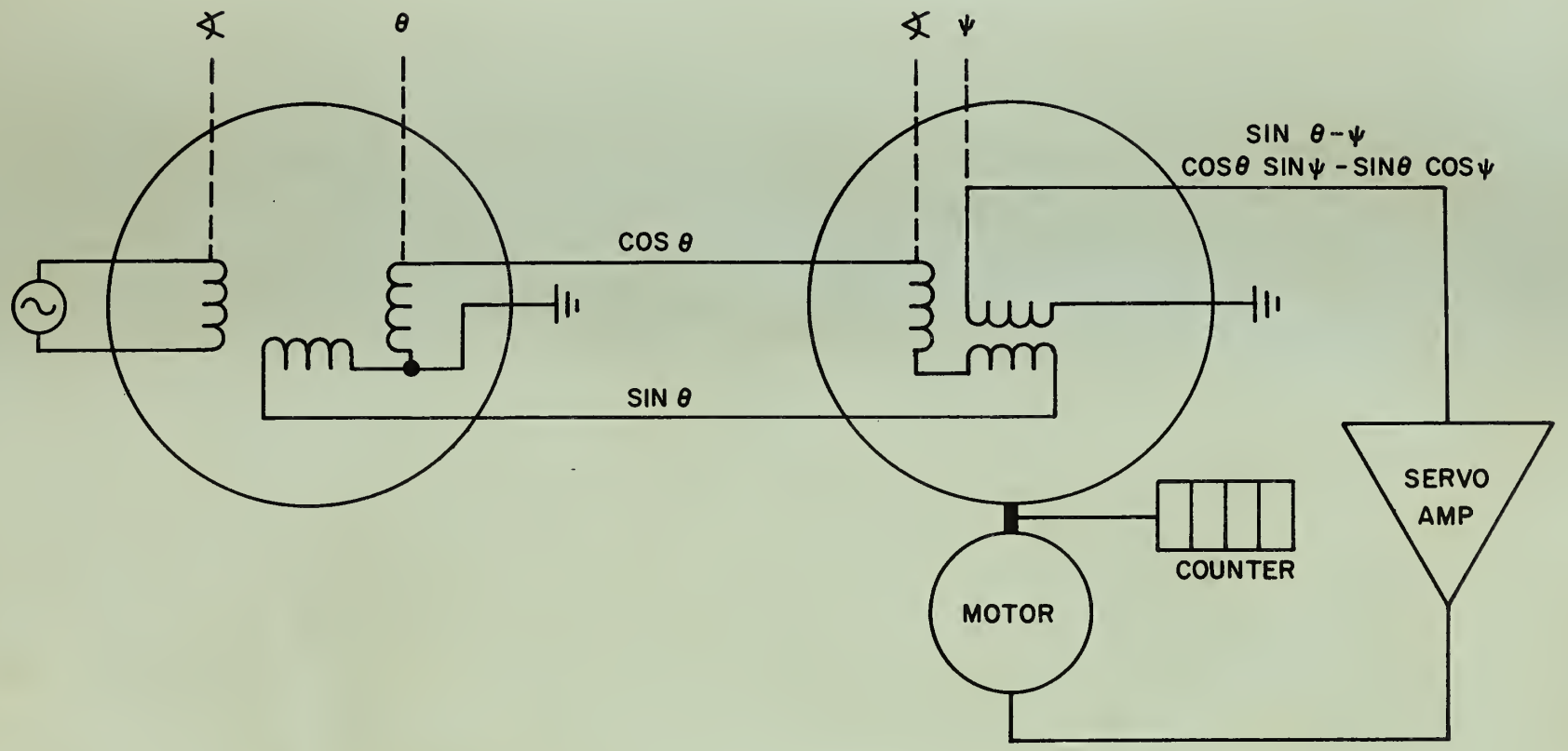


Figure 4-2. Resolver Gimbal Angle Indicator Servo

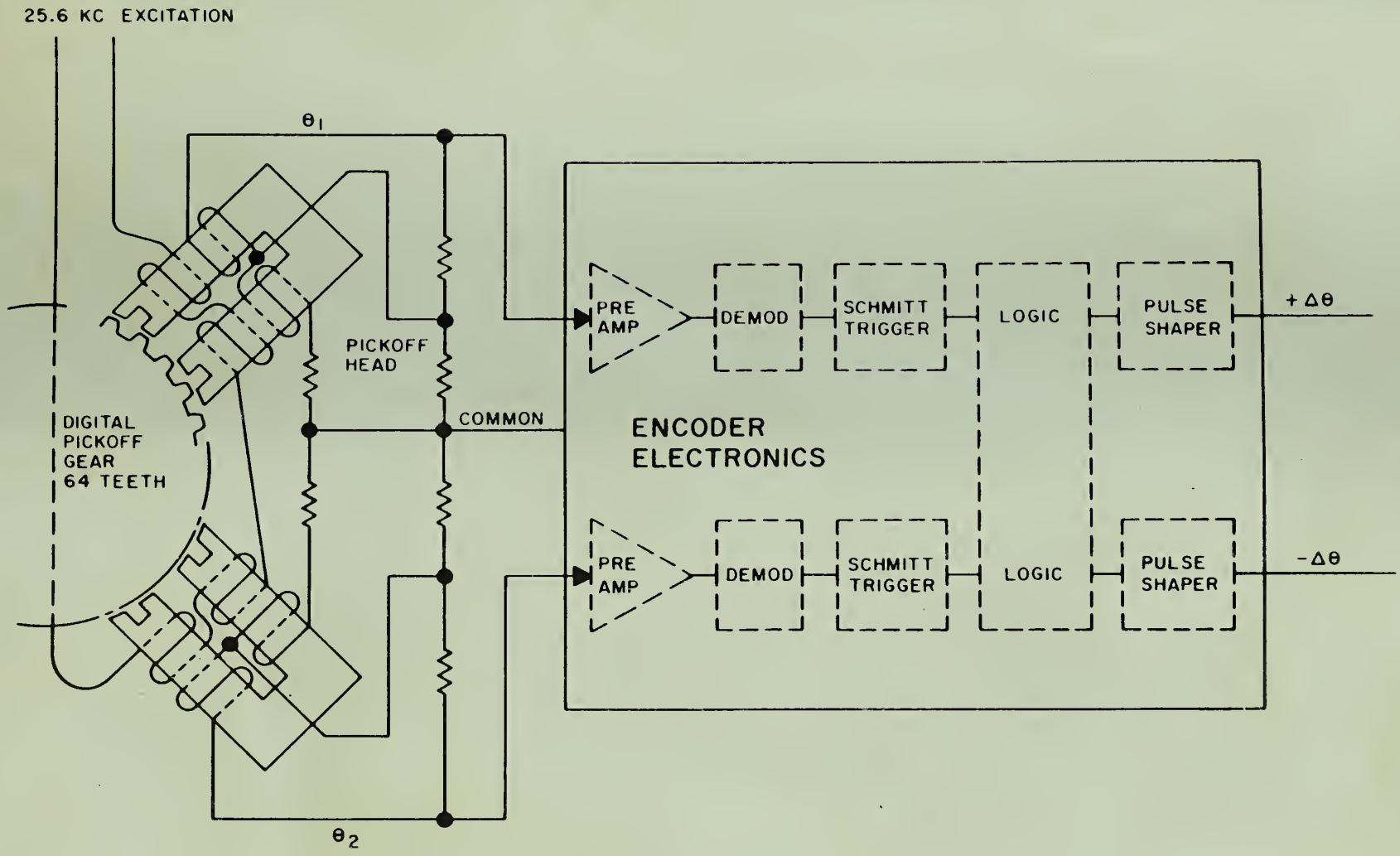


Figure 4-3. CDU Digital Encoder

4.2.1 DIGITAL ENCODER. The digital encoder consists of a digital pickoff gear, two U-shaped digital pickoff heads, and the encoder electronics. The pickoff heads have primary and secondary coils wound on each of the two legs. The primary coil is excited with 25.6 kilocycles. The secondary coils are connected in opposition. When the movable armature (pickoff gear) is symmetrically located between each of the two legs, the flux in each of the two legs is the same. Since the secondaries are wound in opposition, no output voltage results. This position of the gear is referred to as the null position. If the armature is displaced from the null position, a greater voltage is induced in one of the coils. Motion of the gear tooth in the opposition direction similarly produces a greater output voltage in the other coil. The output voltage varies sinusoidally with the displacement of the gear teeth. Thus, this device modulates the excitation at a frequency proportional to the velocity of the armature. The second pickoff head is located so that its output voltage will be displaced from the first output voltage by 90 degrees. The relative phasing between the two outputs indicates the direction of shaft movement.

4.2.2 ENCODER ELECTRONICS. Encoder outputs are routed through preamplifiers in the digital encoder electronics. The preamplifier outputs are routed to Schmitt triggers via synchronous demodulators. The outputs of the demodulators are converted into square waves by the Schmitt trigger. The square wave outputs are then routed into a logic network which identifies the direction of rotation and produces voltage spikes on one output line ($+\Delta\phi$) for clockwise rotation of shaft and on the other output line ($-\Delta\phi$) for counter-clockwise rotation. These spikes are then converted to the proper logic level for the AGC by pulse shaping networks. Each pulse presented to the AGC represents a finite number of arc-seconds of shaft travel. The number depends on the subsystem in which the CDU is being used. For the ISS, the encoder output or scale factor is one pulse for 39.6 arc seconds of gimbal rotation. The logic of the encoder electronics provides two distinct encoder modes of operation; either one pulse per gear tooth or two pulses per gear tooth. Again, the mode of operation depends on subsystem mechanization.

4.2.3 DIGITAL TO ANALOG CONVERTER. While the digital encoder is providing the AGC with information about the position of the CDU, the AGC must also be provided with a means of controlling the movement of the CDU. This is accomplished by the digital to analog converter (DAC). The DAC receives digital commands from the AGC and converts these commands to an electrical analog output usable in the motor drive amplifier. A block diagram of the DAC is shown in figure 4-4. The inputs from the AGC are pulses of approximately three microseconds duration with a repetition rate of 3.200 pps. These pulses are not applied continuously, but are supplied in bursts from the AGC. The feedback signal from the encoder also consists of pulses, but the repetition rate varies according to the speed of encoder pickoff gear rotation. AGC $\Delta\theta$ inputs cause a capacitor in the DAC to be charged in one direction or the other as determined by the AGC. The charge is stored in this capacitor until the CDU is driven at which time CDU $\Delta\theta$ pulses from the encoder are used to remove the charge on the capacitor. The charge on the capacitor is monitored by an integrated chopper stage having two silicon controlled switches. These switches which are chopping at a referenced 800 cycles frequency provide an in-phase or out-of-phase 800 cycle square wave to the capacitor input of a Darlington amplifier to drive the CDU motor. The low impedance Darlington amplifier has a maximum output of approximately 10 volts peak to peak. The requirement of negative feedback $\Delta\theta$ pulses from the CDU assures a defined CDU movement per AGC $\Delta\theta$ pulse, permitting digital control of an analog servomechanism.

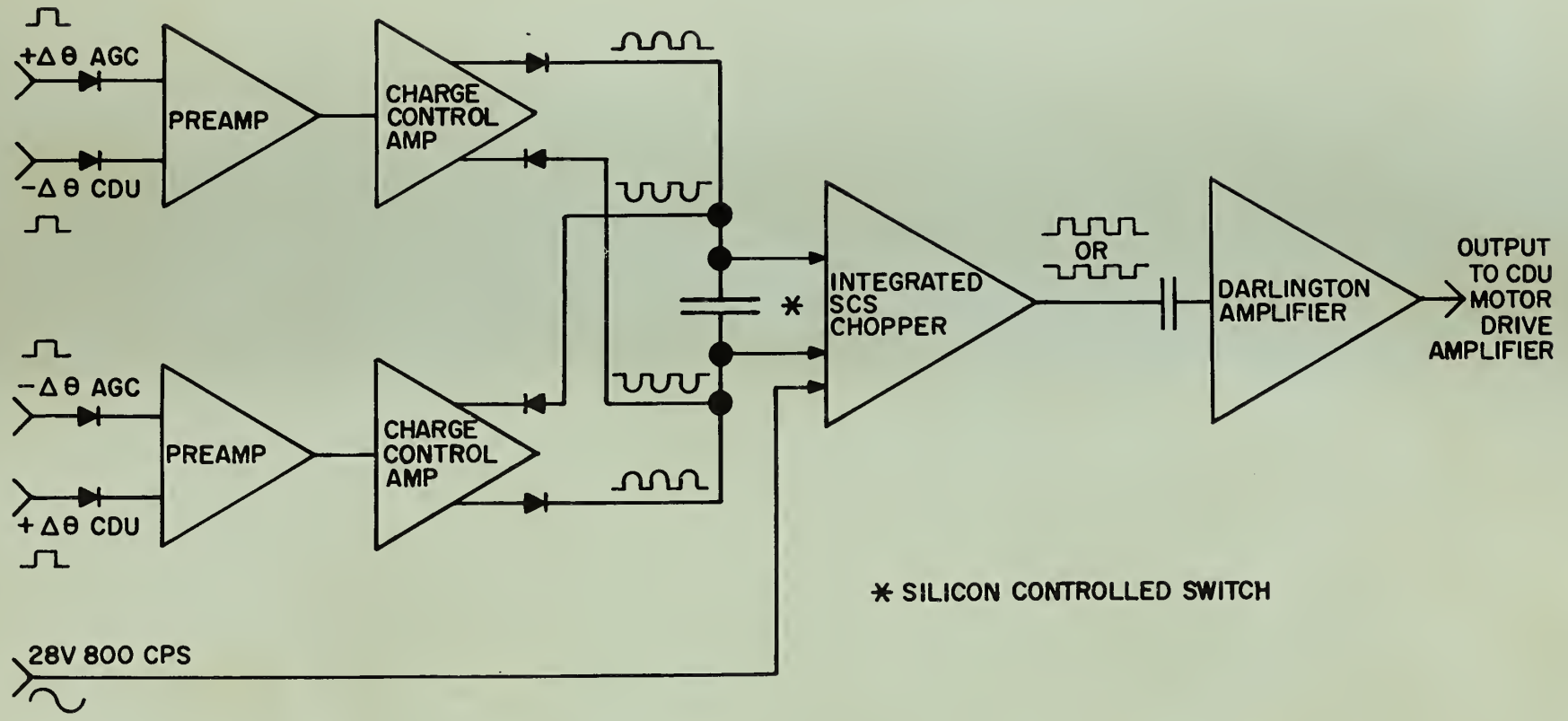


Figure 4-4. Digital to Analog Converter

4.3 CDU MECHANIZATION FOR INERTIAL SUBSYSTEM

The mechanization of the CDU for the inertial subsystem is shown in Figure 3-5. In this mechanization, the sixteen-speed (16X) and the single-speed (1X) resolvers of the CDU function as receivers and the 16X and 1X resolvers mounted on the IMU in the inter-gimbal assemblies serve as transmitters. The one-half speed (1/2X) resolver is used only to zero the CDU. The outputs of these three resolvers provide inputs to the selector circuit. The 1X resolver also provides an input to the coarse align amplifier and the spacecraft attitude control loop, depending on the mode of operation. It should be also noted that the output of the IMU outer gimbal 1X resolver is routed to the outer gimbal CDU 16X resolver and that the output of the CDU 16X resolver is routed to the stabilization control system during the entry mode. A description of the various modes of operation and the function and utilization of the relays shown in figure 4-5 is explained in Section V. The selector circuit consists of three pairs of diodes; one pair is in the output of each of the three CDU resolvers utilized with the IMU. The diodes in the 1X resolver and 1/2X resolver circuits are selected so that the input to the motor drive amplifier is cut off when the voltage drops below a certain level. The diodes in the 16X resolver circuit are selected so that the resolver output is limited at a certain level. This combination of diodes determines which of the resolvers supplies the control of the IMU-CDU loop in the zero encoder and fine align modes.

The motor drive amplifier can also receive inputs from the slew switch or the DAC along with a feedback signal from the tachometer. The inputs to the motor drive amplifier are first amplified and then, through the use of two integrated choppers, the input quadrature voltage is rejected. This signal is again amplified to provide an output to drive the CDU motor. The encoder electronics, as used in the inertial subsystem mechanization, generates one pulse per gear tooth. Each pulse represents approximately 40 arc-seconds of motion of the 1X CDU resolver. The maximum repetition rate for $\Delta\theta$ pulses from the encoder is approximately 2,200 pps. Malfunctions in the CDU loop are identified by the CDU fail indicator. A signal denoting the malfunction is transmitted to the AGC and the failure detection circuitry.

4.4 SUMMARY

The inertial subsystem uses three CDU's as coupling and display devices for the three IMU gimbals. The CDU permits: (1) measurement of gimbal angles and transmission of this data to the computer and/or visual readout, (2) coarse align positioning signals to drive the individual gimbal as commanded by the computer or the operator, and (3) generation of attitude error signals to drive the spacecraft R. C. S. system during G & N control of spacecraft attitude.

The digital encoder converts the analog CDU shaft position data into digital pulses for use in the computer and DAC. The DAC (Digital to Analog Converter) converts AGC drive commands to the CDU into analog voltages for acceptance by the motor drive amplifier of the CDU.

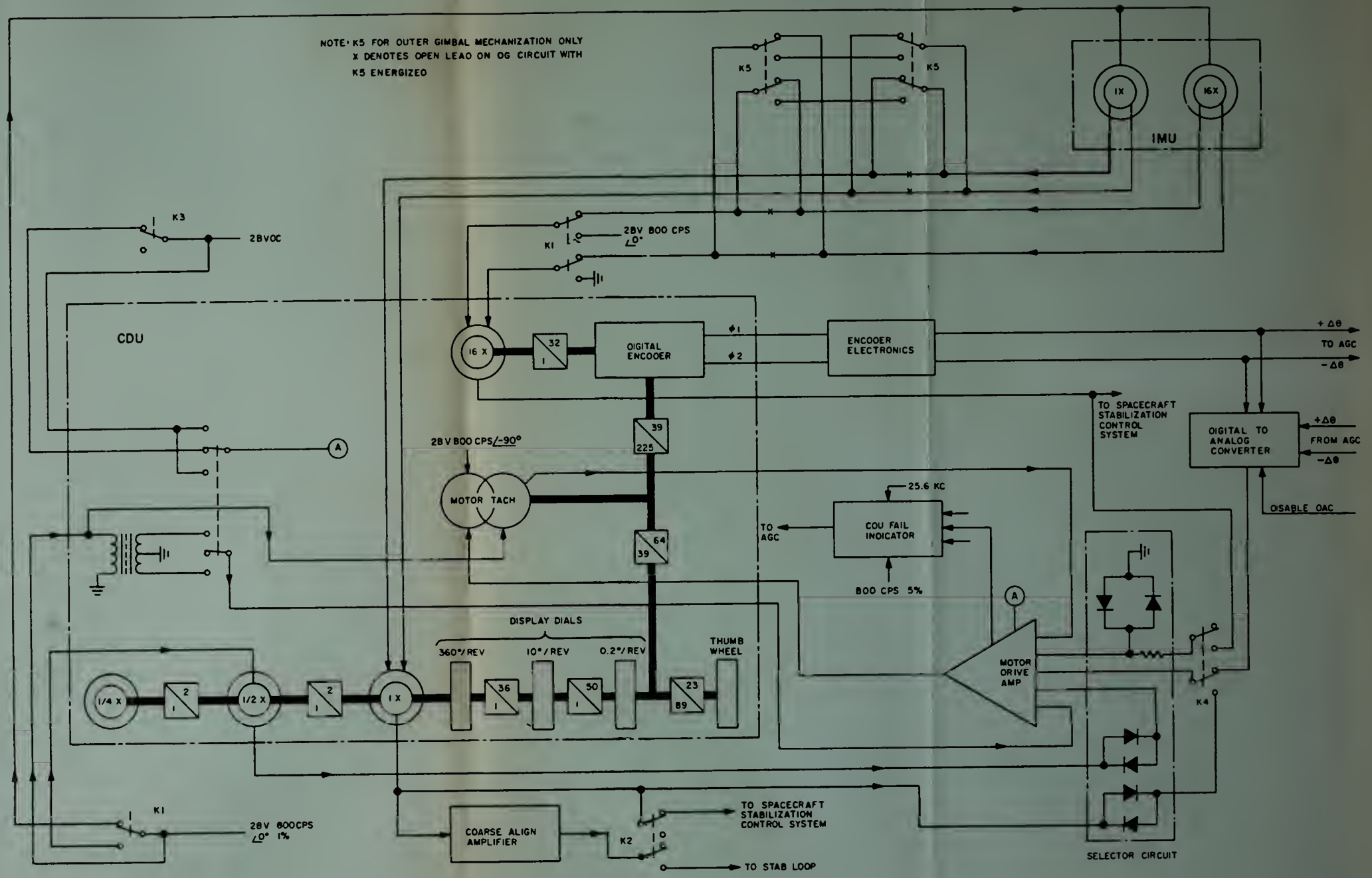


Figure 4-5. CDU Functional Diagram

REVIEW QUESTIONS FOR SECTION IV

1. Describe three possible ways of driving the CDU shaft.

2. Explain three functions of the inertial CDU.

3. Why are the DAC and encoder required in the CDU mechanization?

SECTION V

ISS MODES OF OPERATION

INTRODUCTION

This section describes the six modes of the inertial subsystem, their mechanization and methods by which they are commanded. In addition, mode capabilities and input/output relationships will be explained in detail, as well as ISS turn-on requirements.

5.1 MODES OF OPERATION

The inertial subsystem has six major modes of operation as initiated by the matrix of six mode pushbuttons located on the IMU control panel or by the AGC. The modes are: zero encoder, coarse align, manual CDU, fine align, attitude control, and entry. Two additional switches are provided, a pushbutton for initiating manual align and a transfer switch for selecting either manual or computer control.

5.2 MODE CONTROL

The mechanization of the inertial subsystem mode switching is shown in the appendix. The relays, diodes and 100-second timer are packaged in the display and control electronics. The method of controlling the mode switching circuits depends upon the setting of the transfer switch to the manual or computer position. Relays K1 through K13 constitute the mode controlling relays. These are located in the PSA and D & C electronics. K13 is a bistable relay used in the entry mode. This prevents possible unlatching during the critical reentry phase due to possible power supply transients. All other relays are latched electrically. Complete relay mechanization charts and loop flow diagrams may be found in the appendix to this study guide; however, this section will treat the modes of operation without going into relay and switch configurations.

5.3 ISS PREMODING CONDITIONS

The ISS-IMU is generally kept in a standby condition when not in use. When use of the system is called for, it is turned on and goes through a turn-on sequence prior to entering the desired mode of operation.

5.3.1 STANDBY. During this mode, 28 volt DC prime and 3200 cps sine and square wave power are applied only to the temperature control circuits and the gyro and accelerometer ducosyns to maintain magnetic suspension. All the inertial subsystem mode switching relays are deenergized with K13 being in either the set or reset condition (depending upon the system mode of operation when the power was previously removed). Prior to use, the IMU must have been in the standby condition or on for at least two hours. By storage of the ISS with the Y PIP input axis vertical, the requirement for a two-hour standby condition can be reduced to three minutes. This permits the IMU temperature to stabilize and allows the suspensions of the inertial instruments to settle out. At least three cycles of suspension oscillation are required to settle out the PIP floats and the period of each cycle is about 1/2 hour.

5.3.2 IMU TURN-ON. Upon switching the inertial subsystem to the operate mode (standby operate switch on main D & C panel) prime power is applied to all the subsystem power supplies. A 100 second time delay starts its timing cycle and the IMU delay lamp on the lower D & C is on. The system immediately enters the coarse align mode. This will drive the IMU gimbals to the CDU angles while the gyro wheels are coming up to speed. After 100 seconds, the IMU delay lamp goes out and the system will leave the coarse align mode. It will then automatically enter either the entry or attitude control mode. The mode is selected according to the condition of the entry relay K13. If the previous mode of operation was the entry mode, then K13 will have been left in the set condition and the system will select the entry mode. If the system had been in any other mode, it will automatically go into attitude control. This condition continues until a mode is selected.

5.4 MODE MECHANIZATION

5.4.1 ZERO ENCODER. The purpose of this mode is to drive the CDU shaft angle to a zero position utilizing the CDU 16X and 1/2X resolvers. AGC CDU registers are cleared and encoder outputs indicative of CDU shaft angle changes are thereafter referenced to the zero position for use by the AGC, essentially referencing the computer and CDU to each other. The zero encoder mode is manually selected by pressing S5 (zero encoder) on the IMU control. If the system is in manual control, has been on for 100 seconds minimum and zero encoder is initiated, the following occurs: (1) the zero encoder lamp lights, and (2) a signal is provided to disable the digital to analog converter since it will be receiving pulses and could provide an input to the CDU motor drive amplifier.

In the CDU zero encoder loop (figure 5-1), an 800 cps reference voltage is applied to the stators of the 16X and 1/2X CDU resolvers. The sine windings of the resolvers are applied through a limiter circuit or two speed switch to the motor drive amplifier inputs. The motor drive amplifier output signal is applied to the CDU servo motor which repositions the CDU shaft until the shaft is at the zero angle. At this time the sine of the angle is zero and the resolver outputs are zero. The maximum time for CDU zeroing is approximately 30 seconds.

5.4.2 COARSE ALIGN. The purpose of this mode is to slave the IMU gimbals to an angular position as determined by the CDU. The mode is entered by one of four means: (1) pressing the coarse align pushbutton with the inertial subsystem in manual control, (2) AGC command of coarse align mode with the system in computer control, (3) IMU turned on for less than 100 seconds, and (4) system in manual CDU mode and the manual align button pressed. The coarse align light will come on except in the case of condition (4) when the basic mode is CDU manual.

The basic coarse align loop is shown in figure 5-2. The gimbal 1X resolver is excited with an 800 cps reference and the rotor sine and cosine windings are connected to the CDU 1X resolver rotor. When the two rotor angles differ, an error signal proportional to the sine of the difference is generated by the CDU resolver. The signal is sent to the IMU-CDU difference meter and also to the coarse align amplifier where it is amplified and demodulated. The demodulated signal is sent to the gimbal servo amplifier which drives the IMU gimbal until the error between the IMU gimbal resolver and CDU shaft resolver is driven out.

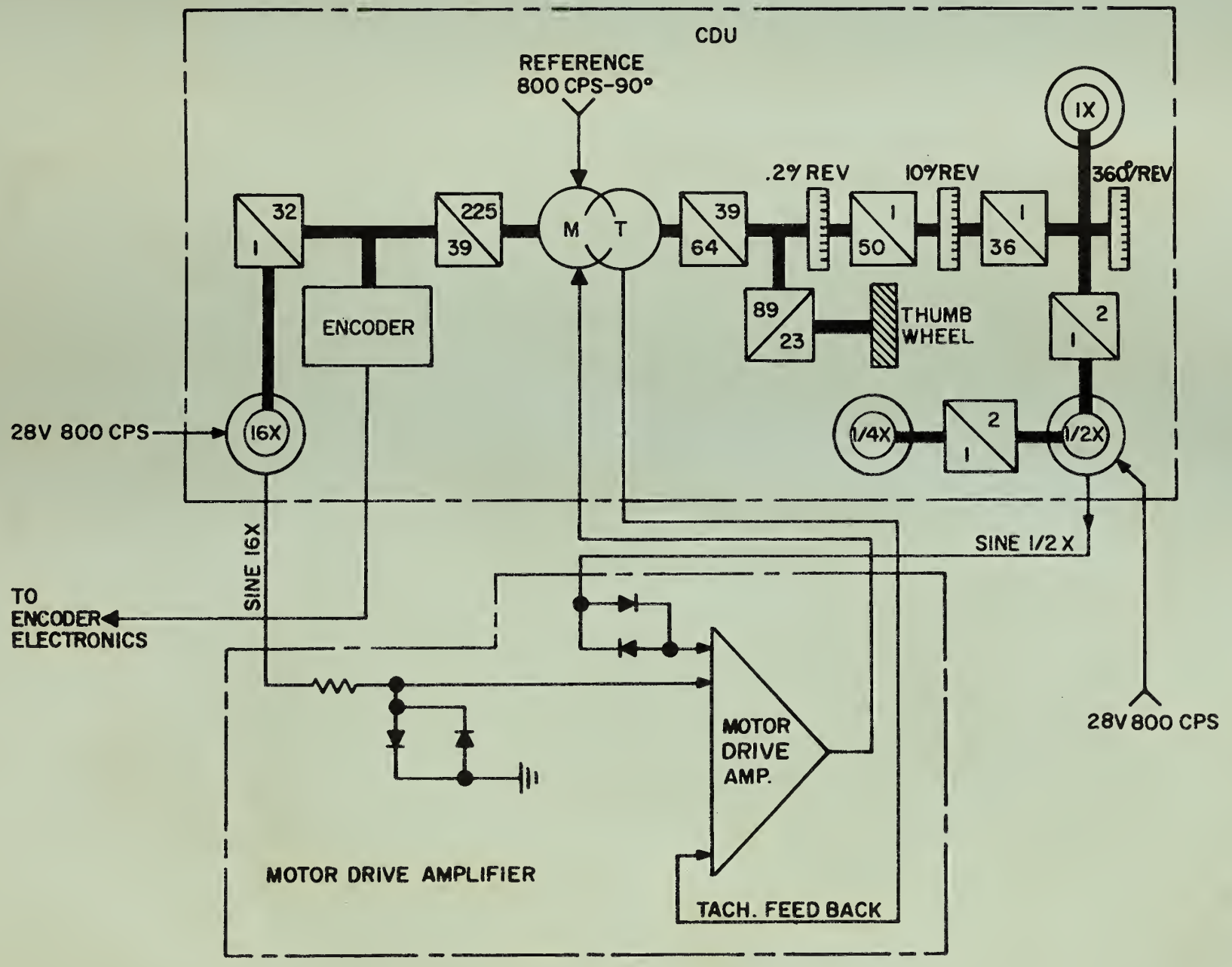


Figure 5-1. Zero Encoder Mode Mechanization

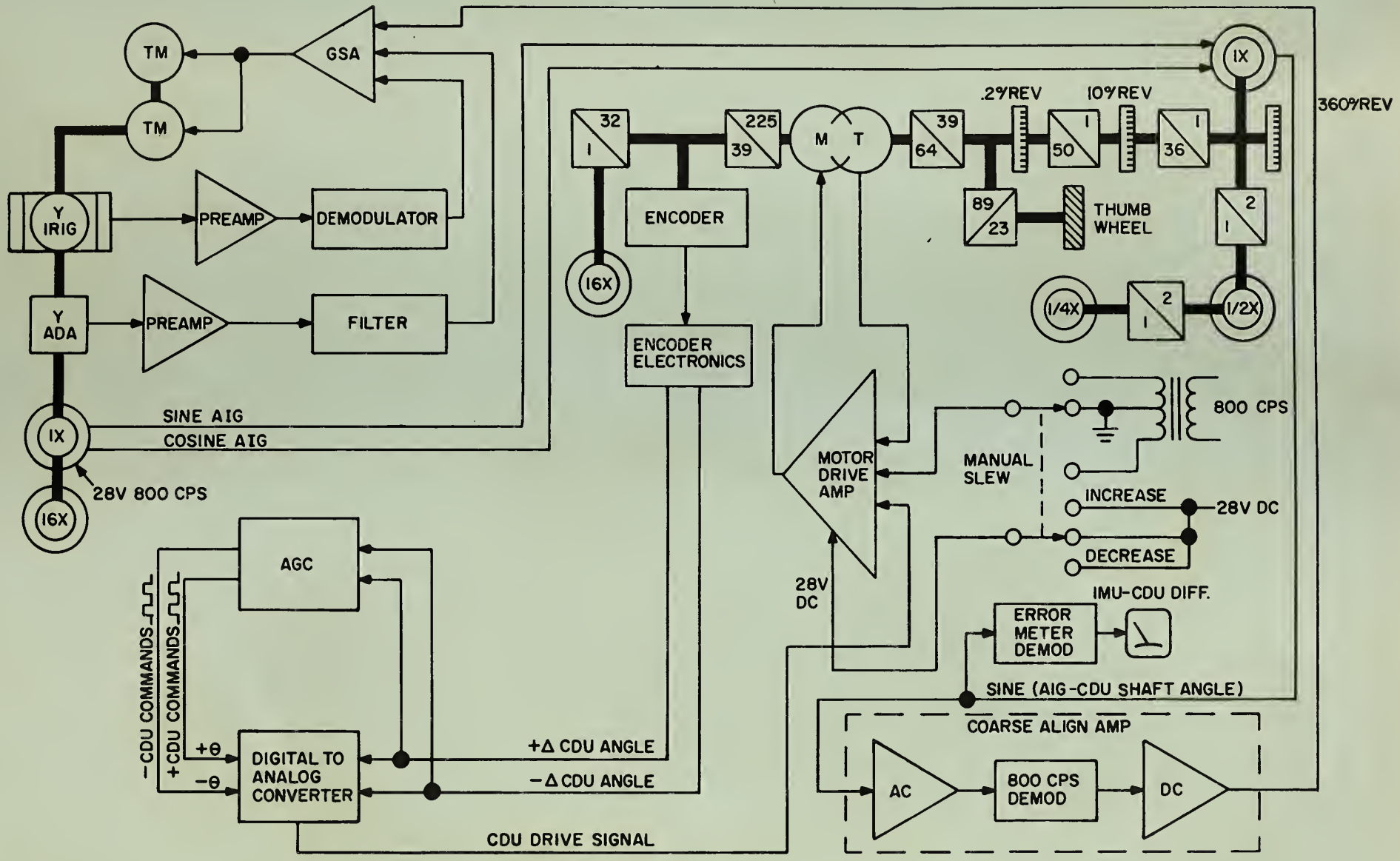


Figure 5-2. Coarse Align Mechanization (Inner Gimbal)

Positioning of the CDU's is performed by the AGC's pulsing the digital to analog converter. When the AGC is used to position the IMU gimbals, a 3,200 pps signal is applied to the digital to analog converter for a 1/12 second interval. The three digital to analog converters receive pulses sequentially, requiring 1/4 second to supply all the digital to analog converters with an input. The cycle is repeated until the required number of pulses have been issued by the AGC. For a small angle of shaft rotation, the digital to analog converter provides an 800 cps output proportional in amplitude to the number of pulses received. The output goes to the motor drive amplifier and drives the CDU shaft. The CDU encoder electronics provides pulses to the AGC and digital to analog converter. The pulses are generated by shaft rotation (approximately 2,200 pps max.). Each pulse is equal to approximately 40 arc seconds of rotation of the one speed resolver. Theoretically, one pulse out of the AGC to the digital to analog converter should cause the encoder to generate one pulse of feedback to the AGC and digital to analog converter. The pulse input from the AGC to the digital to analog converter and the feedback from the encoder should cancel each other when CDU shaft angle equals the AGC commanded angle.

5.4.3 MANUAL CDU. The manual CDU mode is used as a backup mode to provide the coarse align capability in the event of an AGC malfunction, since the CDU is positioned only by the AGC in the coarse align mode. For this mode, three methods of entry are possible:

1. Pressing the "manual CDU" pushbutton with the transfer switch in "manual".

2. By AGC command with the transfer switch in "computer".

3. By turning on the G & N sync switch on the main D & C panel during the attitude control mode. The G & N sync switch initiated manual CDU mode is used to lock the CDU's and hold the spacecraft in the previous attitude reference position obtained by pilot manipulation of the rotational hand controller.

The manual CDU mode loop is shown in figure 5-3. Note that the CDU is slewed to the desired shaft angle by the manual slew switch located on the CDU. When the manual align pushbutton is depressed, Relay K2 energizes and drives the IMU gimbals to the CDU shaft angle. At this time, the DAC is disabled.

5.4.4 FINE ALIGN. The purpose of this mode is to bring the stable member to fine alignment by AGC pulsing of the stabilization gyro torque ducosyns and to provide a stable reference from which the computer can track spacecraft attitude movements. The CDU's at this time are slaved to the IMU and will drive to the IMU gimbal angles. The number of pulses required to fine align the stable member are calculated by the AGC based upon optical measurements. The mode may be selected in a similar manner as the previous mode, by manual operation, computer control, and also by the G & N switch, provided SCS relay K1 is energized. The DAC is not at this time presenting an input to the motor drive amplifier.

The fine align mode (see figure 5-4) performs two tasks: (1) the gyro floats are torqued so the stabilization loops reposition the stable member, (2) the CDU's are driven to repeat the IMU gimbal angles. The torquing is accomplished by the AGC plus and minus torquing pulses at a rate of 3,200 pps applied to the ternary current switch.

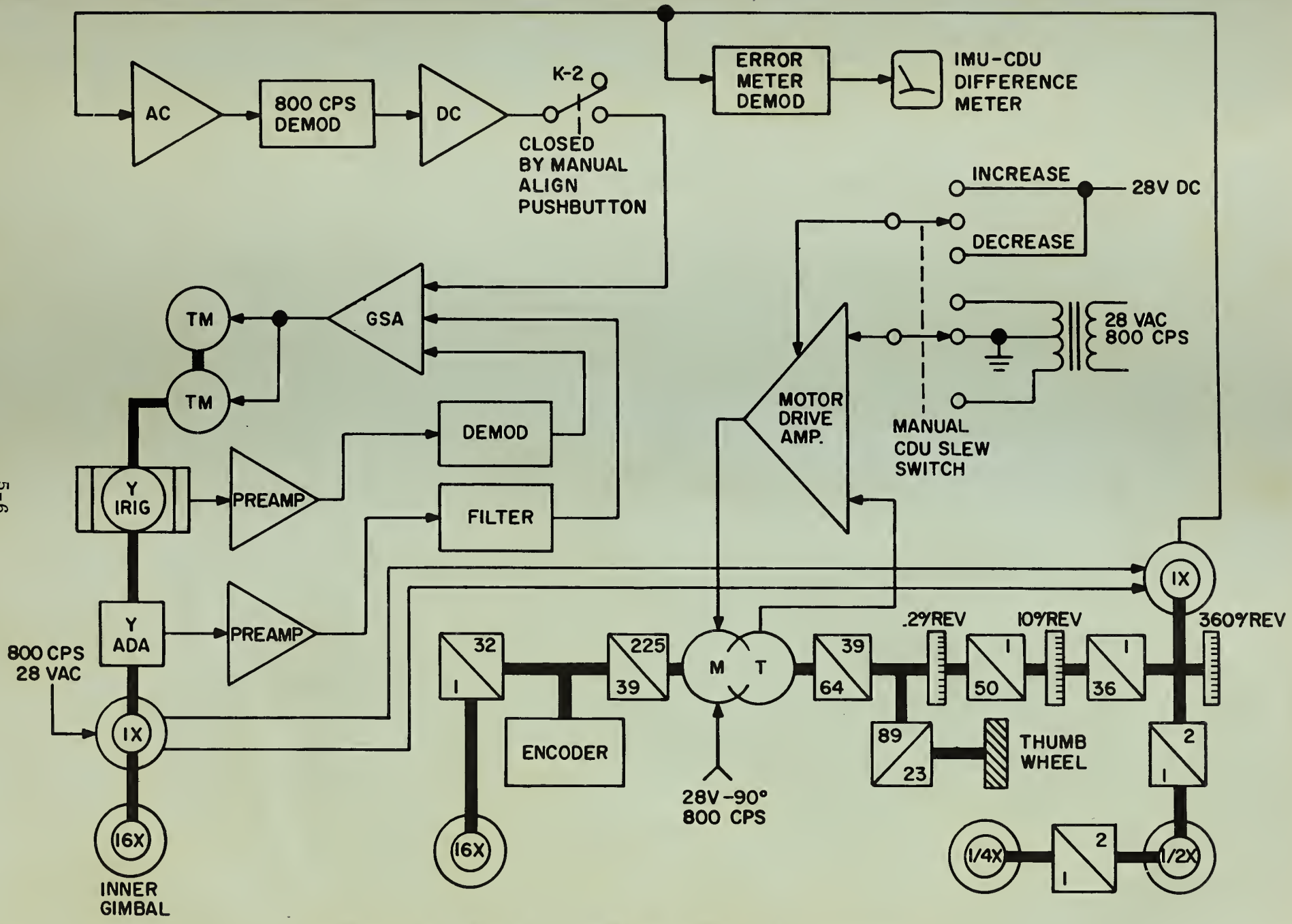


Figure 5-3. Manual CDU Mode Mechanization (Inner Gimbal)

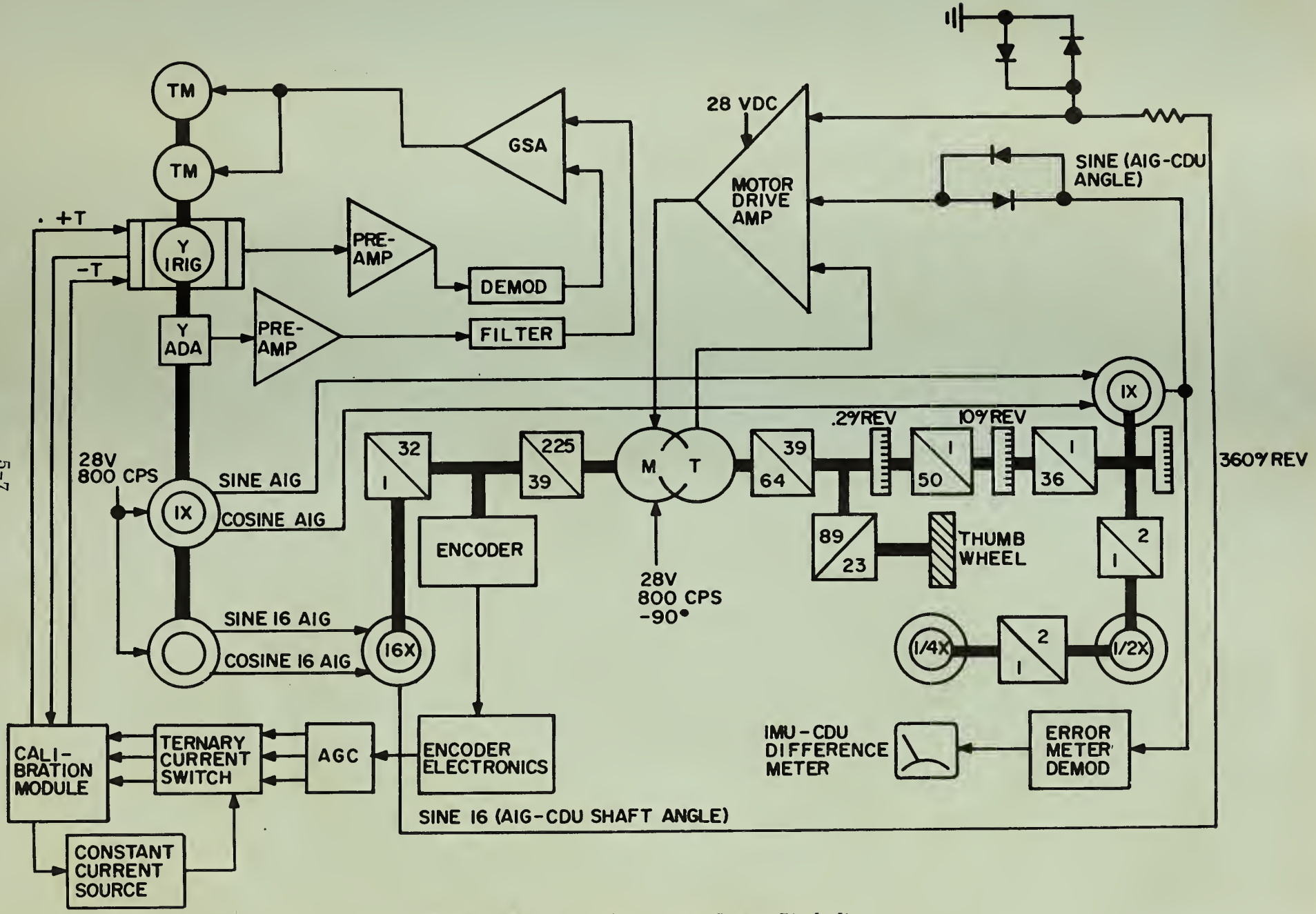


Figure 5-4. Fine Align Loop (Inner Gimbal)

The ternary current switch output pulses displace the stabilization gyro float from a null, and generate error signals in the stabilization loop. Details on the operation of the ternary current switch and calibration module are explained in Section II. The error signal in the stabilization loop causes the torque motors to drive the gimbals to position the stable member. Details of the operation of the stabilization loop also are explained in Section II. The CDU's follow the gimbal angles. The angular difference between the IMU and CDU 1X and 16X resolvers generates a CDU resolver rotor error signal proportional to the sine of the angular difference. The signal is sent to the motor drive amplifier. The motor drive amplifier output excites the control winding of the CDU drive motor and drives the CDU shaft until the IMU and CDU angles are equal. Upon completion of the mode, the stable member is fine aligned to a reference coordinate system and the CDU readouts indicate the gimbal angles.

When the G & N sync switch is on and the SCS relay is energized, the system will also be in fine align. Two conditions are required to energize the SCS relay. First, the SCS must be in the G & N attitude control mode. Second, the astronaut must be using the rotational hand controller to control the spacecraft. Thus, when a new attitude is established, the CDU's having been slaved to the gimbals will have the capability of providing the reference for holding the spacecraft at its new orientation.

5.4.5 ATTITUDE CONTROL. In this mode, velocity steering or attitude control signals are generated so that the IMU gimbal angles and CDU shaft angles remain equal to each other. Any movement of the spacecraft causing a change of gimbal positions about the stable platform will result in an error output from the CDU 1X resolver, which can be applied to the SCS for spacecraft corrective rotational thrusting.

In the attitude control mode (see figure 5-5) all the mode relays except K12 and K6 are deenergized. The error signal which is used for attitude control and velocity steering is generated by the 1X CDU receiving resolver and is sent to the stabilization and control system through the pitch-yaw resolver, and fixed resolution transformer. The error signal results from the difference between the angular position of the IMU and CDU 1X resolvers. While in the attitude control mode, the CDU resolver can be positioned automatically by the AGC as described in the coarse align mode. If velocity steering is being performed, the AGC drives the CDU's to control the direction of the thrust vector and the CDU error signal is used to position the service propulsion engine.

The stable member is held fixed with respect to inertial space by the stabilization loop. In essence, the spacecraft rotates about the stable member. A signal from the gimbal transmitter resolvers (A_{ig}, A_{mg}, A_{og}) indicates any change in the orientation of the spacecraft with respect to an inertial frame defined by the stable member axes. The desired gimbal angles are set into the inner, middle and outer gimbal CDU's and are designated θ_C, Ψ_C, $\emptyset_C$, respectively. When the CDU angles and IMU angles are not equal, error signals E_{ig}, E_{mg}, E_{og}, are generated. Before these error signals can be supplied to the stabilization and control system to reorient the spacecraft, two resolutions are completed. The resolutions are required since the axes about which the spacecraft rolls, pitches and yaws are not parallel to the gimbal axes. In fact, there are four sets of axes. Each set of axes must be considered to fully appreciate the resolution of the error signals. Once the error signals are resolved into spacecraft axes and supplied to the reaction control jets on the service module or SPS engine gimbals, the motion of the spacecraft is resolved back into gimbal axes by kinematics, thus completing the attitude control loop. Figure 5-6 shows the signals described and the necessary transformations. In the attitude control mode, the relays in the SCS are in a configuration to accept the resolved X, Y and Z error outputs EZ_{body}, EY_{body} and EX_{body}.

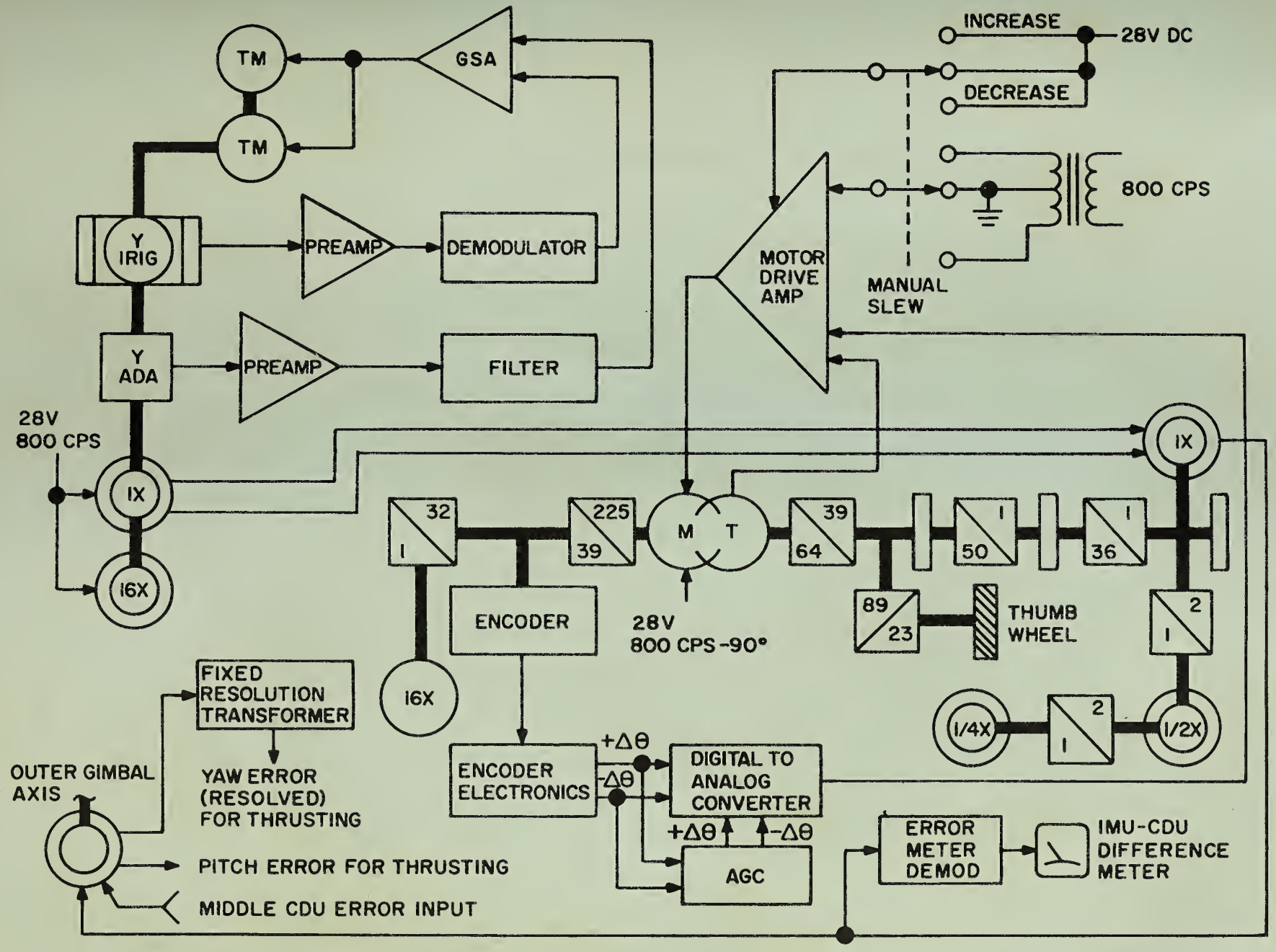


Figure 5-5. Attitude Control Mode Mechanization (Inner Gimbal)

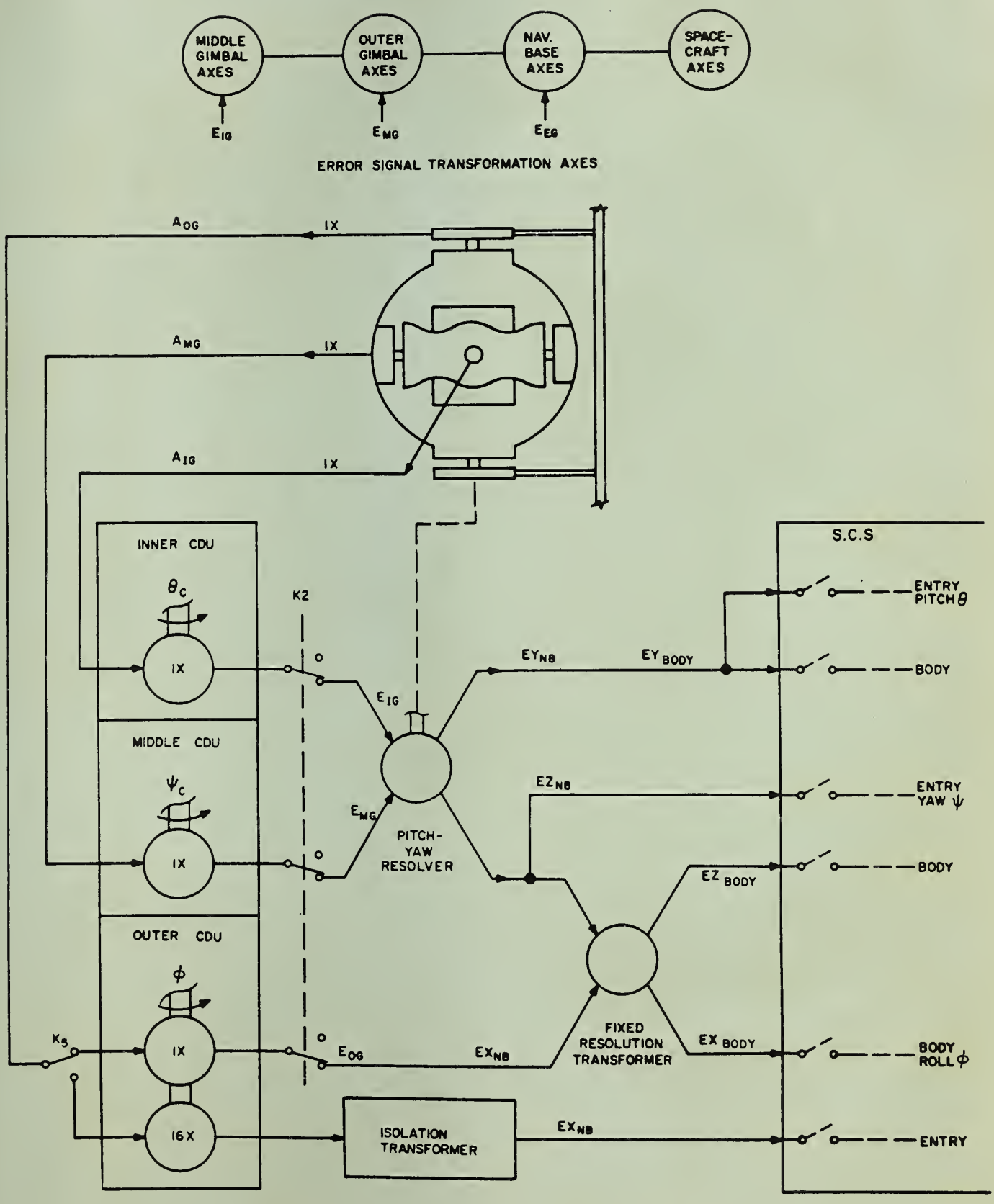


Figure 5-6. Attitude Error Transformation

The resolution required for each error signal is discussed separately even though all three error signals are resolved simultaneously in the actual mechanization (see figure 5-6). The error signals are transformed through as many as four sets of axes. Each error signal is generated in a different set of axes.

The inner gimbal angle A_{ig} is transmitted to the CDU and compared to the CDU angle θ_c and any difference between them results in an error signal, E_{ig}. Since the inner gimbal angle is generated with respect to the middle gimbal and the middle gimbal is mounted to the outer gimbal, it would appear necessary to resolve this A_{ig} about the middle and outer gimbals. However, the middle gimbal angle is small and can be neglected. The outer gimbal displacement may be quite large; therefore, a resolver on the outer gimbal stub shaft is used to modify the inner gimbal error signal. Thus, EY_{NB} the Y Navigation Base error can be shown to consist in part of the resolved inner gimbal error. It is in actuality as follows:

$$EY_{NB} = E_{ig} \cos A_{og} + E_{mg} \text{ sine } A_{og}.$$

Conversely, the Z Navigation Base error, EX_{NB} requires a resolved input because the middle gimbal angle is obtained with respect to the outer gimbal. Thus:

$$EZ_{NB} = -E_{ig} \sin A_{og} + E_{mg} \cos A_{og}.$$

During the attitude control mode, the Navigation Base and stable platform axes do not all coincide with the spacecraft body axes. The X & Z Navigation Base axes are 33 degrees offset from the spacecraft body axes about the Y axis. In order to present error outputs from the ISS in terms of the spacecraft body axes, it is, therefore, necessary to resolve the X and Z Navigation Base errors about the 33^o offset. This is done with a fixed resolution resolver which is used as a transformer. Its action may best be explained by showing the transformations in equation form, thus:

$$EZ_{BODY} = EZ_{NB} \sin 33^o + EX_{NB} \cos 33^o$$

and

$$EX_{NB} = EZ_{NB} \cos 33^o - EX_{NB} \sin 33^o.$$

5.4.6 ENTRY MODE. The purpose of this mode is to reduce the response time required for generating an attitude error signal in the outer CDU which controls the roll of the command module during the entry phase. It is also necessary to provide ISS error output to the SCS in terms of the spacecraft entry axes.

The mode may be entered in manual control or in computer control.

Mechanization of the entry mode is similar to mechanization of the attitude control mode, except that the output of the IMU outer gimbal 1X resolver is switched to the outer gimbal CDU 16X resolver. The roll command to the stabilization and control system during entry is supplied by the outer gimbal CDU 16X resolver. By connecting

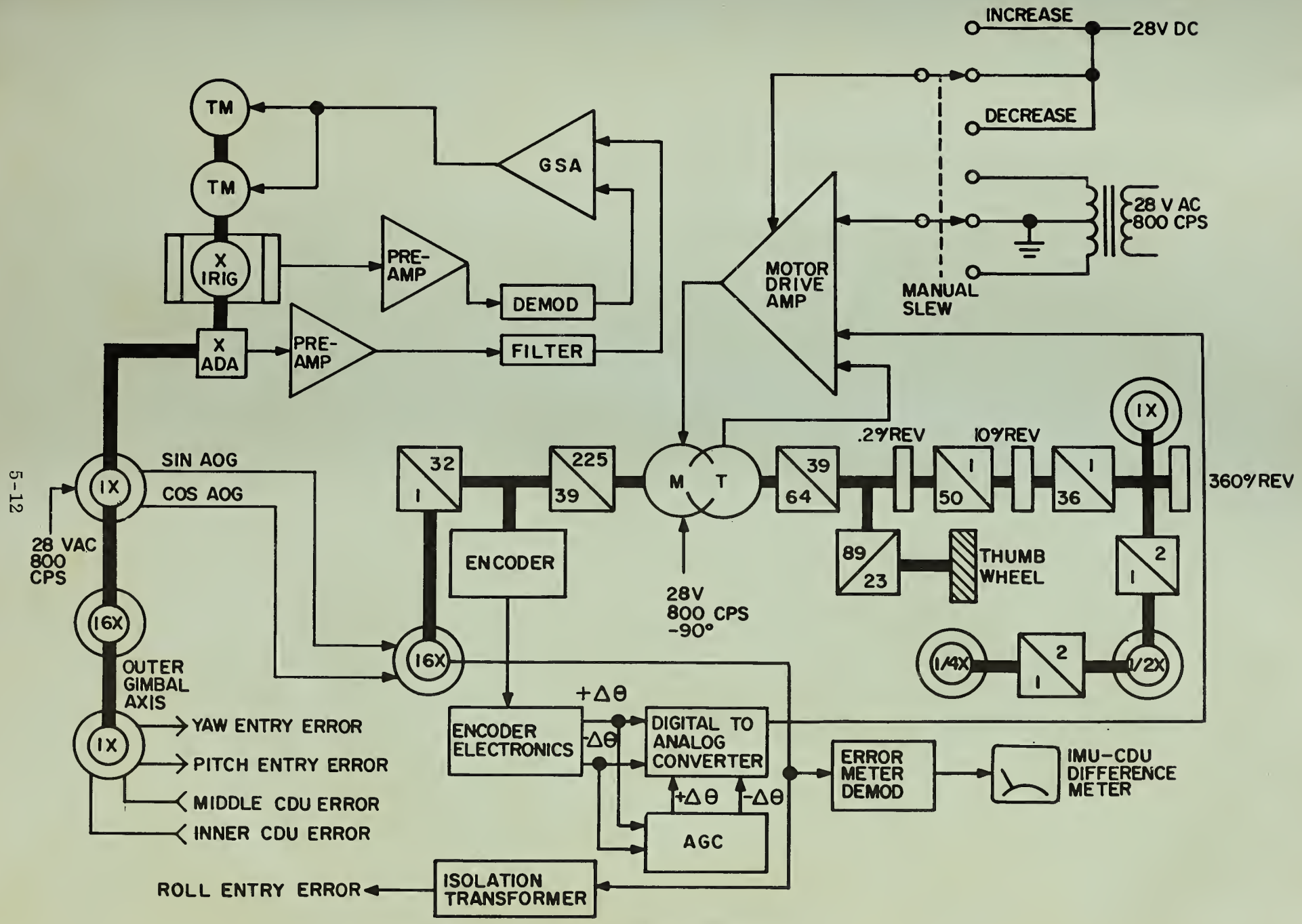


Figure 5-7. Entry Mode (Outer Gimbal)

the 1X IMU resolver to the 16X CDU resolver, the amount of angular rotation of the CDU shaft for a given IMU angle is reduced by a factor of 16. Therefore, when the AGC commands a roll maneuver of X degrees, the CDU is positioned at X degrees/16. Figure 4-6 shows the mechanization for transforming the three CDU attitude errors into spacecraft entry axes.

In addition, the fixed resolution transformer is not being used at this time since the Navigation Base axes coincide with the spacecraft entry axes.

5.5 SUMMARY

The six ISS modes of operation permit the erection and alignment of the IMU stable member and condition the system for the ultimate uses demanded by either the astronaut or the AGC.

The six modes which may be commanded directly by the astronaut or indirectly through the AGC are as outlined below. In addition, the IMU is maintained in a standby condition prior to mode initiation.

5.5.1 ZERO ENCODER. This mode enables the CDU to drive to a zero shaft angle. Outputs from the CDU encoder are thereafter used to accurately indicate CDU angles to the computer, since in this mode, the computer memory is cleared of any CDU angle data.

5.5.2 COARSE ALIGN. In the coarse align mode, the CDU may be positioned to an alignment angle by the AGC. The IMU gimbals are slaved to the CDU angles. The coarse align mode is also entered while gyro wheels are coming up to speed.

5.5.3 MANUAL CDU. The manual CDU mode is similar to the coarse align mode when the manual align button is depressed, except that the CDU's may be positioned with the CDU slew switch. This provision is made in the event of an AGC malfunction.

5.5.4 FINE ALIGN. The fine align mode may be used to bring the stable member to fine alignment by AGC pulsing of the gyro torque microsyn. In this mode, the CDU's are slaved to the IMU gimbals and CDU encoder outputs accurately transmit gimbal angles to the AGC.

5.5.5 ATTITUDE CONTROL. In this mode, attitude error signals are generated by the ISS to control or hold spacecraft attitude. The CDU's are set to a desired angle and the spacecraft is maneuvered until the IMU angles are equal to the CDU angles. The AGC can drive the CDU's in this mode.

5.5.6 ENTRY. In the entry mode, the ISS is mechanized for attitude control of the spacecraft as in the attitude control mode. The outer gimbal 1X resolver is tied into the 16X CDU resolver for increased response to control demands. The ISS axes are at this time parallel with their respective spacecraft entry axes and one stage of resolution is eliminated in the error output signals.

REVIEW QUESTIONS FOR SECTION V

1. The following statements are either True or False, indicate which.

T F a. Of the six modes of operation, three are used for spacecraft steering and attitude control or attitude maintenance.

T F b. The only difference between entry and attitude control modes is the response time of the outer gimbal - CDU error loop.

T F c. During attitude control, the Z spacecraft error is the resolution of the X Navigation Base error and the doubly resolved inner and middle gimbal errors.

T F d. During entry, the axis about which the spacecraft rolls is parallel with the Navigation Base X axis.

T F e. In manual CDU, when the manual align pushbutton is pressed, the CDU's may be driven independently of the gimbals by use of the CDU slew switches.

2. Describe the effect of placing the G & N standby/operate switch on the main D & C panel to operate.

3. What is the reason for zeroing the encoder?

4. In the coarse align mode, the gimbals are driven to specified angles. What determines these angles?

5. Draw a block diagram of the fine align loop showing the following:

AGC to IMU flow.

IMU to CDU flow.

CDU to AGC flow.

SECTION VI

TEMPERATURE CONTROL SYSTEM

INTRODUCTION

This section describes the hardware required to maintain the inertial instruments at their required operating temperatures. Modes of operation, and mode mechanization, as well as selection will be discussed and some malfunction isolation technique will be briefly mentioned.

6.1 IMU TEMPERATURE CONTROL SYSTEM

The purpose of the IMU temperature control system is to maintain the temperature of the three 25 IRIG's and the three 16 PIP's within the required temperature limits during both standby and operating modes of the IMU. The system is designed to both supply and remove heat as required to maintain IMU heat balance with minimum power consumption. Heat is removed by convection, conduction and radiation. The natural convection used during the IMU standby mode is changed to blower-controlled forced convection during IMU operating modes. The forced convection between the middle gimbal and the water-glycol cooled gimbal case is shown in figure 6-1. The IMU internal pressure is maintained between 3.5 and 15 psia to provide the required forced convection. The IMU temperature control system contains circuits designed to supply normal proportional temperature control with the capability of backup or emergency control should the proportional control malfunction. The IMU temperature control system also contains indicator circuitry which provides the astronaut and telemetry with critical parameter monitoring capability, alarm condition indication and provisions for isolating and correcting malfunctions.

6.1.1 MODES OF OPERATION. There are three modes of operation of the temperature control subsystem. These are the proportional, backup and emergency modes. The IMU temperature mode switch on the G & N indicator panel is used to select the mode of operation. There are four switch positions possible and the operation is as follows:

6.1.1.1 Auto Override Position. In the auto override position, the system is normally operating in the proportional mode. Should a failure occur which will cause the temperature of the inertial elements to deviate more than four degrees from normal, an alarm relay automatically switches the control to the emergency mode.

6.1.1.2 Proportional Position. In the proportional position, the control operates such that heater current is supplied by a pulse width modulated 6,400 cps, 2 amp. current. The pulse width is a function of the IRIG control sensor resistance which controls the temperature control magamp output. Should a failure occur in this mode, no automatic override mode switching occurs. This limitation permits operation in the proportional mode when a malfunction occurs in the alarm circuitry.

6.1.1.3 Backup Position. The backup position provides inertial instrument temperature control by changing the function of one of the magamps from that of monitoring to control. The heater current is still proportional to the heat required, but it is amplitude varying DC current and is controlled by both IRIG and PIP indicator sensors. The proportional magamp output is disconnected from the heaters.

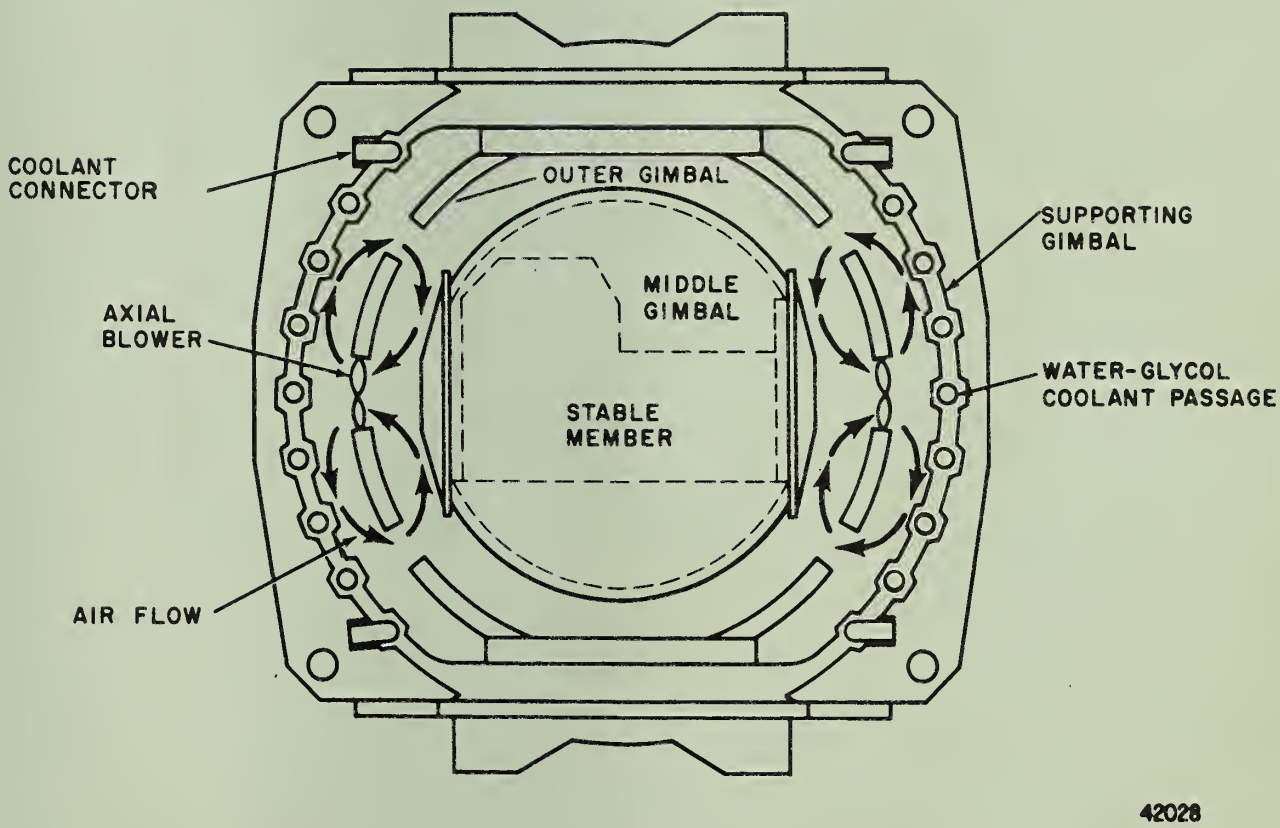


Figure 6-1. Forced Convection Cooling System

6.1.1.4 Emergency Position. The emergency mode places an emergency control module in the heater circuit which provides only on - off control to the heaters. The condition or state of heater current is under the control of a mercury thermostat which has a narrow range of operation. The emergency mode of operation permits only a relatively coarse control of the inertial instrument temperatures. A block diagram of the temperature control is shown in figure 6-2.

6.1.2 TEMPERATURE SENSORS. The temperature sensing elements of the inertial sensors are used for two purposes. One set of sensors is used to control the heating current and one set is used to monitor the temperature. Each IRIG contains four sensors (thermistors). Two are normally used as indicating sensors and are located well within the gyro structure and two, located on the end cap assemblies, are used as control sensors. The PIP's contain two sensors and these are used as indicating sensors. Temperature is controlled at an IRIG end cap temperature of 133.5° F, and a PIP temperature of 130° F.

The IRIG temperature gradient is such that when the internal gyro temperature is 135°, the end cap temperature is 133.5°. The resistance of the sensors is as follows:

SENSOR	TEMPERATURE	RESISTANCE
IRIG Indicator	135° F.	345 ± 10% ohms
IRIG Control	133° F.	126.7 ± .1 ohms
PIP Indicator	130° F.	520 ± .13 ohms

By controlling temperature with the IRIG control sensors, and monitoring the temperature of the PIP's and IRIG's with the indicating sensors accurate proportional control is obtained for both types of inertial instruments.

6.1.3 HEATING ELEMENTS. There are 18 heating elements that are used to maintain correct temperature of the inertial instruments. These are arranged into two groups of parallel heaters, an emergency heat group and a control heat group. During normal operation, all 18 heaters are supplied with power. During the emergency mode, only 9 of the heaters are in use.

The distribution of heating elements for the emergency group is one in each of the three PIP's, one in each IRIG end cap (there are two end caps per IRIG for a total of six emergency heaters) for a total of 9 in parallel.

The control group consists of one control heater in each PIP and one in each IRIG end cap for a total of nine in parallel.

There is an additional fixed bias heater on each of the PIP's which is not controlled by the temperature control but is turned on with the ISS operate power. These supply a bias to compensate for the additional heat generated by the 25 IRIG wheel motor.

6.1.4 AMPLIFIERS. There are five magnetic amplifiers, two saturable reactors and one transistorized control amplifier used in the temperature control electronics. Of the five magamps, two identical units are used as bridge amplifiers for the PIP and IRIG indicating bridges. One amplifier is used for controlling the proportional mode heater current. One magamp is used for measuring heater current and its output is used for telemetry signals. The fifth magamp is a dual purpose magamp. In the proportional mode, it is the indicator sensor alarm amplifier used to monitor the indicator bridges. In the backup mode the amplifier is modified by feedback circuitry changes to become a

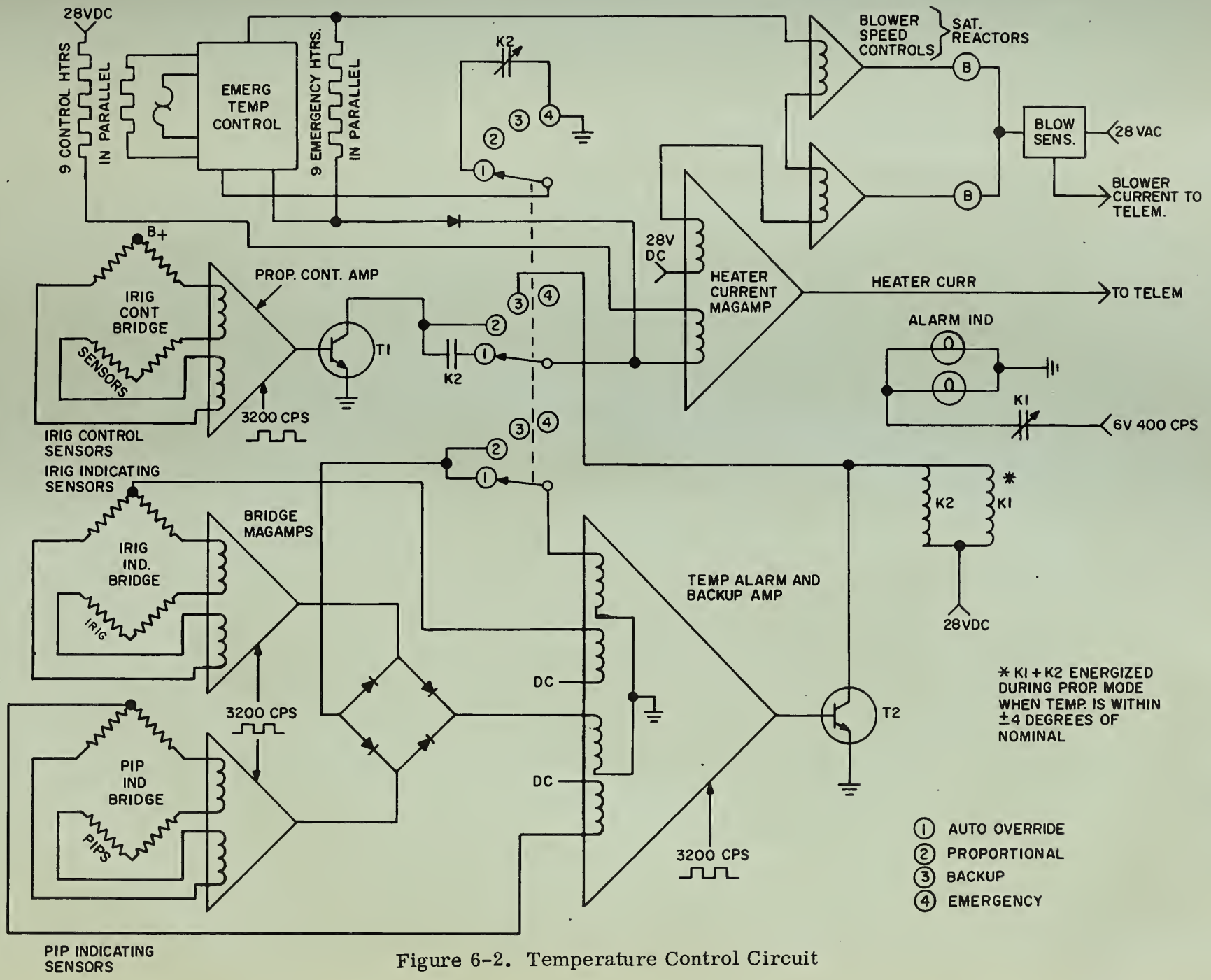


Figure 6-2. Temperature Control Circuit

proportional type of control amplifier for the heaters. Two saturable reactors are controlled by the heater current and their outputs drive the two IMU blowers. A two stage control amplifier comprises the emergency heater module which regulates the heater current on - off cycle in the emergency mode. These amplifiers can be seen in figures 6-2, 6-4, 6-5 and 6-6.

6.1.5 INDICATIONS, TEST POINTS AND SELF-CHECKS. A temperature fail lamp is located on the condition annunciator which gives meaningful indications in the proportional mode. In this mode, it will indicate a temperature error of $\pm 4^{o}$ or greater. When used in conjunction with the zero, IRIG gain or PIP gain switches of the temperature control, it permits a limited malfunction isolation capability to either the IMU or temperature control components. Test points are also available at PSA tray 7 to measure the signals of major importance in the temperature control loops. Figure 6-3 shows the temperature control switches used in commanding the modes and tests.

6.2 PROPORTIONAL TEMPERATURE CONTROL CIRCUIT. The proportional temperature control circuit is the primary means of maintaining the gyro and accelerometer temperature and provides the most accurate control. This type of control is available in two temperature control system switch positions of operation, auto override and proportional. The purpose of the auto override position is to provide automatic switching from the proportional mode to emergency control if there is a temperature control malfunction. If a malfunction occurs in the proportional mode position, the switching to emergency control must be performed manually. (Figure 6-4 shows the proportional temperature control circuit in auto override mode.) In auto override, the emergency mode is entered automatically upon deenergization of the alarm relays, K1 and K2. The six temperature control sensors located in the 25 IRIG end mounts are connected in series to form one leg of a bridge which functions as the control sensing element. The bridge error is applied to a full-wave, self-saturating magnetic amplifier which controls the conduction of an output power transistor. The conduction of the output transistor permits heater current to be supplied to the nine 25 IRIG and 16 PIP control heaters (connected in parallel) and to the nine emergency heaters and two stable member heaters in parallel. Since the supply voltage of the magnetic amplifier is a center-tapped 3,200 cps square wave, the heater current is controlled at 6,400 cps and its pulse width is proportional to the bridge error. The proportional pulse width modulated heater current is two amperes at 28, (+2, -3) volts DC. Since the heater power is proportional only to the temperature error sensed at the 25 IRIG's, it is necessary to supply power to the fixed 16 PIP heaters during IMU operation to compensate for the heat supplied to the 25 IRIG by gyro wheel power dissipation. During IMU operation, the blowers are turned on and their speed is controlled as an inverse function of the heater current sensed by the blower speed control magnetic amplifiers. Blower drive current is inversely proportional to the heater current, and when maximum heat is applied, the blowers are not running. When heater current is off altogether, the blowers are at their maximum speed. Heater current and blower current are indicated to the telemetry system and may be measured at PSA Tray 7 test points.

6.3 BACKUP TEMPERATURE CONTROL CIRCUIT. The backup temperature control and indicator circuit, figure 6-5, is intended for use if the proportional control fails and cannot be repaired by the astronaut. The control sensing elements for this system are three 16 PIP indicating sensors (connected in series) and six 25 IRIG indicating sensors (connected in series) in two separate bridges. These temperature indicating bridge errors are applied to separate temperature indicating amplifiers. The outputs of the amplifiers are applied to the temperature alarm amplifier. The temperature alarm amplifier circuit has been modified by the temperature control mode switch so that it will operate as the backup control amplifier. The switch is placed in the backup mode position to change the transistor operation to

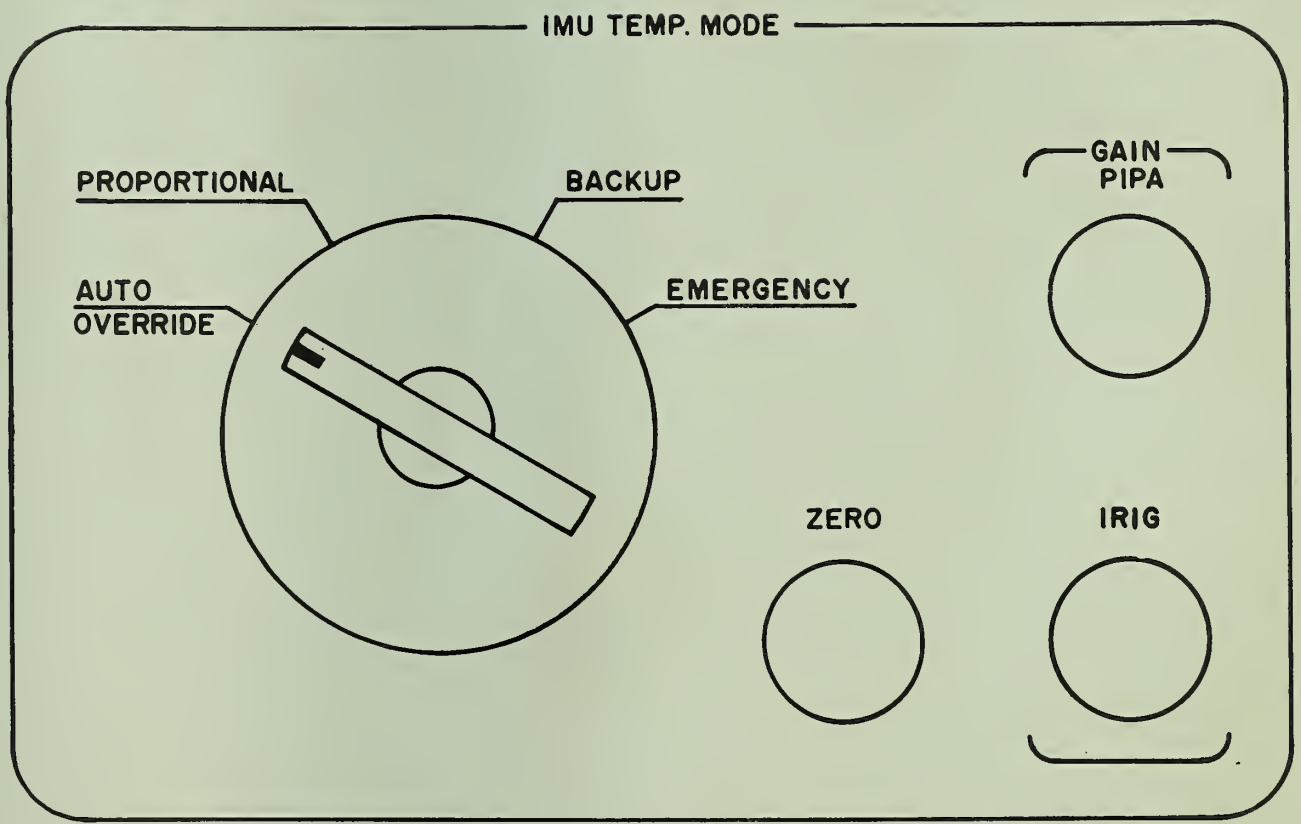


Figure 6-3. Temperature Mode Control

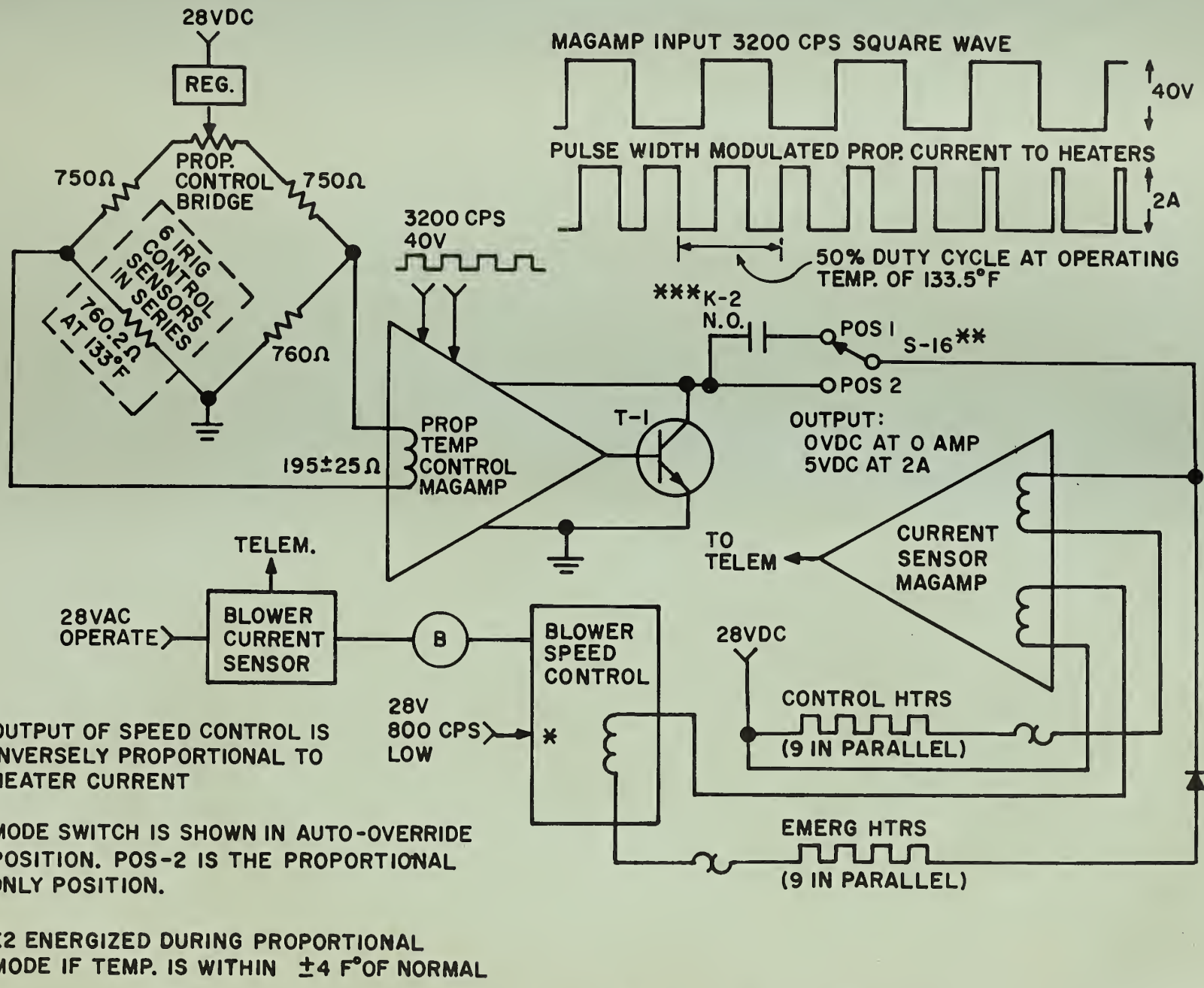


Figure 6-4. Proportional Temp. Control Mode in Auto Override Position

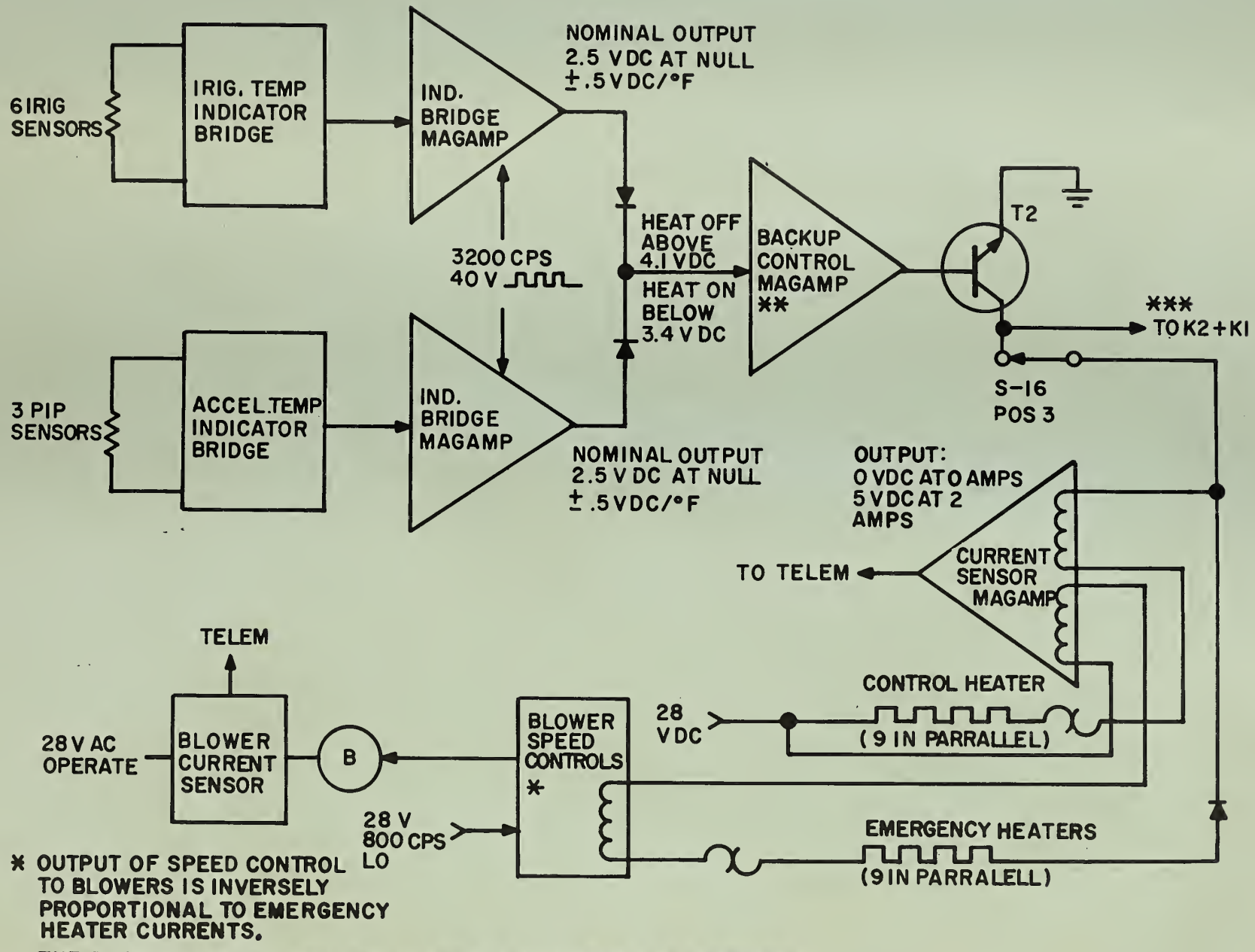

6 IRIG SENSORS
IRIG. TEMP INDICATOR BRIDGE
IND. BRIDGE MAGAMP
NOMINAL OUTPUT 2.5 VDC AT NULL ±.5 VDC/°F
3200 CPS 40 V
HEAT OFF ABOVE 4.1 VDC
HEAT ON BELOW 3.4 VDC
BACKUP CONTROL MAGAMP **
T2
*** TO K2+K1
S-16 POS 3
3 PIP SENSORS
ACCEL. TEMP INDICATOR BRIDGE
IND. BRIDGE MAGAMP
NOMINAL OUTPUT 2.5 V DC AT NULL ± .5 VDC/°F
OUTPUT: 0 VDC AT 0 AMPS 5 VDC AT 2 AMPS
TO TELEM
CURRENT SENSOR MAGAMP
TELEM
CONTROL HEATER
28 VDC
(9 IN PARRALLEL)
28 V AC OPERATE
BLOWER CURRENT SENSOR
B
BLOWER SPEED CONTROLS *
28 V 800 CPS LO
EMERGENCY HEATERS
(9 IN PARRALELL)
* OUTPUT OF SPEED CONTROL TO BLOWERS IS INVERSELY PROPORTIONAL TO EMERGENCY HEATER CURRENTS.
** THE BACKUP CONTROL MAGAMP IS A MODIFIED TEMP ALARM MAGAMP
*** K2 EN. OR DEEN. ACCORDING TO CONDITION OF TRANSISTOR T-2.

Figure 6-5. Temp. Control-Backup Mode

analog proportional current control. The transistor current is used to provide heater current to both the control and emergency heaters. In this mode of operation, an alarm indication is not meaningful to the astronaut because of the modification to the temperature alarm amplifier circuitry.

6.4 EMERGENCY CONTROL CIRCUIT. The emergency control circuit shown in figure 6-6 is intended primarily for use during alarm conditions until the astronaut can determine the trouble in the IMU temperature control system. The emergency control is activated by setting the temperature control mode switch to position 4 (emergency mode) or by deenergizing the alarm relays, K1 and K2, while the mode switch is in position 1 (auto override mode). The control sensing element is a mercury thermostat located near the emergency heaters on the stable member. A preheater element in the mercury thermostat module enables the thermostat to anticipate the instrument temperature and permits more accurate control than a mercury thermostat alone. The thermostat provides switching for the emergency temperature control module, located on the stable member, which controls the emergency heaters. This mode of temperature control is not as accurate as the temperature control provided by the proportional and backup modes. The emergency mode is used only if a malfunction prevents use of the other modes.

6.5 INDICATOR CIRCUIT. The indicator circuit of the temperature control system shown in figure 6-2 operates normally during the auto override and proportional modes. The temperature alarm amplifier is functioning for alarm purposes and the output power transistor is conducting if the inertial components are within $\pm 4^{\circ}$ F. of their normal operating temperature. The conducting condition maintains the alarm relays in an energized state. Should the temperature fall outside these limits, the relays will deenergize and the "IMU TEMP" lamp on the condition annunciator will light. In addition, if the system is in the auto override mode, the system is switched to emergency control. This operation is not applicable during the backup and emergency modes. When these modes are manually selected, the temperature alarm amplifier is modified and the "IMU TEMP" lamp does not indicate a meaningful alarm condition. To provide a ground check of the system operation, 25 IRIG and 16 PIP average temperature indications and controlled heater and blower current indications are channeled to telemetry equipment for transmission to the ground station during flight.

6.6 TEMPERATURE CONTROL SYSTEM OPERATION

The operation of the temperature control system is controlled from the IMU temperature control group located on the G & N indicator control panel described subsequently. This panel contains the temperature control mode switch. The operation and calibration of the indicator circuit can also be checked by utilizing the "zero" and "gain" buttons. When either of the gain buttons is depressed, the indicator bridges are unbalanced by the insertion of a resistor. This resistor duplicates the sensor resistance of the inertial instruments at a 5° F. off temperature condition. Relay K2 should, at this point, deenergize if the alarm circuit is functioning properly and the alarm light will come on. Conversely, if the system has been operating normally in the proportional mode and then jumps into an alarm condition, the "zero" button may be used to isolate the failure. The zero button substitutes a resistor in each of the indicating bridges which duplicates sensor resistance at the exact operating temperature. Should the alarm condition remain, the alarm circuit is obviously malfunctioning and it is assumed that the control circuit and control sensors are operable. Should the alarm condition cease, the inertial instrument temperature may be incorrect, and further checks at test points must be performed. The logical move at this time would be to switch to the emergency mode. Figure 6-7 shows the gain and zero buttons and their effect on indicator circuitry. Signals indicating the condition of the temperature control system are available for monitoring at test points on the power servo assembly.

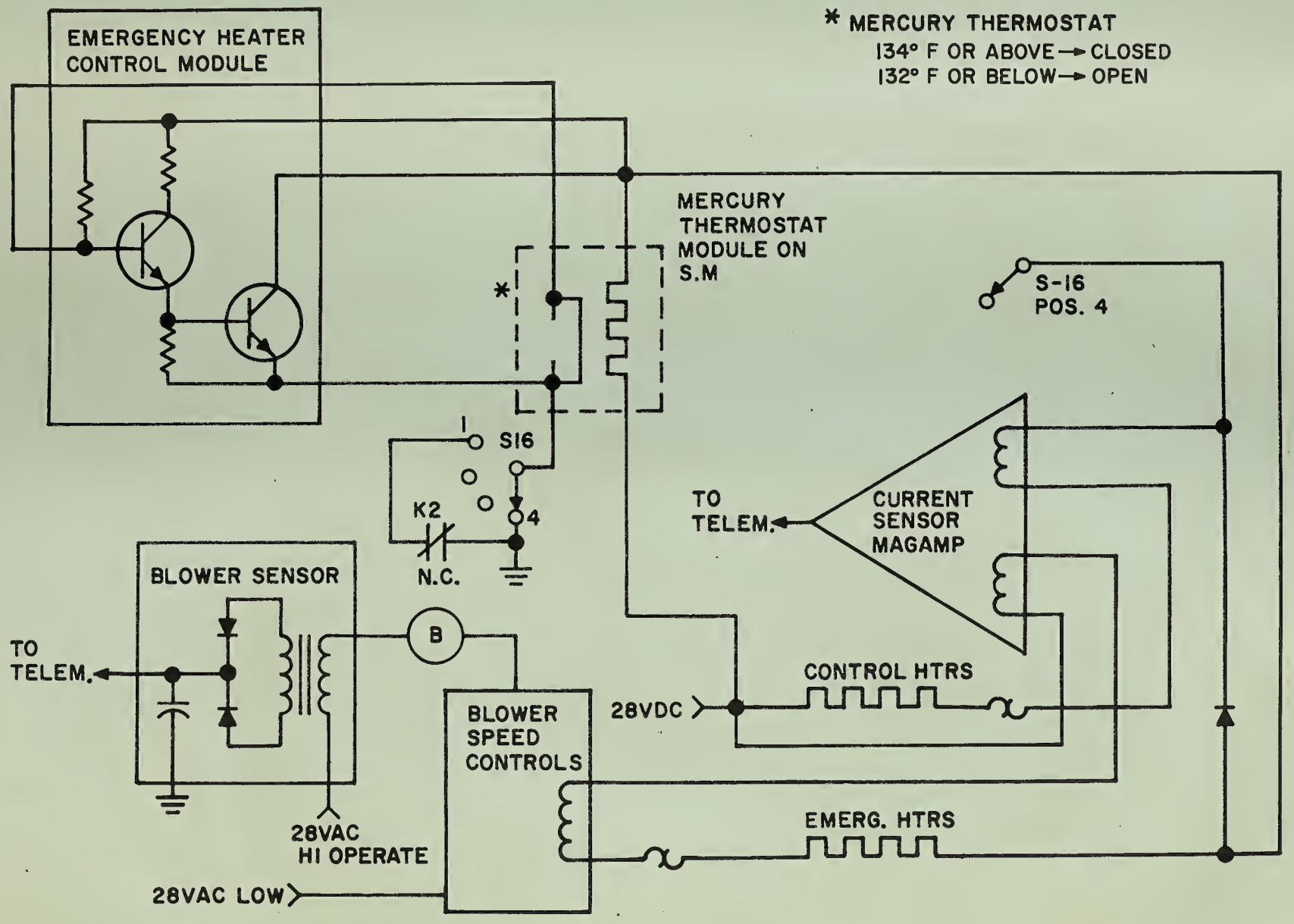


Figure 6-6. Emergency Temp. Control Mode in Emergency Position of S-16

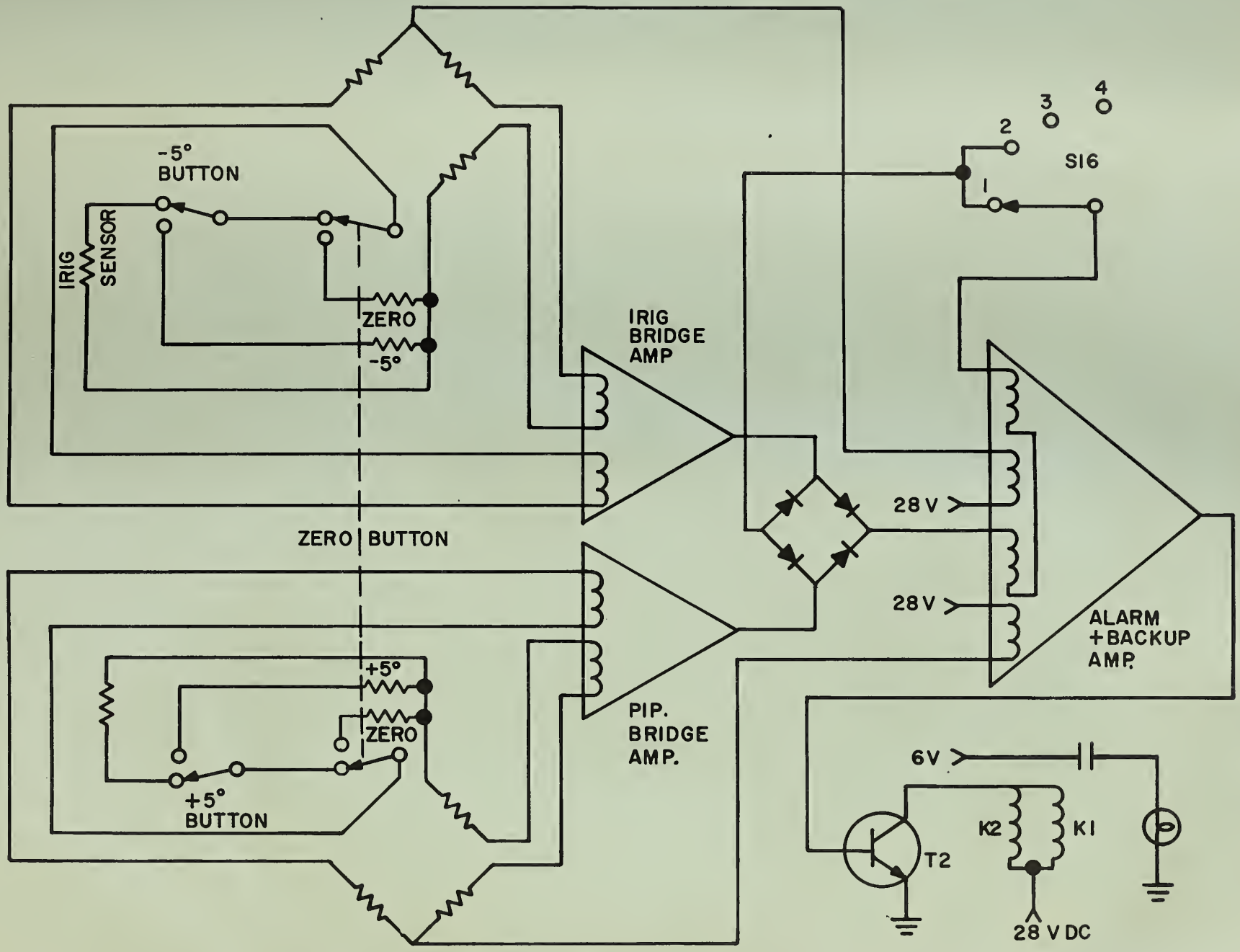


Figure 6-7. Zero and Gain Switch Circuitry to Alarm Amplifier

6.7 SUMMARY

The temperatures of the inertial instruments of the ISS are maintained both by adding and/or removing heat with a combination of heaters and blowers and an IMU case that has integral water-glycol coolant passages. Control of the temperature is accomplished by the temperature control switch on the lower D & C, and the temperature control electronics in PSA Tray 7.

There are four positions of control on the mode switch and three modes of operation. The primary mode is the proportional mode during which heat is controlled by the IRIG control sensors at the input of the proportional temperature control magamp. During this mode, the indicator sensors of the inertial instruments are used to control an alarm amplifier for monitoring the system temperatures. A backup mode is available in the event of a failure of the proportional control amplifier. In this mode, the indicator circuitry is modified to provide control of heat to the instruments. There is also an emergency mode which does not depend on the circuitry of the other modes and supplies heat as a function of stable member temperature.

The three modes of operation are demanded by corresponding switch positions on the control. In addition, an auto override position permits the system to operate in the primary mode (proportional) and in event of malfunction will automatically switch to the emergency mode.

REVIEW QUESTIONS FOR SECTION VI

1. The following statements are either True or False; if False state why.

T F a. In the proportional mode of temperature control, the IRIG indicator sensors control the heater current.

T F b. If the IRIG gain button is depressed during the proportional mode, the alarm light will come on.

T F c. The auto override position will switch the temperature control to backup automatically in the event of a failure.

T F d. The PIP gain switch simulates a 5^{o} F. underheat condition.

T F e. The emergency mode mercury thermostat is preheated by the bias heaters.

2. What type of temperature control operation and indications would you expect to see in the auto override position if the PIP indicator sensors were open?

3. How many heaters are used for temperature control and where are they located?

4. How could you verify the conditions of question 2? Would the astronaut remain in this mode or not? Which mode could be used to provide the astronaut with the most accurate control under the conditions of question 2?

SECTION VII

DISPLAY AND CONTROL GROUP

INTRODUCTION

This section describes the lower display and control components and their functions in the inertial subsystem.

7.1 LOWER DISPLAY AND CONTROL PANELS

The lower display and control panels provide the navigator with a means of manually controlling and monitoring the G & N system. The lower display and control panels consist of an IMU control panel, G & N indicator control panel, CDU panel, computer display and keyboard panel, condition annunciator and optics control panel. The optics control panel is explained in Section IX and the computer display and keyboard panel is explained in Section XI. The CDU panel has been explained in Section III, and the condition annunciator is described in Section VIII. See table 7-1 for a list of switches used on the IMU control panel and on the G & N indicator control panel. Figure 7-1 shows the lower D & C panels.

7.2 IMU CONTROL PANEL

The IMU control panel is approximately six inches wide by 9-3/4 inches high, constructed on honeycombed, sandwiched aluminum. It contains an IMU mode control switch assembly, a transfer switch, an IMU-CDU difference meter and a manual align switch. (See figure 7-2.)

7.2.1 TRANSFER SWITCH. The transfer switch determines the method of mode selection. It allows selection of operational modes by the AGC or the navigator. When it is in the computer position, the AGC controls the selection of the IMU mode of operation. When it is in the manual position, the navigator can select the IMU mode of operation with the mode control switch.

7.2.2 MODE CONTROL SWITCH ASSEMBLY. The six button mode control switch assembly allows manual selection of six operational modes. Each button contains an internal lamp which lights to indicate that the G & N system mode of operation has been entered.

7.2.3 IMU-CDU DIFFERENCE METER. The IMU-CDU difference meter presents a three-axis display of signals generated by the G & N system. The display is presented on a meter as pitch, yaw and roll deviation signals. The signals are applied to the meter as a demodulated output of the CDU single-speed resolvers. The meter scales are calibrated from 0 to ± 5 degrees.

7.2.4 MANUAL ALIGN BUTTON. The manual align button allows control of the IMU gimbals by the CDU's in manual CDU mode.

Table 7-1. D & C Panel Switches

Panel	Switch Name	Operational Use	Switch Type
IMU Control Panel	1. Transfer	IMU Moding Control	Toggle
	2. Manual Align	IMU Moding	Pushbutton
	3. Mode	IMU Mode Selection	Pushbutton
G & N Indicator Control Panel	1. Check condition lamps	IMU temperature lamps	Pushbutton
	2. Check coolant	Lights up IMU case	Pushbutton
	3. Zero	Temperature Control Check	Pushbutton
	4. Gain PIPA	Temperature Control Check	Pushbutton
	5. Gain IRIG	Temperature Control Check	Pushbutton
	6. IMU Temp Mode	Temp. Mode Select	Rotary
	7. Check mode lamps	Mode lamps	Pushbutton
	1. Optics hand controller	Optics drive	Control
	2. Slave telescope	Optics Moding & Control	Toggle
	3. Sextant power	Optics Moding & Control	Toggle
	4. Optics mode	Optics Moding & Control	Rotary
	5. Speed controller	Optics Moding & Control	Toggle
	6. Mode controller	Optics Moding & Control	Toggle
	7. Mark and mark reject	Optics Moding & Control	Momentary Pushbutton
	1. Control	Attitude impulse control	Impulse
	2. Enable	Attitude impulse control	Toggle
	1. Panel brightness	Panel lamp control	Rotary

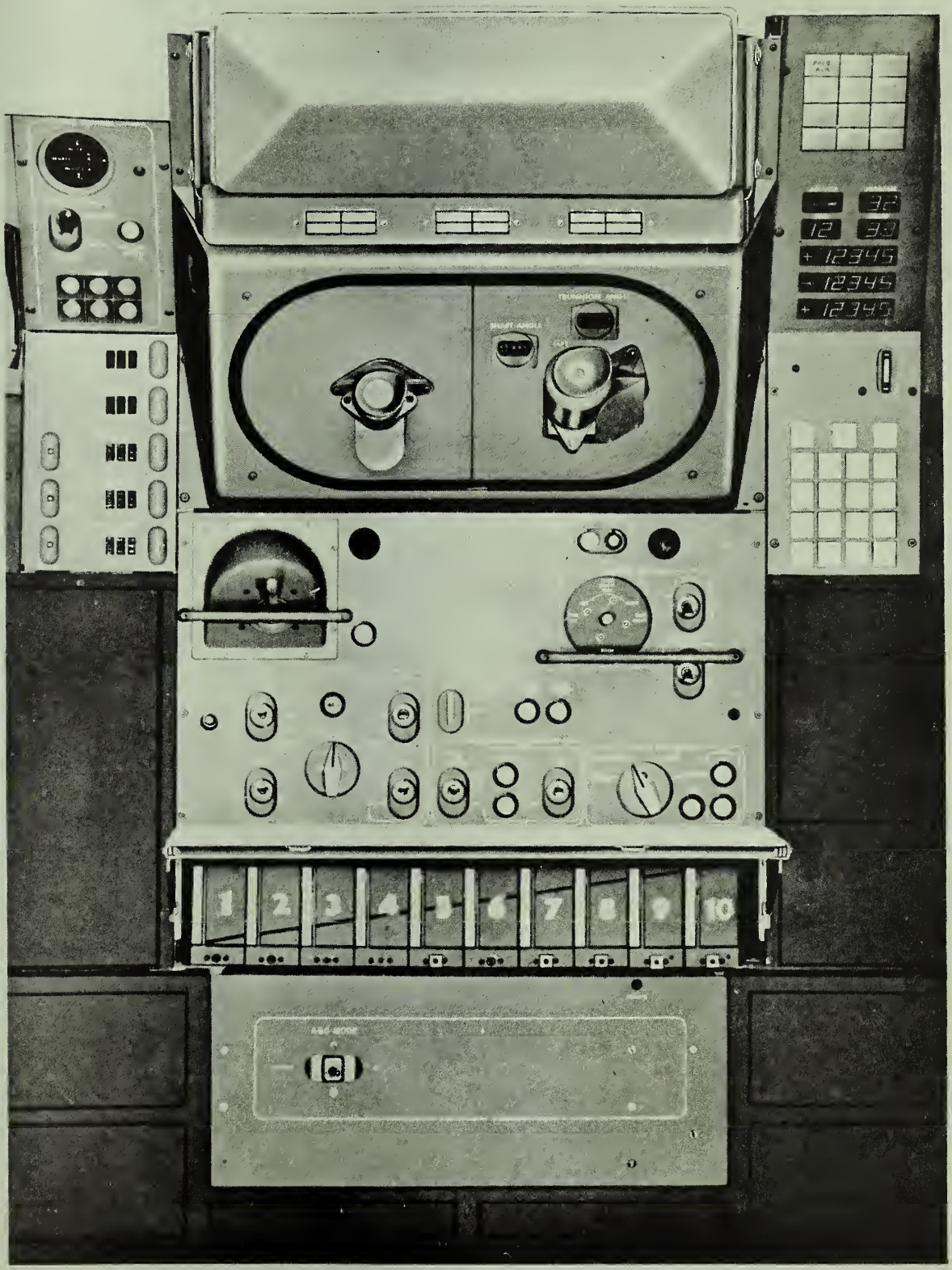


Figure 7-1. Lower D & C Panels

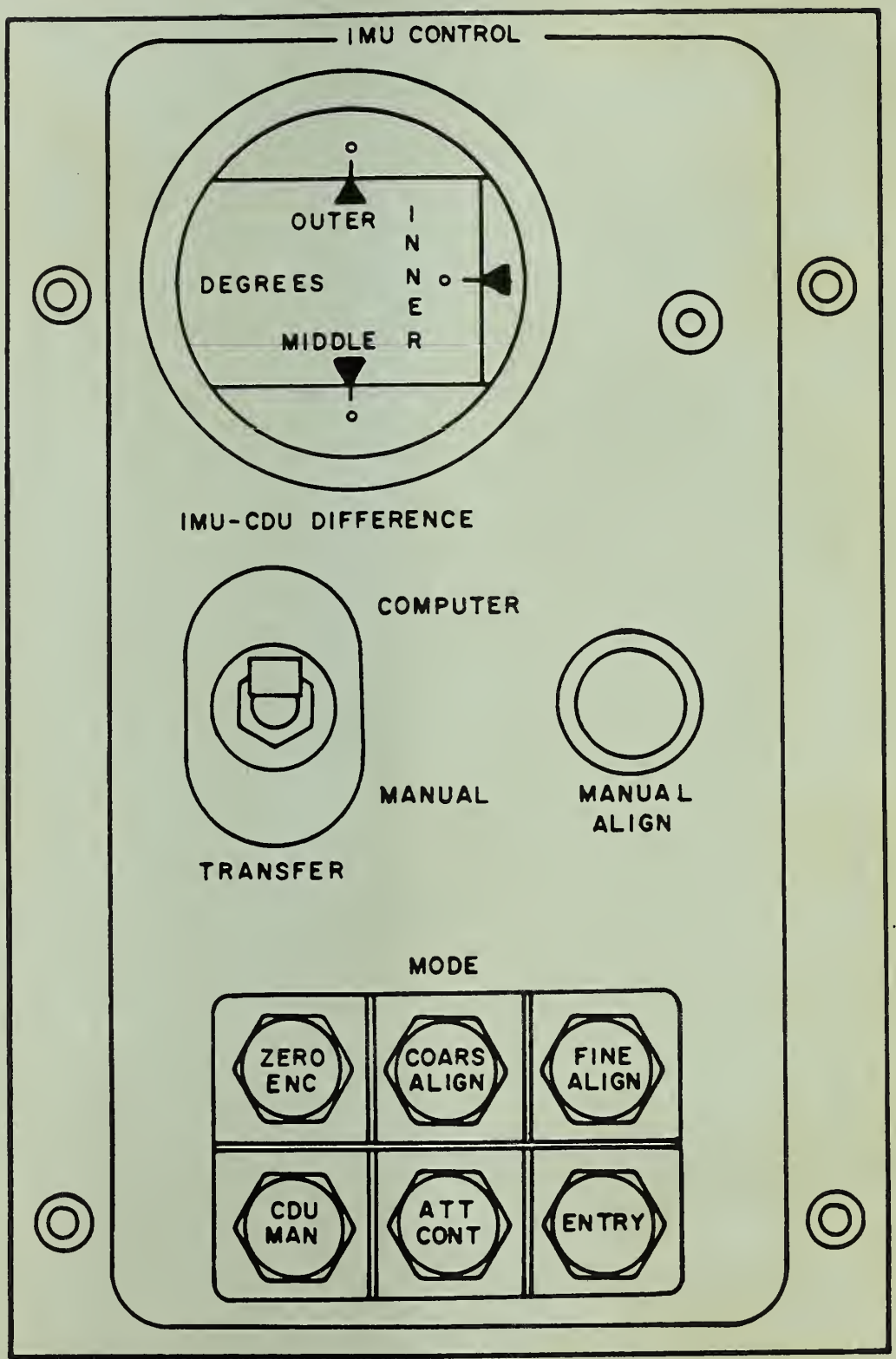


Figure 7-2. IMU Control Panel

7.3 DISPLAY AND CONTROL ELECTRONICS

The display and control electronics are welded, encapsulated, plug-in-type modules mounted on a base assembly which is attached to the spacecraft structure above the left PSA tray. The electronics consists of a panel brightness control, a 100 second time delay electronics, a relay and diode module, and three attitude error demodulators. The relay and diode module is constructed with an aluminum housing while the other display and control electronics modules are constructed with a plastic housing (see figure 7-3).

7.3.1 PANEL BRIGHTNESS CONTROL. The panel brightness control allows the navigator to control the brightness of various lamps and indicators in the spacecraft. A +28 volt DC input is dropped across a 1,500 ohm, 3 watt resistor in series with the control winding and then applied to the control winding of a saturable reactor. A variable rheostat regulates the excitation of the control winding. As the current in the control winding increases, the impedance of the output winding increases resulting in decreased current flow in the 6 volt, 400 cps illumination output circuit.

7.3.2 100-SECOND TIME DELAY. The 100-second time delay circuit is used during IMU turn-on to provide time for the stabilization gyro wheels to come up to speed before switching control of the stable platform to the stabilization loop. A 28 volt DC input is dropped across a resistor and held at 18 volts by a zener diode. A resistor capacitor network, controlled by a transistor, allows the capacitor to change slowly. The capacitor buildup permits a voltage to be impressed on the emitter of a unijunction transistor which acts as a gate. The output of the gate conducts through a zener diode to a switching transistor. When the transistor conducts, it provides a ground to the time-delay-relay circuit, causing the relay to energize. When the time-delay-relay energizes, the +28 volt DC circuit is completed to ground through the energized relay contacts.

7.3.3 DEMODULATOR CIRCUIT. The three attitude error demodulators receive and demodulate the output of the 1X inner, middle and outer gimbal CDU resolvers. The input to each demodulator is applied to an input transformer and amplified by two transistor stages. This amplification is controlled by a zener diode and applied to the primary winding of a coupling transformer. The transformer secondaries are used to control a rectifying circuit consisting of a chopper and a resistor-capacitor network, with a 28 volt rms, 800 cps reference. Switching occurs, based on the demodulator phase input, and a related DC output is provided which is routed to the IMU-CDU difference meter.

7.4 G & N INDICATOR CONTROL PANEL

The G & N indicator control panel is approximately 23-1/2 inches wide by 12-3/4 inches high and is constructed from honeycombed, sandwiched aluminum. It is located in the center portion of the lower display and control panel at the navigation station. It contains the IMU temperature control group, check coolant button, optics control group, map and data viewer panel controls and attitude impulse control (see figure 7-4). The map and data viewer is no longer a part of the system; therefore, the controls are not functional even though present.

7.4.1 IMU TEMPERATURE CONTROL GROUP. The IMU temperature control group consists of a temperature control mode selector, a zero button, IRIG gain button, and a PIPA gain button. The IMU temperature control group selects the mode of temperature control and provides switching to check out the indicating circuitry. The temperature control circuits have four modes of operation activated by a rotary selector and monitored by the controls and indicators of the IMU temperature control group. An interlock switch places the IMU temperature control in the emergency mode when the G & N indicator control panel is removed.

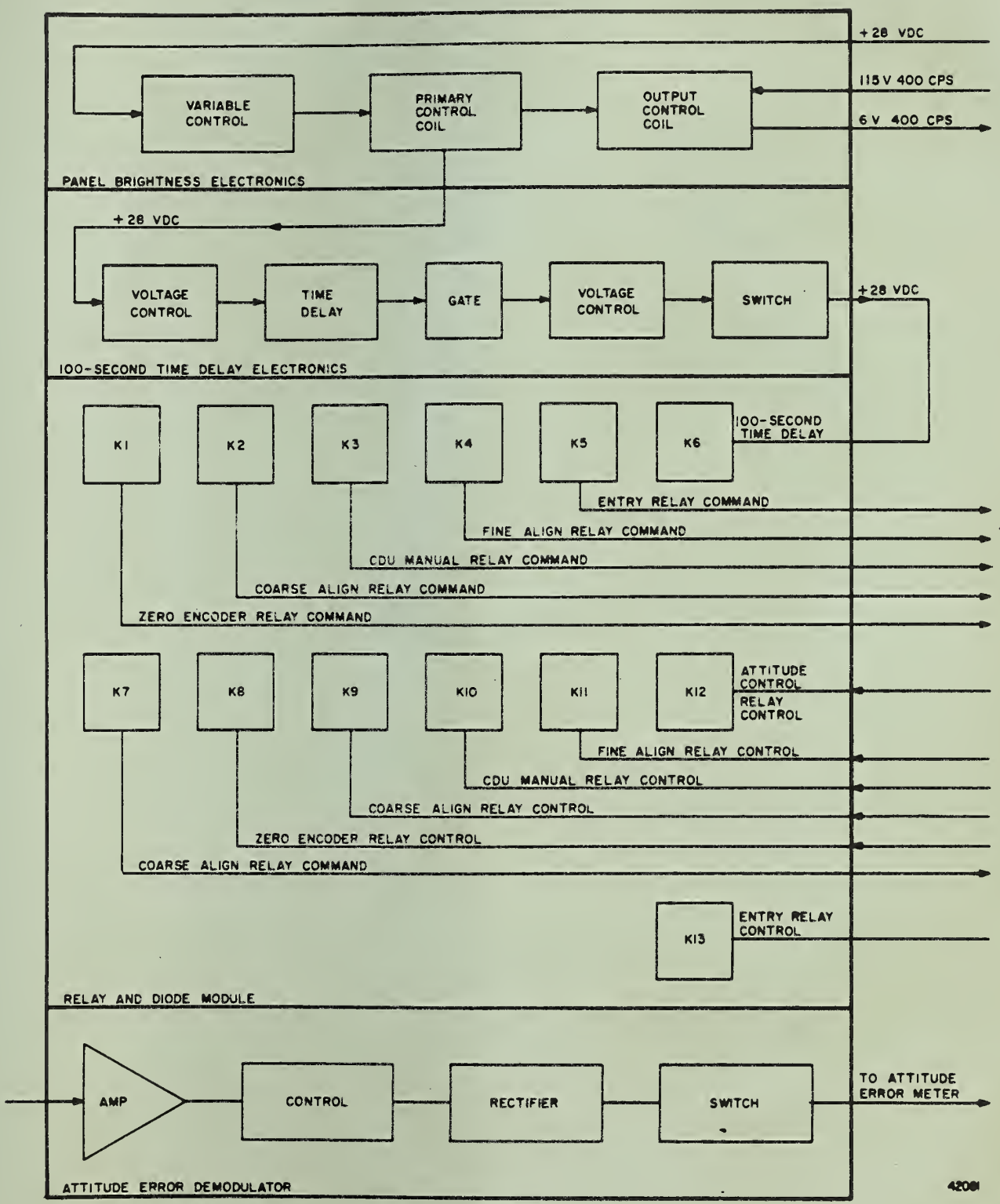


Figure 7-3. D & C Electronics

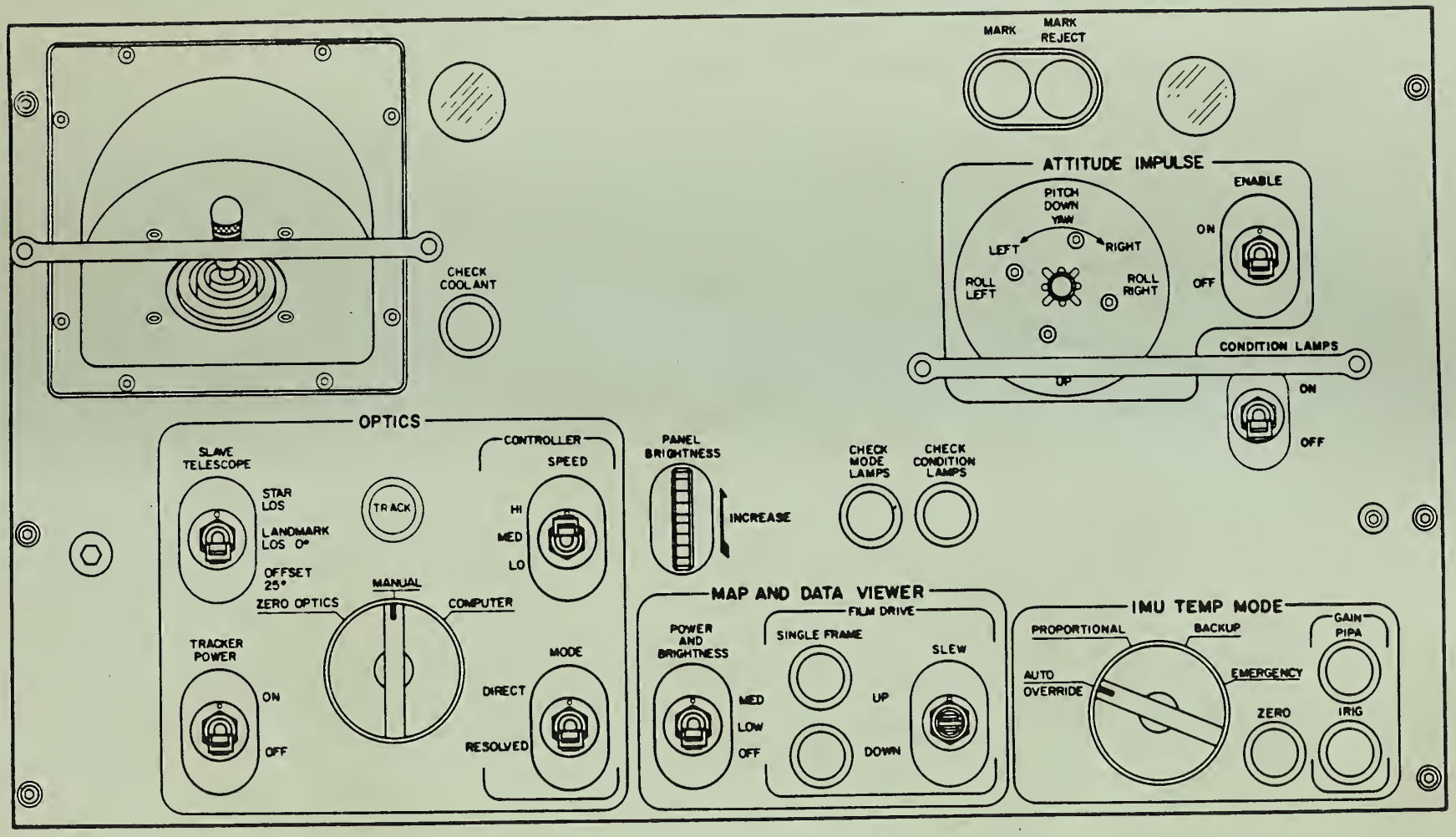


Figure 7-4. G & N Indicator Control Panel

7.4.1.1 Temperature Control Mode Selector. The temperature control mode selector gives the navigator the capability of manually selecting proportional, back-up or emergency temperature control. An auto-override position provides automatic switching from proportional to emergency control in the event of an alarm condition.

7.4.1.2 Zero Pushbutton. This pushbutton is pressed to calibrate 25 IRIG and PIPA temperature monitoring devices. Standard operating resistances are used as a dummy load.

7.4.1.3 IRIG Gain Pushbutton. This pushbutton is depressed to calibrate 25 IRIG temperature monitoring devices with a standard resistance equal to the resistance of the 25 IRIG temperature indicating sensor when operating at 5^{o} F. below normal temperature and to check condition annunciator alarm indication.

7.4.1.4 PIPA Gain Pushbutton. This pushbutton performs a function similar to the IRIG gain button except that the resistance is equivalent to PIPA indicating sensors when operating at 5^{o} above normal temperature. It also checks the condition annunciator alarm indication.

7.4.2 CHECK COOLANT. The check coolant button enables the navigator to physically monitor the condition of the IMU coolant supply system. When the button is pressed, power is applied to flood lamps located behind the lower panel. This enables the navigator to view the IMU quick disconnect hoses through two inspection windows in the G & N panel.

7.4.3 ATTITUDE IMPULSE CONTROL. The attitude impulse control switch is used for fine control of the spacecraft in pitch, yaw and roll. The switch is an impulse type switch providing incremental outputs. A twist of the switch will provide yaw movements. Up and down movements of the switch affect spacecraft pitch, and right and left movements of the switch affect roll.

7.5 CONDITION ANNUNCIATOR ASSEMBLY

An indicating light assembly is located at the upper left area of the D & C to indicate G & N malfunctions. This will be described further in Section IX.

7.6 MAIN DISPLAY AND CONTROL PANELS

The main display and control panel is located directly in front of the astronauts as they assume reclining positions on their couches. It displays monitoring signals from the spacecraft systems and contains controls to operate portions of the systems. This paragraph describes only those controls which affect the G & N system.

The main display and control panel contains a flight director's attitude indicator which receives IMU gimbal angle position signals from the 1X resolvers located on the IMU gimbals when the SCS is in the G & N modes. Power switches located on the panel apply power to the G & N system. The G & N sync switch is a two position paddle arm toggle switch. It is used when slaving the CDU's to the IMU during manually commanded spacecraft attitude changes. Following completion of a spacecraft attitude change, the CDU's establish an attitude hold position at the new spacecraft attitude. Placing the switch in the on position places the inertial subsystem in the manual CDU mode. If the stabilization and control system G & N attitude control mode is selected and the three-axis rotational hand controller is utilized by the astronaut, the stabilization and control system relay energizes. This relay will cause the

inertial subsystem to enter the fine align mode at which time the CDU's will follow the IMU gimbals. At the completion of the spacecraft maneuver, that relay will deenergize and a new attitude will be established and maintained.

The stabilization and control system backup accelerometer is also controlled from the main display and control panel. This accelerometer and its associated electronics and displays are utilized as a backup for the inertial subsystem and accelerometer in case of G & N system malfunction.

7.7 SUMMARY

The lower display and control group provides the astronaut with complete G & N control and monitoring capabilities. It contains the IMU control panel, CDU panel, computer display and keyboard panel, condition annunciator assembly, and G & N indicator control panel.

Associated with the lower D & C is the D & C electronics containing relays and a demodulator for ISS operation circuit as well as panel brightness lamp circuitry.

REVIEW QUESTIONS FOR SECTION VII

1. List the panels found on the lower D & C group.

2. Which of the D & C panels are associated with the inertial subsystem?

3. Describe the purposes of the various control groupings on the G & N indicator panel.

SECTION VIII

ISS POWER AND POWER DISTRIBUTION

INTRODUCTION

This section deals with a discussion of the inertial subsystem power supplies on a block diagram level. Additional discussion includes descriptions of the power servo assembly and the construction and purposes of the components constituting the PSA. A guide to the location of the various G & N amplifiers, power supplies and other circuit modules is included in the discussion.

8.1 ISS POWER SUPPLIES

The inertial subsystem has seven power supplies. These are controlled by the IMU and IMU heater switches on the main D & C panels of the spacecraft. These power supplies are as follows: -28V DC supply, pulse torque supply, 800 cps, 1% supply, 800 cps 5% supply, 25.6 k cps encoder supply, 3.2 k cps 1% sine wave supply, 3.2 k pps square wave supply. Frequency reference inputs to all AC power supplies are obtained from the computer; however, built-in frequency sources are a part of each supply to enable operation independent of the computer. Figure 8-1 shows the distribution of power to the G & N system.

Inputs to the inertial subsystem power supplies are 7 volt signal pulses generated by the AGC scaler and 27.5 volts DC from the spacecraft primary power.

8.1.1 -28 VOLT DC SUPPLY. The -28 volt DC power supply module is located in Tray 1 of the PSA. It supplies excitation to three gimbal servo amplifier modules and three gimbal coarse align amplifier modules in Tray 1 of the PSA. It also supplies excitation to three AC differential amplifier modules located in Trays 3 and 4. The -28 volts DC is also supplied to the angular differentiating accelerometer preamplifiers in the IMU (see figure 8-2). Inputs to the -28 volt DC power supply are +27.5 volt DC primary power to B+ application and 12,800 pps continuous power from the AGC scaler as a 7 volt 3.0 microsecond square pulse. The 12,800 pps input is inverted and supplied to a multivibrator with a triggered frequency of 6.4 kc. If no input is supplied to the multivibrator, it will free run at 6.0 to 6.2 kc. The multivibrator output is used to drive a high-power chopping stage. The output of this chopping stage is applied to a full wave rectifier through transformer coupling. The full wave rectifier circuit is connected to provide a filtered negative voltage output.

8.1.2 PULSE TORQUING DC SUPPLY. The pulse torquing DC supply modules are located in Trays 2 and 7 of the PSA. These power supplies provide the 16 PIPA current switch excitations, the 25 IRIG current switch excitations, and precision voltage regulator power. Monitoring circuits for the pulse torquing DC power supply outputs are built into the supply. The pulse torquing DC supply modules can be used interchangeably as a 25 IRIG power supply or 16 PIPA power supply. When they are used to supply the three PIP accelerometer loops, the +12 volt dc output is not used (see figure 8-3). A B+ signal of 27.5 volts DC from spacecraft primary power and a 7 volt, 3 microsecond, square pulse at 12,800 pps from the AGC scaler are the inputs to the pulse torquing DC supply. The pulse train input is inverted and supplied to a

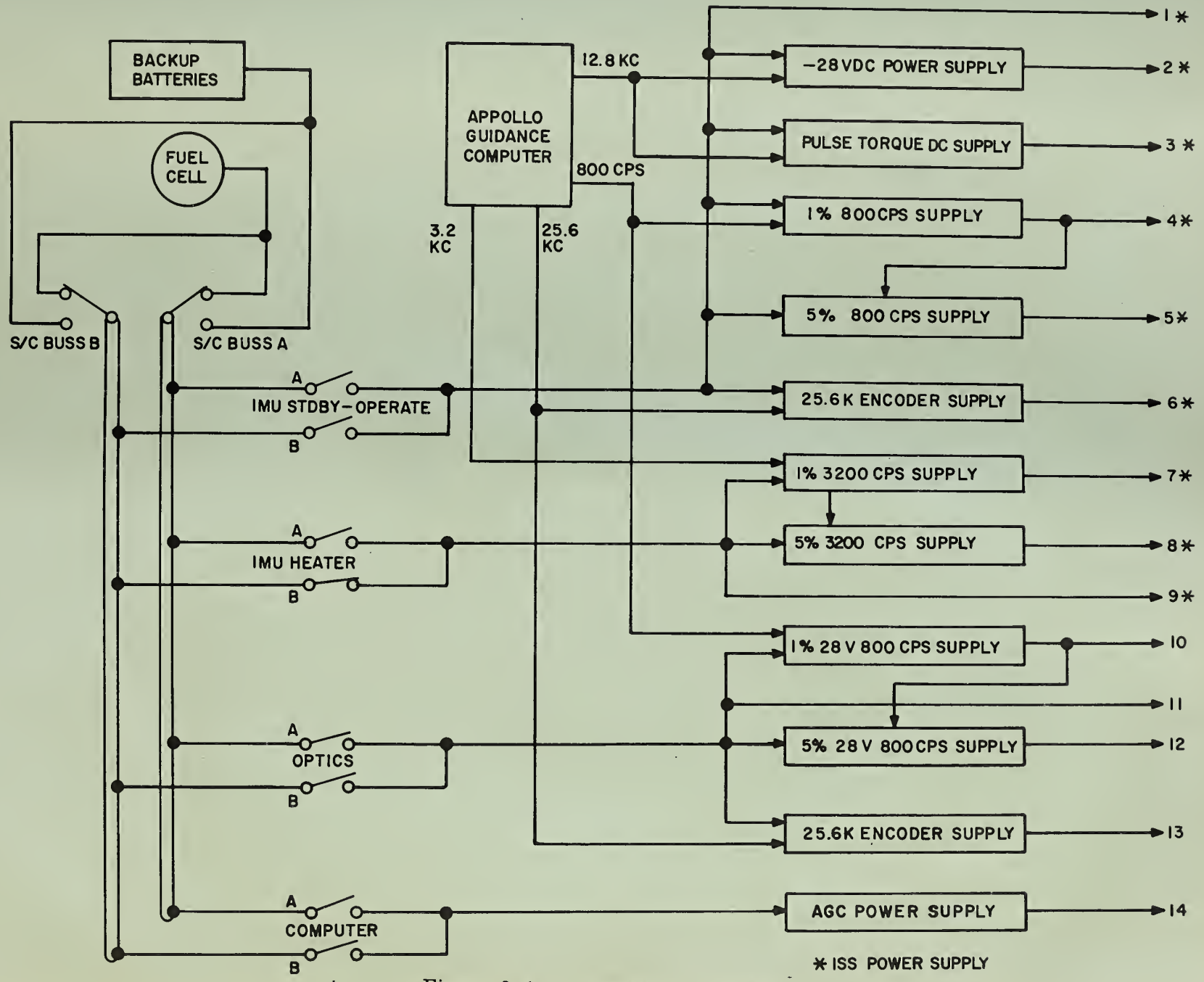


Figure 8-1. Inertial Power Supplies

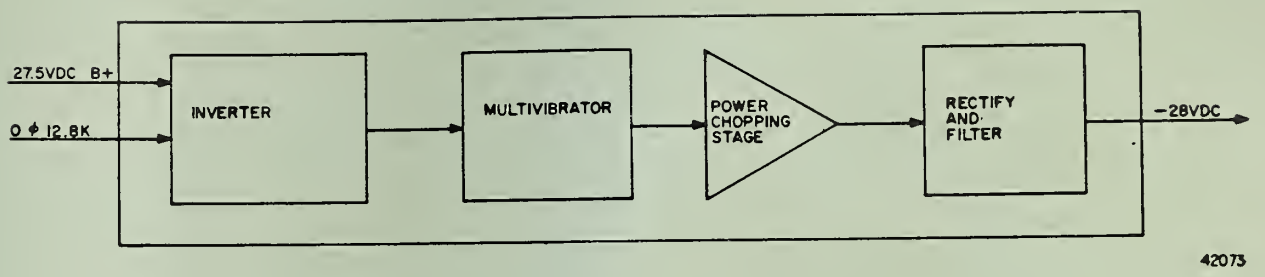


Figure 8-2. -28 VDC Supply

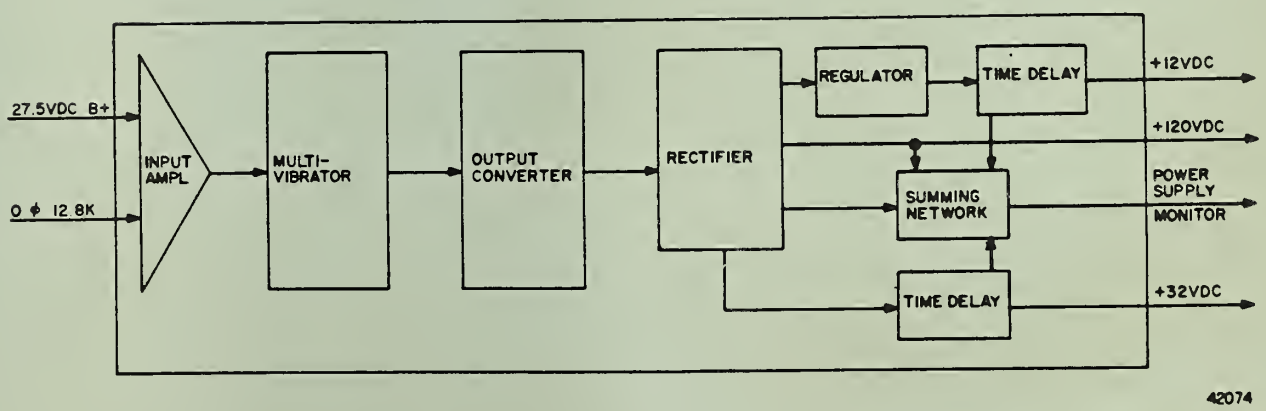


Figure 8-3. Pulse Torque Power Supply

multivibrator which is triggered, and runs at 6.4 kc. If an input is not supplied to a high-power chopping stage where the signal is amplified, chopped and transformer-coupled to a full wave rectifier. The +12 volt DC output is regulated utilizing a three-stage transistor circuit with a zener reference.

8.1.3 800 CPS POWER SUPPLIES. The 800 cps inertial power supply circuits each consist of three modules: (1) automatic amplitude control, filter and multivibrator, (2) 800 cps, 800 cps, 5% amplifier, and (3) 800 cps 1% amplifier. The 800 cps supplies are located in Tray 2 of the PSA (see figure 8-4). The outputs of the 800 cps, 1% supply are used for CDU resolver excitation, CDU tachometer excitation, S.C.S. reference, IMU resolver excitation and coarse align demodulation. The outputs of the 800 cps, 5% supply are used for 25 IRIG wheel excitation, IMU blower excitation and CDU motor excitation. A dual (0 phase and π phase), 800 cps, 7 volt, 3 microsecond pulse signal from the AGC is used as an input to a multivibrator that is part of the automatic amplitude control, filter and multivibrator module. The automatic amplitude control output is filtered before it is supplied as an input to the 1% power amplifier module. The output of the 1% power amplifier is a 28 volt rms signal which, in addition to its direct uses, is a feedback signal to the automatic amplitude control and an input to the 5% power amplifier. The input signal to the 5% power amplifier is applied to a phase shift network and then amplified to obtain the 28 volt rms, -90 degree-out-of-phase output. The outputs of both the 5% and the 1% power amplifiers are applied to an IMU-CDU load compensation network to provide a power factor correction. In addition, a portion of the 5% power supply output is phase shifted +90 degrees back to 0 degrees by the IMU CDU load compensation network. The other portion remains at -90 degrees. Both 5% outputs of the IMU-CDU load compensation network supply the 25 IRIG wheel with two phase excitation. The -90 degree output is also used as excitation for the IMU blowers and the CDU motors.

8.1.4 25.6 KCPS POWER SUPPLY. The 25.6 kc power supply module is located in Tray 2 of the PSA. The outputs of this power supply are utilized as encoder excitation (see figure 8-5). The zero and π phase, 25.6 kc, 3 microsecond pulse continuous AGC input is sent to a multivibrator in conjunction with a 27.5 volt dc, B+ voltage. The output of the multivibrator is filtered and amplified. The amplifier output is 2.5 volts, 25.6 kc. The IMU-CDU load compensation network provides a power factor correction for the 2.5 volt signal.

8.1.5 3,200 CPS POWER SUPPLIES. The 3,200 cps power supply consists of three modules located in Tray 1 of the PSA. It is composed of an automatic amplitude control, a 1% power amplifier, and a 5% square wave temperature control power supply (see figure 8-6). The outputs of the 3,200 cps power supply are used for 16 PIP and 25 IRIG ducosyn magnetic suspension and signal generator primary excitation. The 3,200 cps, 5% power supply is used for IMU heater control. In addition to the 27.5 volt DC, B+ voltage, a zero and π phase 7 volt input pulse is applied to a multivibrator in the automatic amplitude control circuitry. From the multivibrator a signal is supplied to the automatic amplitude control circuitry. From the multivibrator, a signal is supplied to the automatic amplitude control and is also supplied to the 5% power amplifier of the temperature control module. The signal from the automatic amplitude control is chopped and filtered and used as an input to the 1% power amplifier, which provides a 2 volt signal. This 2 volt signal is sensed at the signal generator excitation winding and used as a feedback signal to the automatic amplitude control.

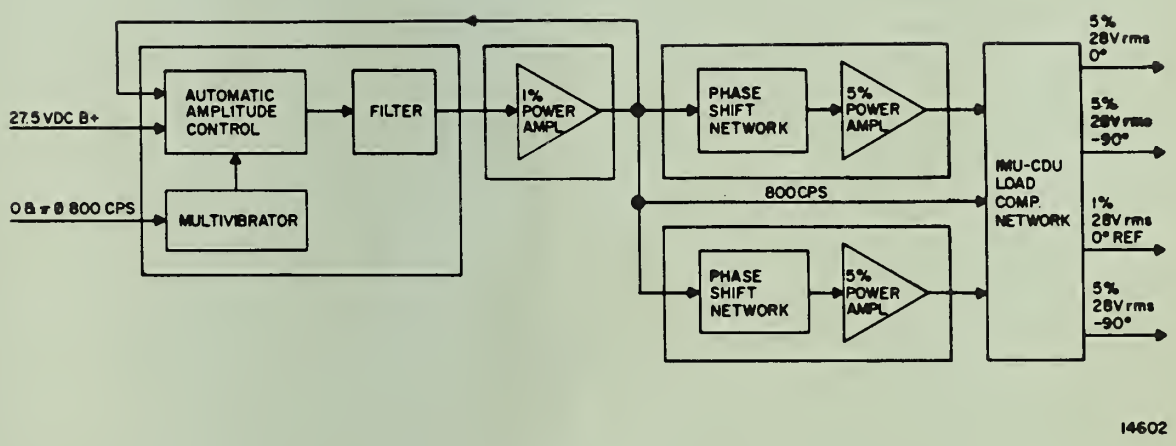


Figure 8-4. 800 CPS Supplies

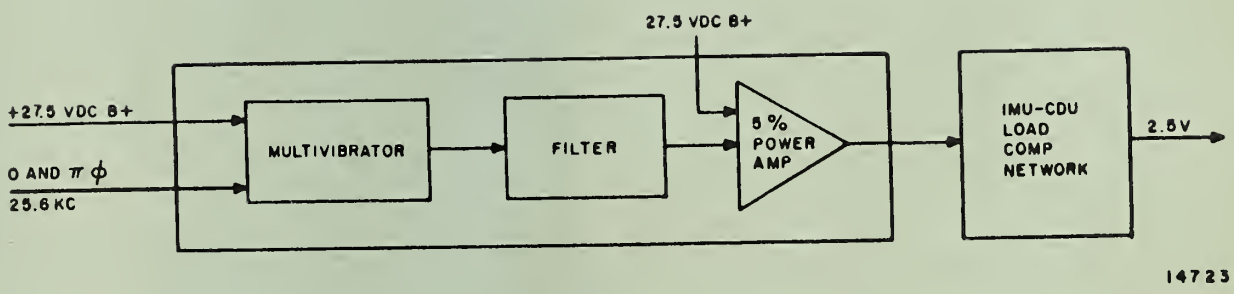


Figure 8-5. 25.6 KCPS Supply

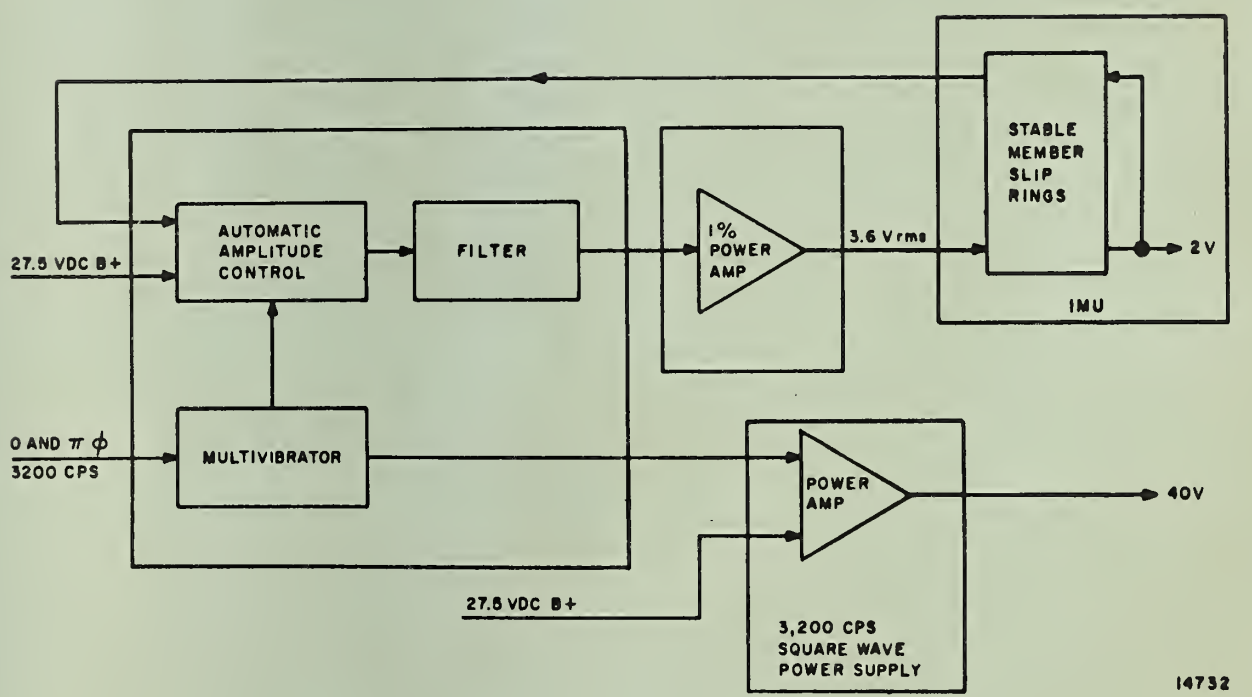


Figure 8-6. 3200 CPS Power Supplies

8.2 POWER AND SERVO ASSEMBLY

The purpose of the power and servo assembly (PSA) is to provide a central mounting point for the majority of the G & N system power supplies, amplifiers and other modular electronic components (see figure 8-7).

The PSA is located in the lower center of the display and control panel above the AGC. It consists of 10 removable trays mounted adjacent to each other and connected to a junction box. A cold plate mounted below the trays provides a means of heat dissipation. Thermal interface material is placed between the PSA trays and the cold plate to provide thermal conduction. A water-glycol coolant from the spacecraft environmental system flows through the cold plate. Encapsulated modules containing the electronics for the G & N system are mounted in two rows on the T-frame backbone of each tray. The T-frame mount is made of magnesium which is machined and electrolytically nickel coated (immersed in zinc, copper flash applied, nickel coated). The modules are mounted on the PSA tray using a guide pin and three screws. The module connector pins are protected by a relieved collar on the module structure. The tray harness is connected to the PSA junction box which an 84 pin male connector. A tapered tongue, angled at 5 degrees and projecting from the junction box end of the tray, compresses the tray on the thermal interface for intimate contact between the tray, thermal interface and cold plate. The tongue also serves as a guide for inserting the tray connector. Each tray is approximately 17-1/2 inches long, 4-1/4 inches high and 2-1/8 inches wide. The PSA trays utilize three wiring harnesses to provide electrical connection. Harness A connects module to module, Harness B connects module to junction box, Harness C connects the modules to a 38 pin female test plug on the front of the PSA tray. This provides the navigator with test point access to the PSA electronics (see figures 8-8 and 8-9). Inertial subsystem electronic modules are located in Trays 1, 2, 3, 4, 5, 7 and 10.

8.2.1 MODULE PACKAGING.

Two types of modules are used in the PSA, the cordwood type and the heat sink type. The cordwood type is used to package lower power electronics and the heat sink type for the high dissipation amplifiers.

8.2.1.1 CORDWOOD PACKAGING.

Cordwood packaging is so designated because module components are stacked between two wafers giving the appearance of a stack of cordwood (see figure 8-10). Nickel ribbon is used to electrically connect components at both ends. A careful selection of temperature and pressure is required to assure uniformity and strength in welding the nickel ribbon to the components. The assembly is enclosed in an aluminum housing and encapsulated in polyurethane foam.

8.2.1.2 HEAT SINK PACKAGING.

The heat sink method of packaging modules allows for maximum dissipation of heat by conduction (see figure 8-11). A block of magnesium is selected to hold preselected electronic components. Holes are drilled into the magnesium block and components are inserted and cemented into the block. Nickel ribbon is used to connect components using printed mylar boards as guides for installing the nickel connecting ribbon. Male connector pins are mounted on one edge. The assembled module is encapsulated in polyurethane foam with a density of six pounds per cubic foot.

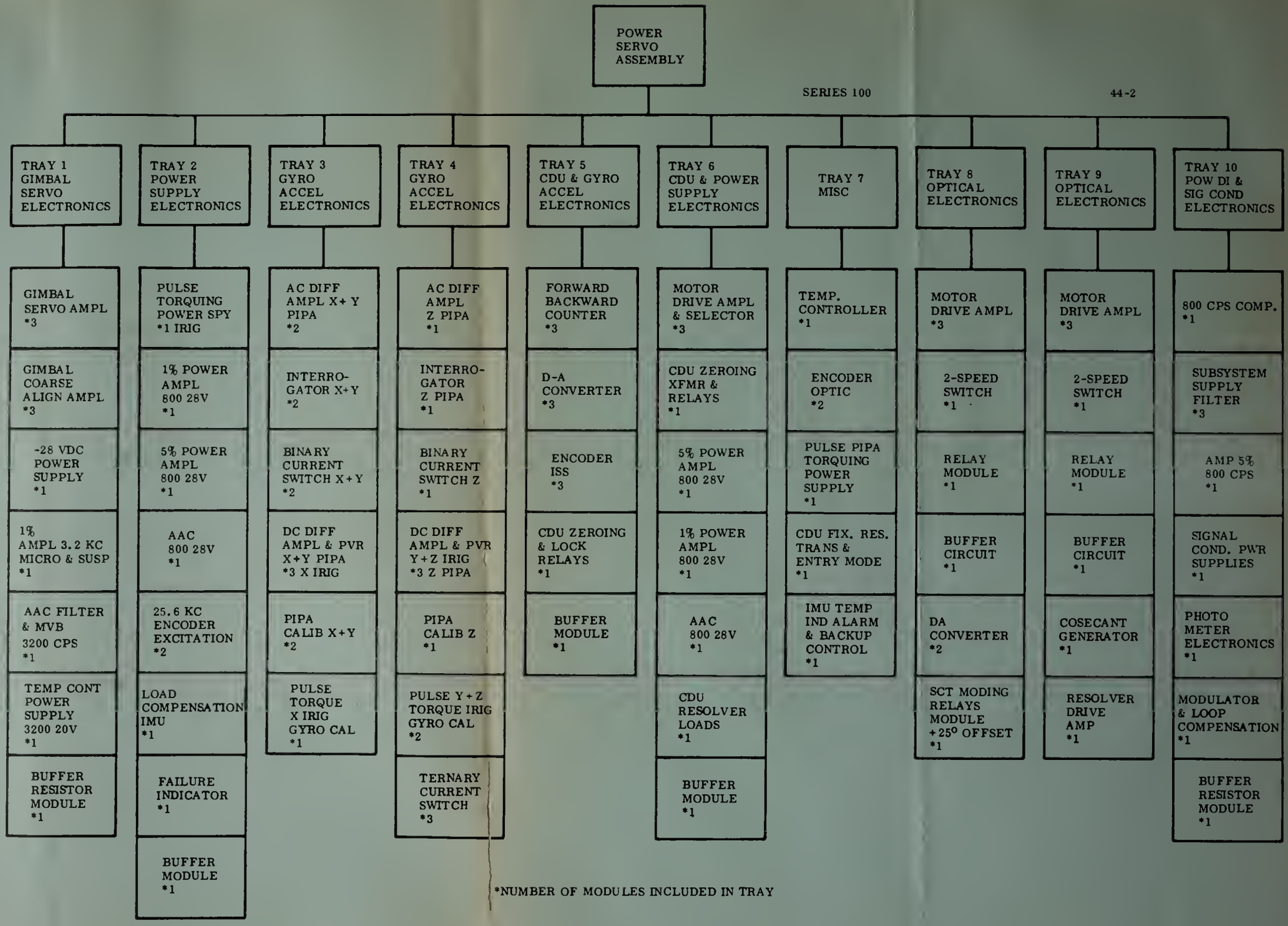

POWER SERVO ASSEMBLY
TRAY 1 GIMBAL SERVO ELECTRONICS
GIMBAL SERVO AMPL *3
GIMBAL COARSE ALIGN AMPL *3
-28 VDC POWER SUPPLY *1
1% AMPL 3.2 KC MICRO & SUSP *1
AAC FILTER & MVB 3200 CPS *1
TEMP CONT POWER SUPPLY 3200 20V *1
BUFFER RESISTOR MODULE *1
TRAY 2 POWER SUPPLY ELECTRONICS
PULSE TORQUING POWER SPY *1 IRIG
1% POWER AMPL 800 28V *1
5% POWER AMPL 800 28V *1
AAC 800 28V *1
25.6 KC ENCODER EXCITATION *2
LOAD COMPENSATION IMU *1
FAILURE INDICATOR *1
BUFFER MODULE *1
TRAY 3 GYRO ACCEL ELECTRONICS
AC DIFF AMPL X+ Y PIPA *2
INTERRO-GATOR X+Y *2
BINARY CURRENT SWITCH X+Y *2
DC DIFF AMPL & PVR X+Y PIPA *3 X IRIG
PIPA CALIB X+Y *2
PULSE TORQUE X IRIG GYRO CAL *1
TRAY 4 GYRO ACCEL ELECTRONICS
AC DIFF AMPL Z PIPA *1
INTERRO-GATOR Z PIPA *1
BINARY CURRENT SWITCH Z *1
DC DIFF AMPL & PVR Y+Z IRIG *3 Z PIPA
PIPA CALIB Z *1
PULSE Y+Z TORQUE IRIG GYRO CAL *2
TERNARY CURRENT SWITCH *3
TRAY 5 CDU & GYRO ACCEL ELECTRONICS
FORWARD BACKWARD COUNTER *3
D-A CONVERTER *3
ENCODER ISS *3
CDU ZEROING & LOCK RELAYS *1
BUFFER MODULE *1
TRAY 6 CDU & POWER SUPPLY ELECTRONICS
MOTOR DRIVE AMPL & SELECTOR *3
CDU ZEROING XFMR & RELAYS *1
5% POWER AMPL 800 28V *1
1% POWER AMPL 800 28V *1
AAC 800 28V *1
CDU RESOLVER LOADS *1
BUFFER MODULE *1
TRAY 7 MISC
TEMP. CONTROLLER *1
ENCODER OPTIC *2
PULSE PIPA TORQUING POWER SUPPLY *1
CDU FIX. RES. TRANS & ENTRY MODE *1
IMU TEMP IND ALARM & BACKUP CONTROL *1
TRAY 8 OPTICAL ELECTRONICS
MOTOR DRIVE AMPL *3
2-SPEED SWITCH *1
RELAY MODULE *1
BUFFER CIRCUIT *1
DA CONVERTER *2
SCT MODING RELAYS MODULE +25° OFFSET *1
TRAY 9 OPTICAL ELECTRONICS
MOTOR DRIVE AMPL *3
2-SPEED SWITCH *1
RELAY MODULE *1
BUFFER CIRCUIT *1
COSECANT GENERATOR *1
RESOLVER DRIVE AMP *1
TRAY 10 POW DI & SIG COND ELECTRONICS
800 CPS COMP. *1
SUBSYSTEM SUPPLY FILTER *3
AMP 5% 800 CPS *1
SIGNAL COND. PWR SUPPLIES *1
PHOTO METER ELECTRONICS *1
MODULATOR & LOOP COMPENSATION *1
BUFFER RESISTOR MODULE *1
*NUMBER OF MODULES INCLUDED IN TRAY

Figure 8-7. PSA Tray Module Location

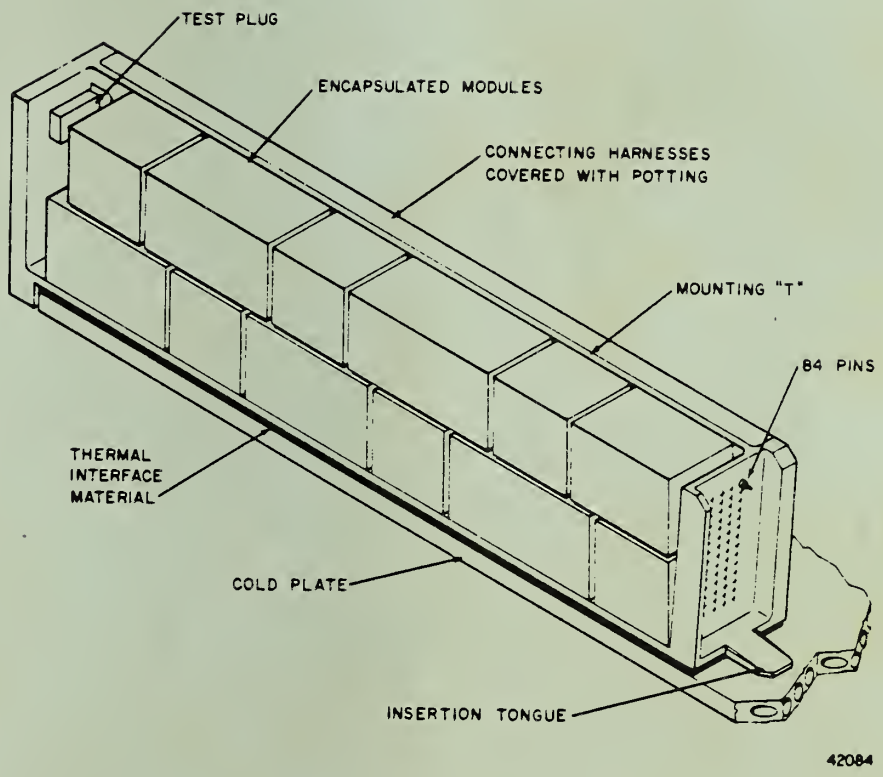


Figure 8-8. PSA Tray

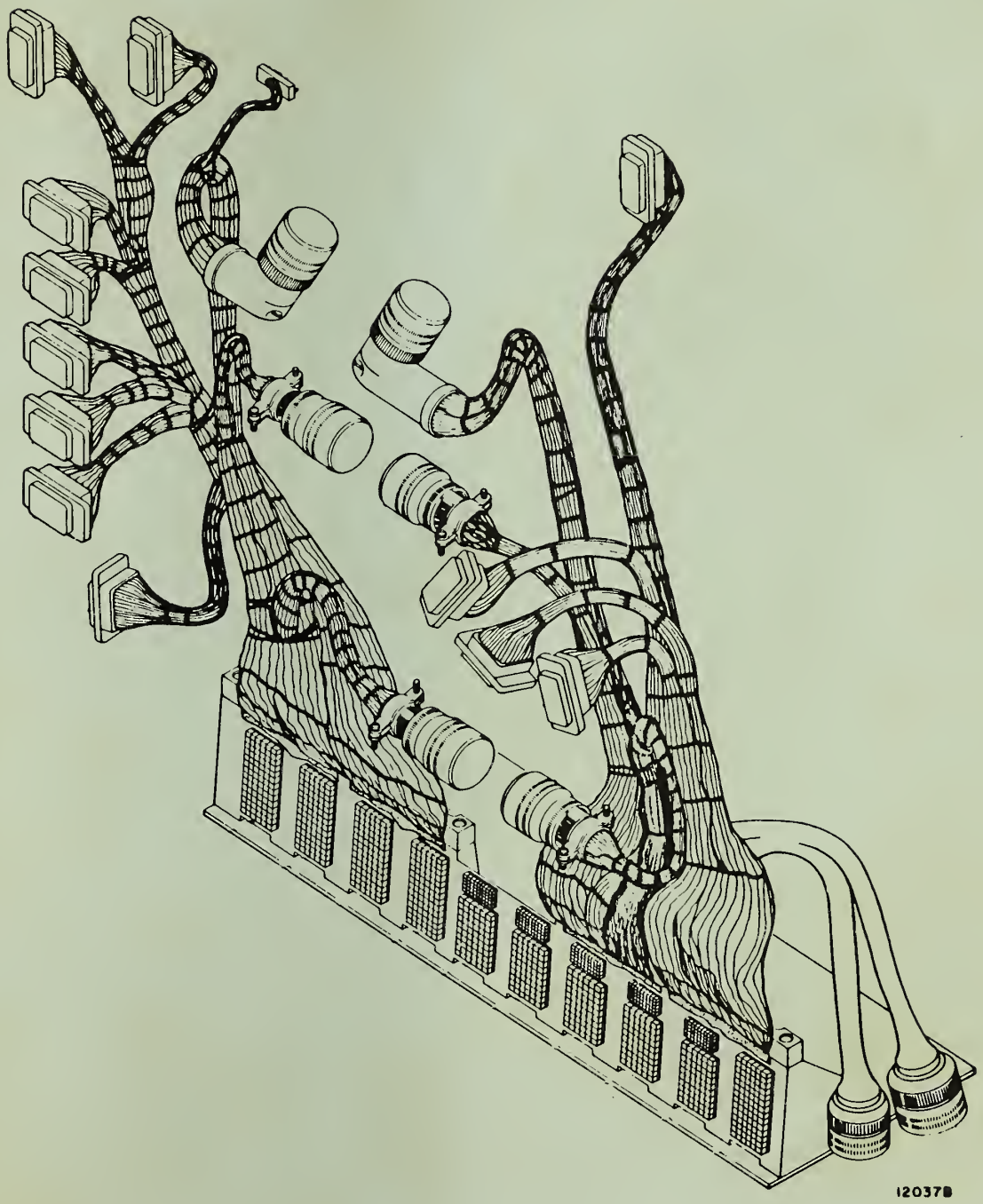


Figure 8-9. G & N Harness and Junction Box

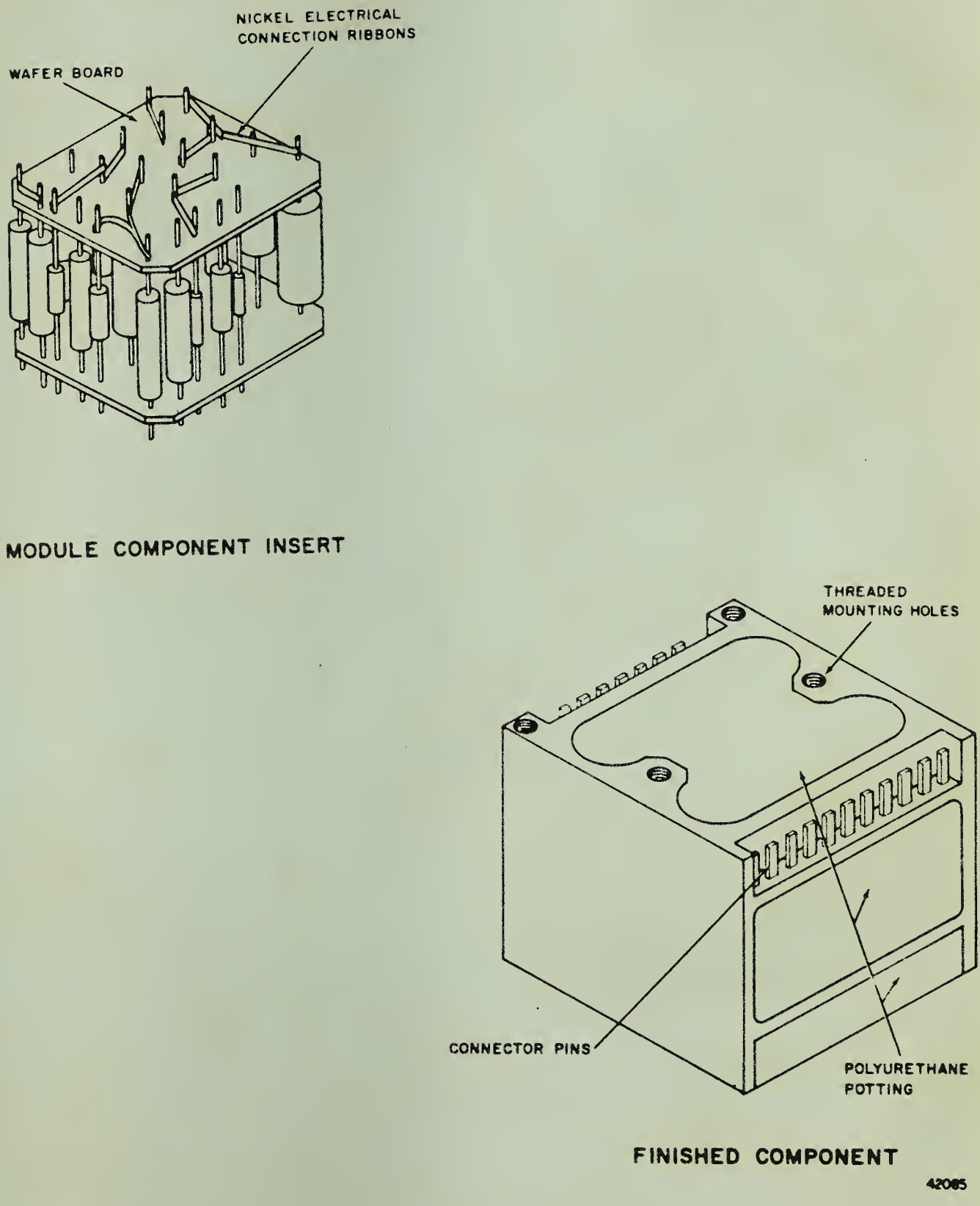


Figure 8-10. Cordwood Module

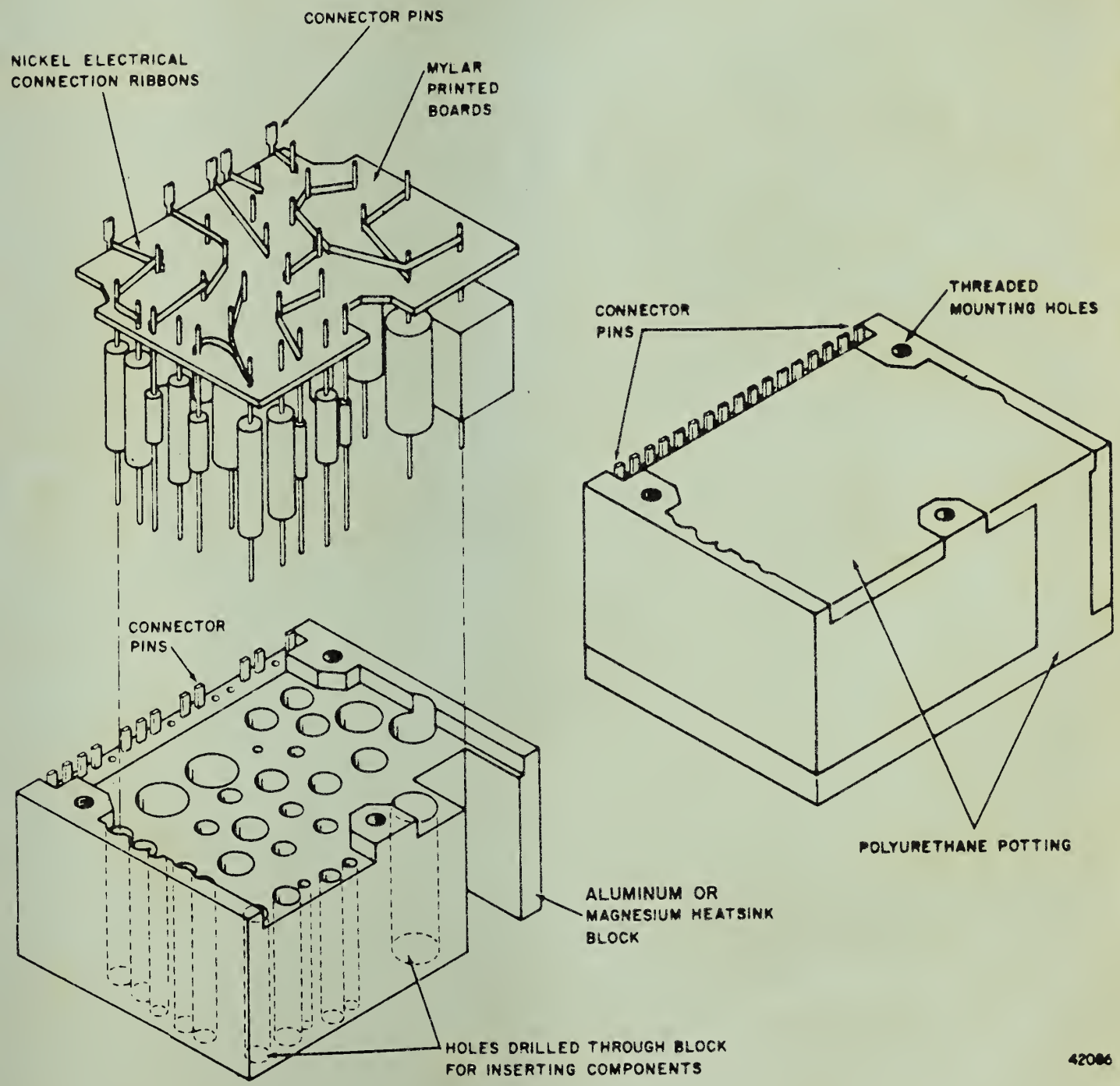


Figure 8-11. Heat Sink Module

The 1%, 800 cps and 5% 800 cps power supplies are mounted in an aluminum heat sink because they require a greater heat dissipating capability and aluminum has a higher thermal conductivity. Otherwise, the construction and packaging of these modules is identical to the heat sink type.

8.3 PSA JUNCTION BOX

The PSA junction box consists of connectors mounted in an encapsulated bracket attached to the PSA cold plate (see figure 8-9). The junction box connectors allow for electrical connection between the PSA electronics and the rest of the G & N system via the G & N harness. With the cabling leading from its connectors, the junction box forms an integral part of the display and control harness assembly.

8.4 SUMMARY

The inertial power supplies, located in the PSA are used primarily to supply DC and AC power to the ISS. DC power is supplied at -28V, 120V, 32V and 12V. AC power is supplied at frequencies of 800 cps, 25.6 kcps and 3200 cps as well as 3200 pps square wave.

AC references are provided by the computer although self-contained frequency sources are found in the AC supplies.

The PSA provides a central mounting point for the power supplies, as well as amplifiers and relays. It consists of 10 removable trays of modules which are cooled by the spacecraft environmental system. All modules are potted to withstand high "g" environment.

REVIEW QUESTIONS FOR SECTION VIII

1. The following questions are either True or False. Indicate which and if False, explain.

   a. If the computer fails all ISS ac power supplies will fail due to the loss of reference frequency.

   b. The IMU standby-operate switch controls all ISS power supplies.

   c. The 120 vdc, 32 vdc and 12 vdc voltages are all supplied by the pulse torque power supply.

   d. The PSA is convection (air) cooled.

2. Which power supply(ies) is(are) regulated? Draw the block diagram for these supplies.

3. Describe the types of module packaging methods on the PSA and explain the reasons for the difference.

SECTION IX

SIGNAL MONITORING AND CONDITIONING

INTRODUCTION

This section describes the ISS signal monitoring and detection circuitry and hardware as well as the signal conditioning assembly which processes G & N signals to make them acceptable to the downlink telemetry system.

9.1 SIGNAL MONITORING AND DETECTION

The signal monitoring and detection circuits provide a means of remotely monitoring the inertial subsystem circuits. The signals can be displayed to the astronauts and, after conditioning, relayed as a telemetry signal to a ground station. These signals can be used to isolate an equipment malfunction for maintenance purposes.

9.1.1 FAILURE DETECTION. The purpose of the failure detection circuit is to inform the astronaut and the AGC of the following power losses or incorrect signals in the G & N system (see figure 9-1).

a. Loss of 3,200 cps ducosyn excitation.

b. Loss of 800 cps wheel excitation.

c. Stabilization loop errors.

d. Loss of CDU motor excitation.

e. CDU loop errors.

f. PIPA loop errors.

g. AGC fail.

h. AGC power supply fail.

i. Loss of 25.6 kc encoder excitation.

A primary guidance and navigation system error lamp on the condition annunciator indicates when the IMU failure, CDU failure, or accelerometer failure signals are being sensed. The navigator can observe the P.G.N.S. error lamp and possibly correct the malfunction. The error detection signals also are applied to the AGC to prevent miscalculations.

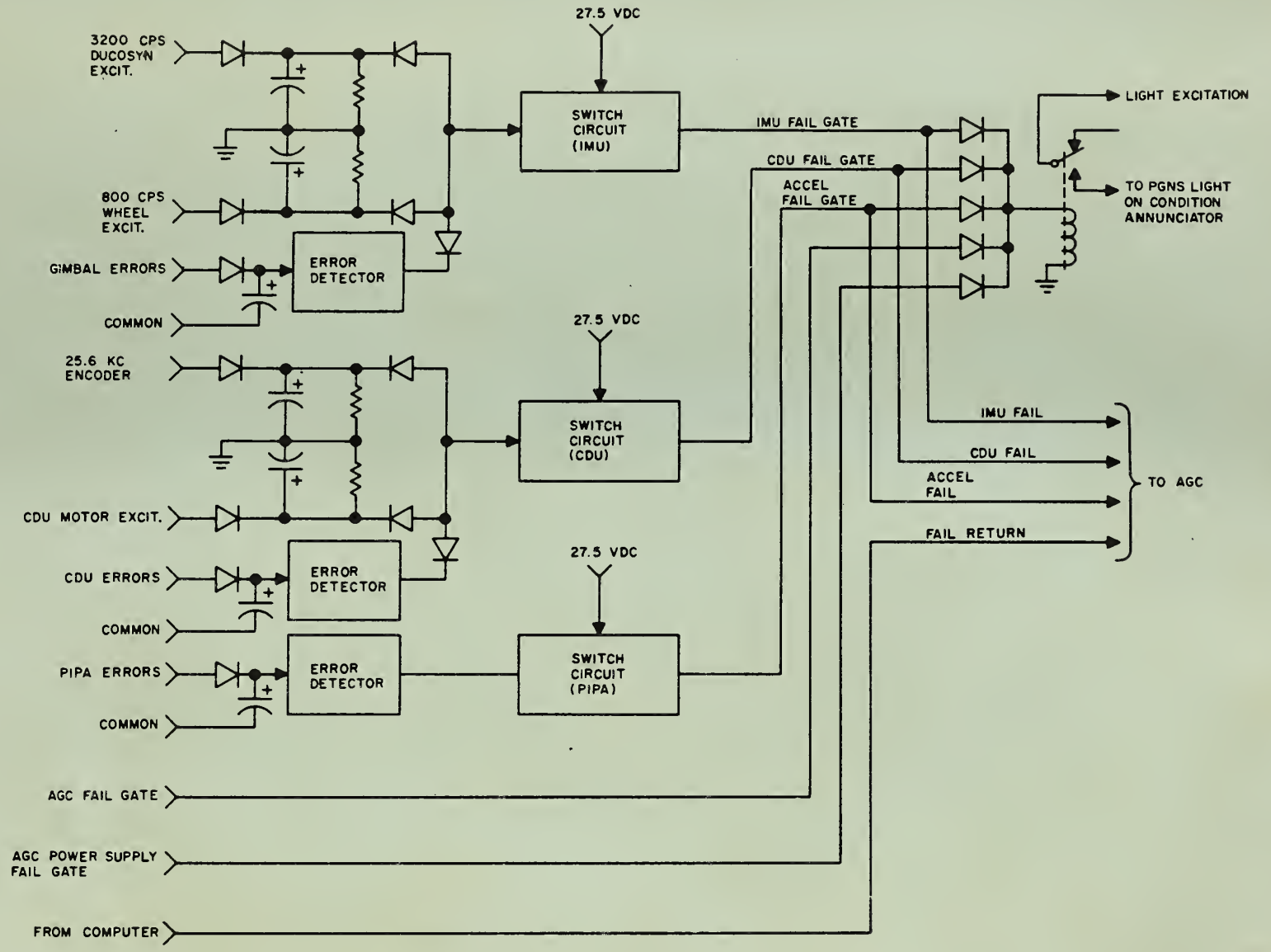


Figure 9-1. Failure Detection Circuitry

Since the operation of the IMU, CDU and PIPA error detection circuits are similar, only the operation of the IMU error detection circuit is described. (See figure 9-1). During normal operation when all input signals are present and within specifications, the transistorized IMU switch circuit is cut off. The input capacitors are charged to a positive value equivalent to the excitation voltages, which reverse-biases two diodes. This reverse bias prevents the switch circuits from being energized. If either the 3,200 cps microsyn excitation or the 800 cps wheel excitation voltage is not present, one of the input capacitors will discharge to forward-bias one of the diodes. The forward-biased diode turns on the IMU switch circuit by causing a 27.5 volt dc short through the switch to energize an error detect relay. When this relay is energized, 6 volt dc excitation voltage is applied to the P.G.N.S. lamp on the Condition Annunciator. Simultaneously, an IMU failure signal will be supplied to the AGC until the 3,200 cps or 800 cps excitation voltages are within the specified limits.

The switch circuit also will be turned on if any of the gimbal error signals become too large. An excess gimbal error signal will be detected by the gimbal error detector and the output of the gimbal error detector will turn on the switch circuit. The switch circuit shorts the error detect relay to light the error detect lamp. When the AGC fail gate or power supply fail gate signal is generated, it is routed through the failure detection circuit to energize a relay which causes the error detect lamp to light.

9.1.2 CONDITION ANNUNCIATOR. The condition annunciator located on the lower D & C receives ISS and AGC malfunction signals and displays the observed malfunctions.

Figure 9-2 shows the annunciator and its display capabilities. The fail indications of the condition annunciator are as follows:

PGNS - primary guidance and navigation system failure, indicating AGC, IMU, ACCEL., or CDU Malfunction.

Computer Power Failure - indicates loss of +13 volts, +3 volts, or +28 volt power in the AGC.

IMU Fail - IMU servo failure of -28 V, 3200 cps, or wheel power failure.

CDU Fail - Loss of encoder excitation, motor excitation or CDU-IMU error.

Accel. Fail - Accelerometer error failure.

Gimbal Lock - indicates outer to middle gimbal angle in excess of $\pm 60^{\circ}$.

IMU Temp - indicates temperature deviation in excess of $\pm 4^{\circ}$.

Zero Encoder - indicates during CDU zeroing operation.

IMU delay - indicates 100 second delay during IMU turn on.

Master alarm - indicates failure of one of the major spacecraft systems.

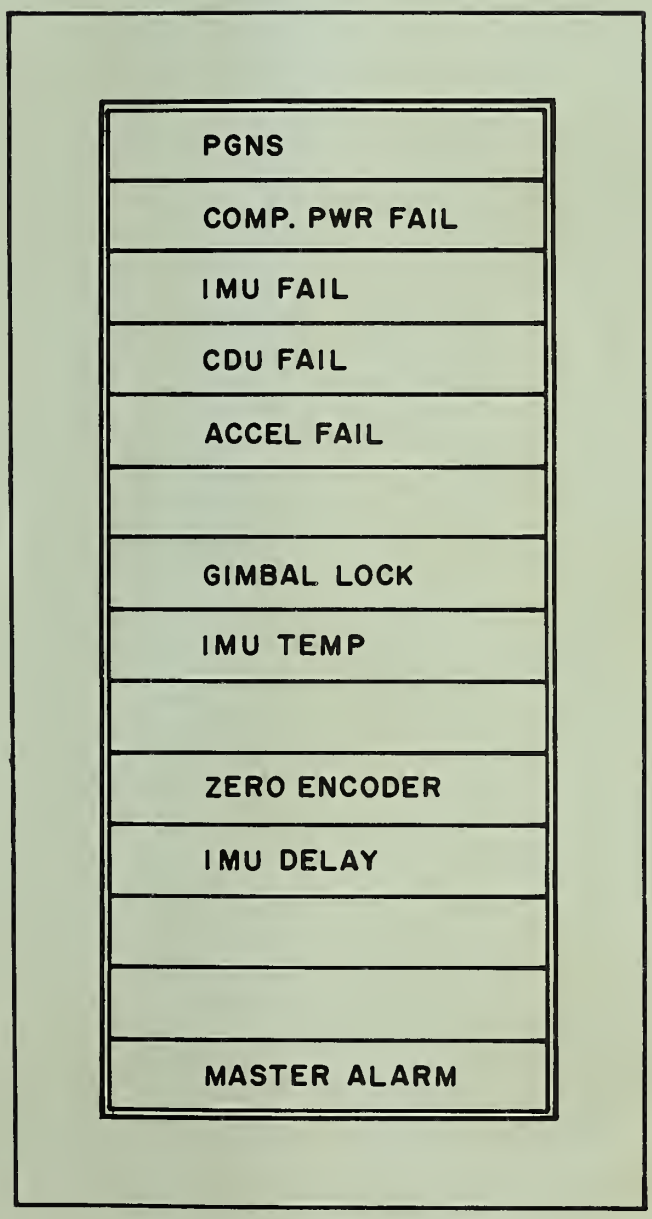


Figure 9-2. Condition Annunciator

Some signals from the failure detect circuitry are routed directly to the condition annunciator to light the PGNS lamp. These signals (IMU Fail, CDU Fail, Accel Fail) also go to the computer. The computer determines if a failure actually exists or whether the indication is the result of some action being taken by the operator or AGC. If the failure is verified, the appropriate lamp will then be lit by a computer signal to the annunciator. Some signals such as gimbal lock, are hard wired to the annunciator from the circuitry involved. IMU temp and IMU delay are also directly connected. The zero encoder lamp is lit as a computer program function during that mode of ISS operation.

9.2 SIGNAL CONDITIONER ASSEMBLY

The signal conditioner assembly (signal conditioner) receives 34 G&N signals and conditions them to a form acceptable to the airborne (pulse code modulated) PCM multiplexer or encoder. Four additional signals, which do not require further conditioning are routed through the signal conditioner to the multiplexer. The multiplexer then transforms the conditioned signals into a form suitable for telemetry transmitter modulation. The signal conditioner also provides isolation between the component or circuit being monitored and the telemetry system. The signal conditioner consists of six different modules and a mounting frame assembly on which the modules are mounted. The complete signal conditioner is mounted to the rear of the G&N system station in the spacecraft.

9.2.1 SIGNAL CONDITIONER MODULES. Each type of module is designed to condition a particular type of G & N system signal. The six conditioning modules are:

a. Torque motor signal conditioner.

b. CDU resolver signal conditioner.

c. Scaling signal conditioner.

d. IRIG and PIPA signal conditioner.

e. Gimbal signal conditioner.

f. Optics signal conditioner.

The signal conditioner receives 20 volt dc, B+ supply voltage and 2.5 volt dc conditioning bias voltage from the signal conditioner power supply in tray 10 of the PSA. The 20 volt dc B+ is applied to each module except the optics signal conditioner. The 2.5 volt dc bias voltage is connected in series with the outputs of all modules except the scaling signal conditioner so that the 2.5 volt dc bias low becomes the common low to the telemetry system (see figure 9-3). The 2.5 volt dc bias high is connected to the signal low of each module and becomes the reference point for the 0 to 5 volt signal outputs of the signal conditioner modules. In this manner a zero phase ac signal, after conditioning, may be represented as a dc voltage value above the 2.5 volt reference. A pi phase signal, after conditioning, may be represented as a dc voltage value below the 2.5 volt reference. Bipolar dc signals from the G & N system which may be positive or negative and have a zero volt reference, may, after conditioning, be represented in a similar manner. Positive voltages may be represented as a voltage value below the 2.5 volt reference.

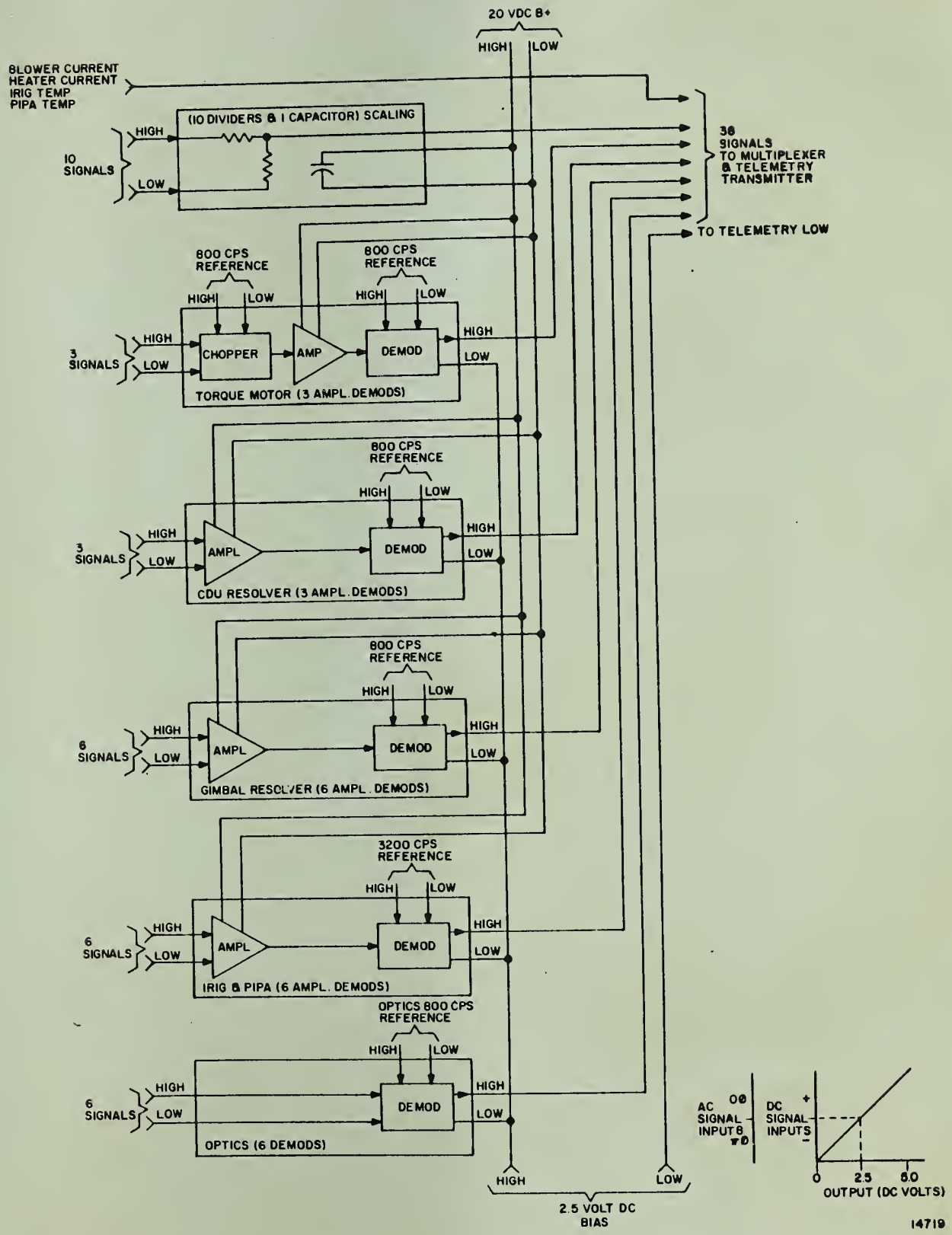


Figure 9-3. Signal Conditioner

9.2.2 SIGNAL CONDITIONER POWER SUPPLIES. The signal conditioner power supply module consists of three separate power supplies which provide 2.5 volt dc conditioning bias voltage and 20 volt dc B+ supply voltage to the signal conditioner assembly. The module also provides 28 volts dc for IMU pressure transducer excitation. The signal conditioner power supply module is in tray 10 of the PSA (see figure 9-4).

9.2.3 INPUTS. The signal conditioner power supply inputs are optics 28 volts dc, IMU 28 volts dc and 115 volts 400 cps. The 115 volt, 400 cps input is applied to a transformer that has two output windings. One output of the transformer is rectified and filtered to provide the 28 volt dc pressure transducer supply. The second transformer output is rectified, filtered and applied to a series regulator circuit. The output of the regulator is attenuated by a voltage divider to provide the 2.5 volt dc conditioning bias voltage. The optics 28 volts dc and the IMU 28 volts dc are applied to the 20 volt dc signal conditioner B+ power supply circuit through isolation diodes so that the power supply circuit will continue to function as long as either 28 volt dc input is present. The 28 volt dc input is applied across a zener diode and resistor to provide a reference to a regulator circuit whose output provides the signal conditioner assembly B+ supply.

9.2.4 TORQUE MOTOR MODULE. The torque motor signal conditioner module conditions the inner, middle and outer gimbal torque motor signals to a representative 0 to 5 volt dc voltage. The module contains three identical signal conditioning circuits. Each circuit contains a chopper, an ac amplifier, and a phase sensitive demodulator. The input signals, which may vary from approximately +7 to -7 volts dc, are received from the torque drive amplifiers.

The incoming dc signal is first applied to a chopper circuit consisting of two integrated chopper semiconductors. The chopper modulates an 800 cps square wave reference with the dc input. The modulated square wave, which is representative of the magnitude and polarity of the dc input, is transformer-coupled to the ac amplifier. The amplified signal is transformer-coupled to a phase sensitive demodulator circuit consisting of two dual emitter chopper/switch transistors. The switching action of the transistor pairs in both the chopper circuit and the demodulator circuit is controlled by a switch drive circuit consisting of an 800 cps reference signal applied through a transformer to the base-collector junction of each transistor. The switch drive circuit alternately turns on one transistor while the other one is turned off. The output of the demodulator is a pulsating dc signal whose magnitude and polarity are dependent on the magnitude and polarity of the input signal. The output of the demodulator is filtered and then biased at 2.5 volts dc. The output of the torque motor signal conditioner, which could vary from +2.5 volts to -2.5 volts at a zero reference, will, as a result of the 2.5 volt reference, remain in a 0 to 5 volt range.

9.2.5 CDU RESOLVER MODULE. The CDU resolver signal conditioner module conditions the inner, middle and outer gimbal CDU 1X resolver error signals into a representative 0 to 5 volts dc. The module contains three identical signal conditioning circuits, each of which contains an amplifier and a phase sensitive demodulator. The inputs to the amplifier and demodulator are transformer-coupled. The operation of the demodulators is similar to the demodulator in the torque motor signal conditioner module. The magnitude and polarity of the CDU resolver demodulator, however, are dependent on the magnitude and phase of the input signal, respectively.

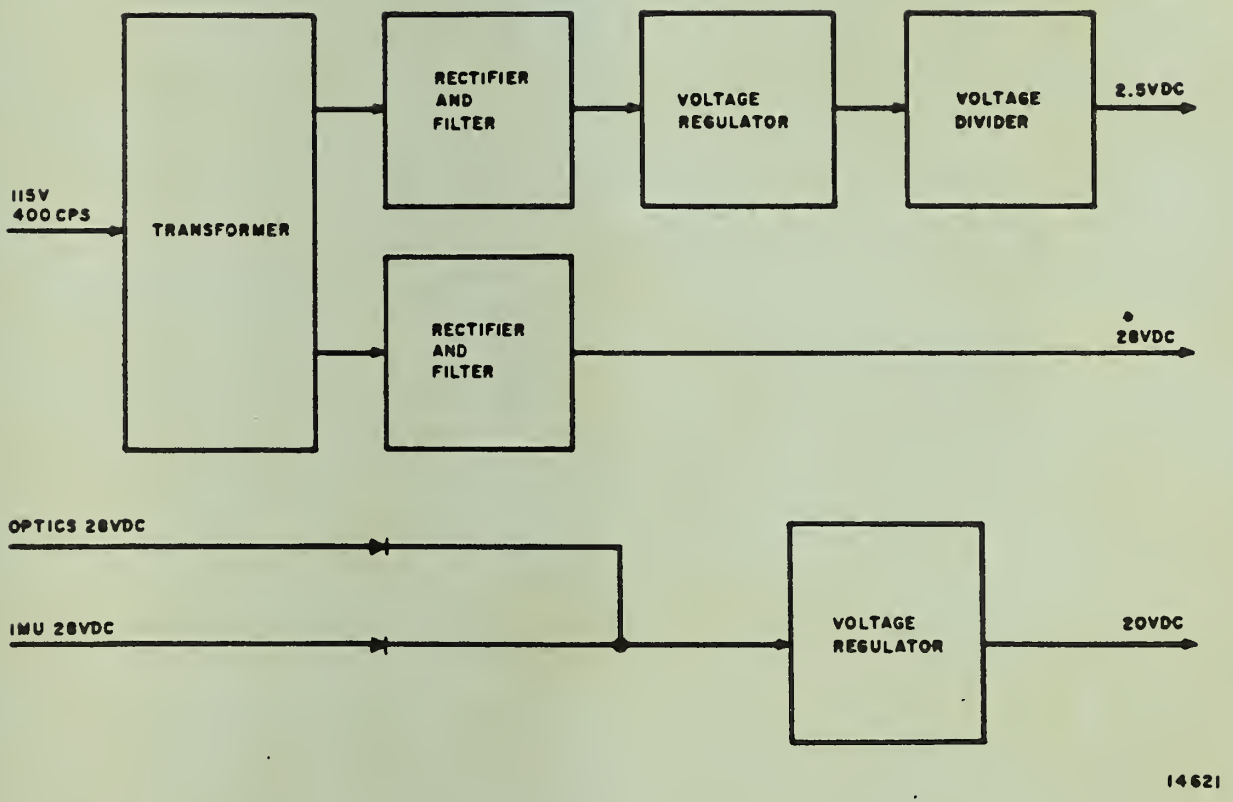


Figure 9-4. Signal Conditioner Power Supplies

9.2.6 SCALING MODULE. The scaling signal conditioner module conditions ten discrete dc signals which require only voltage division. The voltage divider circuits drop the input signals to the proper 0 to 5 volt level. The scaling signal conditioner module also contains a capacitor which filters the 20 volt dc, B+ supply voltage.

9.2.7 IRIG AND PIPA MODULE. The IRIG and PIPA signal conditioner module conditions six signals. Three signals are the three 16 PIP ducosyn signal generator outputs. The other three signals originated at the 25 IRIG signal generators. As a result of the resolution of the X and Z gyro signals, the three signals represent the Y gyro and inner gimbal error, the middle gimbal error and the outer gimbal error. The module contains six identical signal conditioning circuits, each containing an amplifier and a phase sensitive demodulator. The demodulator is similar in operation to the demodulators previously discussed. The IRIG and PIP demodulators, however, require a 3,200 cps reference. The 3,200 cps reference is applied to six modulator circuits through a buffer transformer and amplifier circuit which provides isolation between the signal conditioner module and the 2 volt, 3,200 cps source.

9.2.8 GIMBAL RESOLVER MODULE. The gimbal resolver signal conditioner module conditions the signals from the sine and cosine windings of the inner, middle and outer gimbal 1X resolvers. The module contains six signal conditioning circuits, each containing an amplifier and a phase sensitive demodulator. The operation of the circuits is similar to the CDU resolver signal conditioning circuits.

9.2.9 OPTICS MODULE. The optics signal conditioner module conditions signals from the shaft and trunnion CDU MDA's, the sextant trunnion and controllers. The module contains six signal conditioning circuits, each of which is a phase sensitive demodulator. The reference for the demodulators is from the optics 800 cps, 1% power supply.

9.3 SUMMARY

The signal monitoring and detection circuits provide the means for measuring and displaying to the astronauts several ISS circuit malfunctions. These enable maintenance and malfunction isolation.

The signal conditioner converts G & N signals to levels acceptable to the telemetry encoder. A power supply located in the PSA drives the conditioner. Conditioned signal levels are 0 to 5 volts dc.

REVIEW QUESTIONS FOR SECTION IX

1. T F Telemetry inputs are supplied by the signal conditioner as a 0 - 5 volt ac signal.

2. What are the names and functions of the six signal conditioner modules?

3. Describe the failure detect circuitry. Show outputs to the AGC and condition annunciator.

4. How would the IMU fail lamp be turned on by the system in case of an ISS failure input IMU fail switch circuit?

SECTION X

INTRODUCTION TO THE OPTICAL SUBSYSTEM

INTRODUCTION

This section classifies the OSS equipment into functional blocks and explains each block.

10.1 OSS PURPOSE

The optical subsystem enables the astronaut to make optical sightings on celestial objects by means of a telescope and sextant. These sightings are used in updating this spacecraft's position and velocity and in aligning the IMU. The celestial bodies serve as the primary reference for navigation of the spacecraft when using the G&N System.

The taking of optical sightings is a semi-automatic operation and requires the astronaut to point the optical instruments. If the celestial objects cannot be acquired by operating the optical controls alone, the astronaut must change the attitude of the spacecraft by commanding roll, pitch and yaw motion with the spacecraft rotation control.

At the instant the optical sighting is taken, the time of sighting, the angles of the optical instruments and the IMU gimbal angles if the ISS is enabled, are recorded by the AGC. Data pertaining to the location of the celestial objects and programs for navigational calculations have been stored in the AGC. The navigational measurements can be accomplished during earth orbit by measuring the angles to landmarks with the telescope. Midcourse navigation is accomplished by measuring the angle between a landmark and a star with the sextant. The IMU is aligned during flight by measuring the angle between the navigation base and each of two stars with the sextant. Optical sighting data is also used in IMU prelaunch alignment.

In case of a failure in the optics electronics, the astronaut may be required to operate the telescope manually with the universal tool and read the angles off counters on the telescope axes.

10.2 OSS EQUIPMENT

The optical subsystem consists of the following equipment (see figure 10-1):

a. Navigation Base (NB)

b. Optical Assembly

c. Coupling Display Unit (CDU) (two required)

d. Power Servo Assembly (PSA) (portions)

e. G&N Indicator Control Panel (portions)

f. Optical Panel

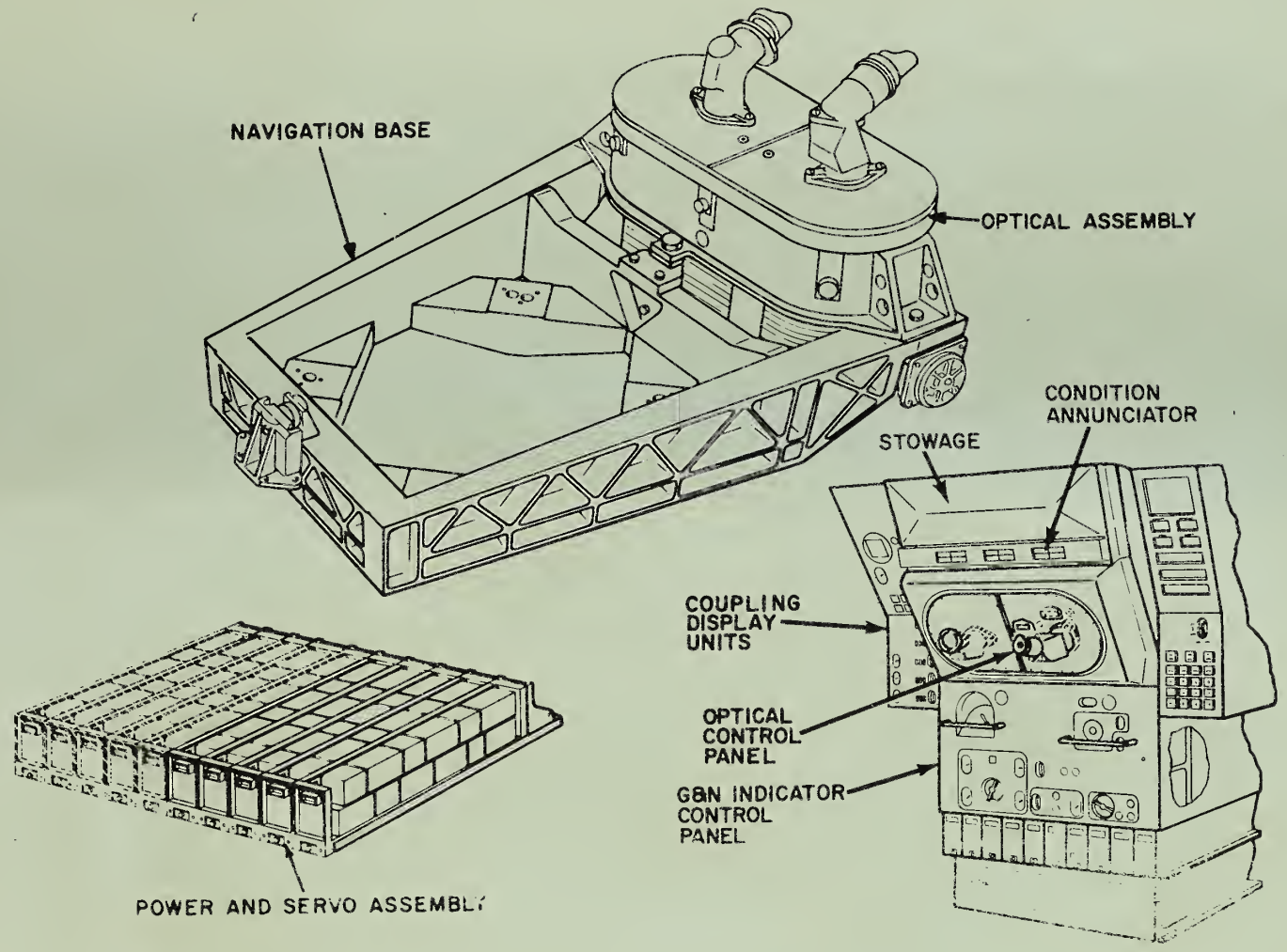


Figure 10-1. Optical Subsystem Equipment

10.3 OSS FUNCTIONAL BLOCKS

For the purpose of this explanation, the optical subsystem equipment is divided into functional blocks as shown in figure 10-2. The operation and interrelationship of these blocks are described in the following paragraphs.

10.3.1 NAVIGATION BASE. The navigation base is used as a holding fixture to provide a rigid support of the optics with respect to the IMU. The optics are fixed in precise alignment to the navigation base. Flexible sealing at the spacecraft opening is supplied by a bellows assembly around the optical instruments.

10.3.2 TELESCOPE. The telescope is mounted beside the sextant to permit parallel lines of sight through an opening in the spacecraft. The telescope, with its large field of view, is used as an aid to the sextant for coarse acquisition in midcourse flight and for measuring angles to landmarks during earth orbit.

The telescope is a refracting type and has magnification power of 1X with a field of view of 60 degrees. The telescope has two degrees of rotational freedom with the shaft axis and trunnion axis defining the axes of rotation. Continuous rotation is physically possible about the shaft axis, which is fixed with respect to the spacecraft, but in operation, is limited to the shaft movement of the sextant. Rotation about this axis defines the shaft angle (A_S). Continuous rotation is also possible about the trunnion axis, which is perpendicular to the shaft axis. Rotation about this axis defines the trunnion angle (A_t). A prism located on the trunnion axis, is rotated to reflect the image into the objective lenses of the telescope. Because of obstructions caused by spacecraft airframe, the line of sight (LOS) of the trunnion has a useful range of approximately 53 1/2 degrees. By rotating the telescope about the trunnion and shaft axes, a maximum field of approximately 107 degrees can be viewed. To control the motion of the telescope line of sight, shaft and trunnion drive rates are normally supplied to the sextant drive circuits, which position the sextant shaft and trunnion. During normal operation, the shaft and trunnion of the sextant and telescope are slaved together. To acquire objects outside the 107 degree field of view, the attitude of the spacecraft must be changed. The shaft and trunnion angles can be read directly from the telescope by counters mounted on the face of the optical panel. A tool is also provided so that the trunnion and shaft angles can be manually positioned.

10.3.3 SEXTANT. The sextant is more precise than the telescope and is used primarily during the midcourse phase for measurement of angles between a landmark and a star or for sighting each of two stars for fine alignment of the IMU. The sextant has two lines of sight, landmark and star. The landmark line of sight (landmark LOS) is fixed with respect to the spacecraft. To align the landmark LOS to a particular landmark, the attitude impulse control, which makes small changes in the spacecraft attitude rates, and the spacecraft rotation control are used. The star line of sight (star LOS) has two degrees of freedom and operates similarly to the telescope in that it can scan a field of approximately 107 degrees. Both the star LOS and landmark LOS have a 1.8 degree field of view and a magnifying power of 28X. When looking through the sextant eyepiece, objects in the star and landmark lines of sight are superimposed. By obtaining a coincidence of a star and a landmark, the angle between the two can be measured.

10.3.4 SHAFT AND TRUNNION DRIVE. The telescope and sextant drive circuits perform similar functions; they reposition their respective shaft and trunnion axes at the commanded rate. Sextant shaft and trunnion movement can be commanded by the sextant hand controller or the computer. The telescope shaft always follows the sextant shaft. The telescope trunnion can be commanded by mode switching to: (1) follow the sextant trunnion, (2) drive to 0 degrees, or (3) drive to 25 degrees.

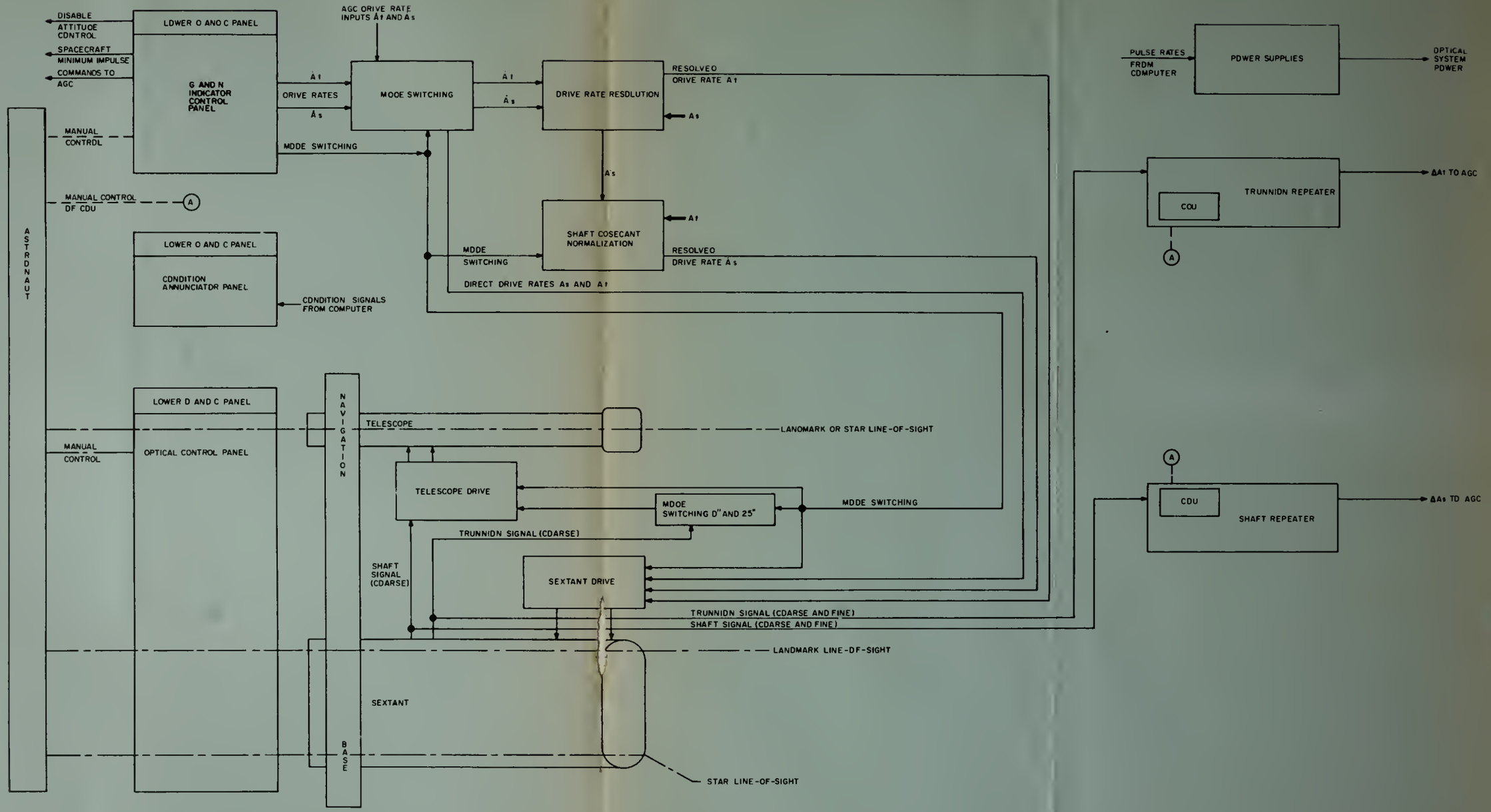


Figure 10-2. Optical Subsystem Interface

10.3.5 SHAFT AND TRUNNION REPEATERS. The shaft and trunnion repeater circuits follow the sextant shaft and trunnion and display the shaft and trunnion angles. The repeater circuits include the shaft and trunnion coupling display units (CDU's) and their associated electronics. A coarse-fine resolver system is used between the sextant assembly and the shaft and trunnion CDU's. Any error signal, resulting from a difference between the CDU resolver angles and the sextant shaft or trunnion angles, drives the shaft or trunnion CDU to repeat the sextant angles. Both CDU's have a digital pickoff for transmitting changes in the shaft or trunnion angles to the AGC.

10.3.6 DRIVE RATE RESOLUTION CIRCUIT. The purpose of this circuit is to resolve the sextant hand controller drive rates so the image motion in the eyepiece (left-right for large trunnion angles and up-down) is independent of the shaft angle. Without this resolution, the direction of image movement in response to the sextant hand controller would vary and depend upon the shaft angle. The drive rates are routed through the drive rate resolution circuit by mode switching controlled from the G&N indicator control panel during the manual resolved mode. The resolution is accomplished by a resolver contained in the shaft CDU.

10.3.7 SHAFT COSECANT NORMALIZATION CIRCUIT. For easier optical sightings, it is desirable that the rate of image motion (left-right or up-down) in the eyepiece be constant for a given rate input from the sextant hand controller. Since the trunnion angle affects this rate, a resolver in the trunnion repeater CDU and a cosecant amplifier are used to resolve the image motion rate. The shaft cosecant normalization circuit conditions the shaft drive rates only and is connected to the sextant hand controller by switching the optics into the manual resolved mode.

10.3.8 MODE SWITCHING. The mode switching is controlled from the G&N indicator control panel. The switching is performed by relays and selection switches.

10.3.9 DISPLAY AND CONTROL SUBSYSTEM OPERATIONS. The panels used by the optical subsystem to display and control subsystem operation and the panel functions are as follows:

1. The optical panel provides: (a) a mount for the optical eyepieces, (b) manual control of the telescope shaft and trunnion angles, and (c) readouts of the telescope shaft and trunnion angles.

2. The G&N indicator control panel:

   a. Provides controls for switching optical subsystem modes.

   b. Issues mark commands to the AGC to define the time of measurement and to record shaft and trunnion angles at the time of the discrete.

   c. Issues mark rejects to the AGC to reject time and angle information which was recorded as a result of a mark command.

   d. Supplies commands to the stabilization and control system to enable attitude impulse control of the spacecraft.

   e. Controls the positioning of the optical unit by generating drive rates.

10.3.10 POWER SUPPLIES. The 28 volt 800 cps optics supply and 2.5 volt 25.6 KC encoder excitation supply, packaged in the PSA, are required to operate the optical subsystem.

The power supplies operate from 28 volt dc prime power and pulse rates from the AGC. The outputs of the power supplies are monitored for malfunction detection indications which are supplied to the AGC.

10.4 SUMMARY

The OSS is used to determine spacecraft position and attitude by use of the optical unit. The optical unit consists of a telescope and sextant. The telescope is a wide angle, low power unit used for coarse acquisition of celestial bodies. The sextant is a dual line of sight, narrow field of view, high power of magnification unit used to finely acquire celestial bodies. The OSS provides the CSS with shaft and trunnion angles from which the AGC calculates spacecraft position and orientation.

REVIEW QUESTIONS FOR SECTION X

T F 1. Two basic optical subsystem functions are navigation and IMU alignment sightings.

T F 2. The sextant is a dual line of sight optical instrument.

T F 3. The sextant is used for coarse acquisition of the celestial bodies.

T F 4. The telescope has a large field of view.

T F 5. The telescope is used for coarse acquisition of celestial bodies.

T F 6. The telescope is a dual line of sight optical instrument.

T F 7. The optical CDU's are used to drive the sextant and telescope.

SECTION XI

OPTICAL SUBSYSTEM EQUIPMENT DESCRIPTION

INTRODUCTION

This section describes the G&N equipment associated with the optical subsystem.

11.1 OPTICAL UNIT ASSEMBLY

The optical unit assembly consists of (1) the optical base, (2) the scanning telescope (SCT), and (3) the sextant (SXT). The position of the optical unit assembly in the spacecraft and the scanning limits of the optics are illustrated in figures 11-1 and 11-2. These limits are imposed by the spacecraft structure and the optical doors which open to expose the instruments to space. For all practical purposes, the total field of view of the SXT and SCT can be considered to be 107°.

11.1.1 OPTICAL BASE. The optical base section houses most of the electro-mechanical components of the SCT and SXT. For the SCT shaft and trunnion axes, these components include: motor generators, gear trains, resolvers and mechanical counters; for the SXT shaft axis, these components include a motor generator, gear box and a resolver. Cutaway drawings of the scanning telescope and sextant, including the optical base equipment, are shown in figures 11-3 and 11-4, respectively. The optics underpanel assembly is fastened to the optical base. It contains (1) windows for viewing the SCT shaft and trunnion mechanical counters, (2) an input adapter for using the universal tool for operating the SCT manually and (3) the SCT prism housing assembly and eyepiece assembly. The panel also contains the mounting for the eyepiece window and the mounting for the SXT eyepiece assemblies. Attached to the exterior of the optical base are the three mounting points which are mated to the navigation base.

11.1.2 SCANNING TELESCOPE. The cutaway structure of the SCT is shown in figure 11-3. The SCT is mechanized with two axes - shaft and trunnion. The SCT operates such that the head assembly rotates about the shaft axis. The double dove prism, which is located in the head assembly, is the only component which rotates about the trunnion axis. The components which rotate about these axes are capable of 360° of rotation; however, these capabilities are not fully utilized. The SCT is a single line-of-sight (LOS), lower power (1X), refracting type of instrument with a 60° instantaneous field of view. The optical schematic of the SCT is shown in figure 11-5. Target search and recognition is possible by direct viewing through the 60° field of view.

The shaft axis section of the SCT is made up of an outer and inner tube assembly. The outer tube assembly contains the objective lens assembly and the focal plane reticle assembly. Fixed on top of the outer tube assembly is the trunnion axis section which contains the (1) double dove prism and mount assembly, (2) mount support, (3) cam-follower and spring assembly, and (4) trunnion worm drive. The inner tube assembly contains the pechan prism and half of the relay lens system. The remaining half of the relay lens system is secured to the face of the SCT panel.

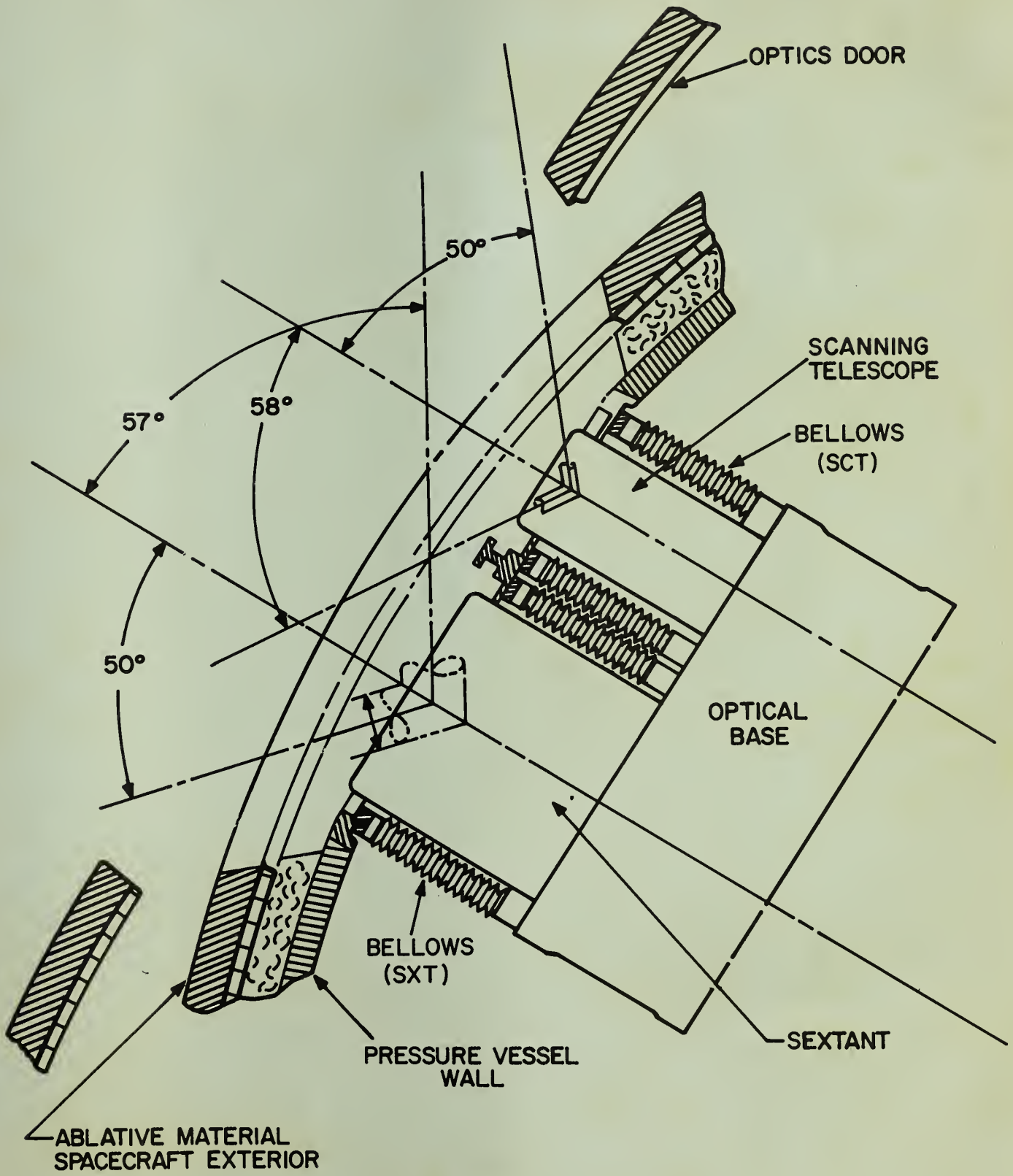


Figure 11-1. Optical Unit Cutaway

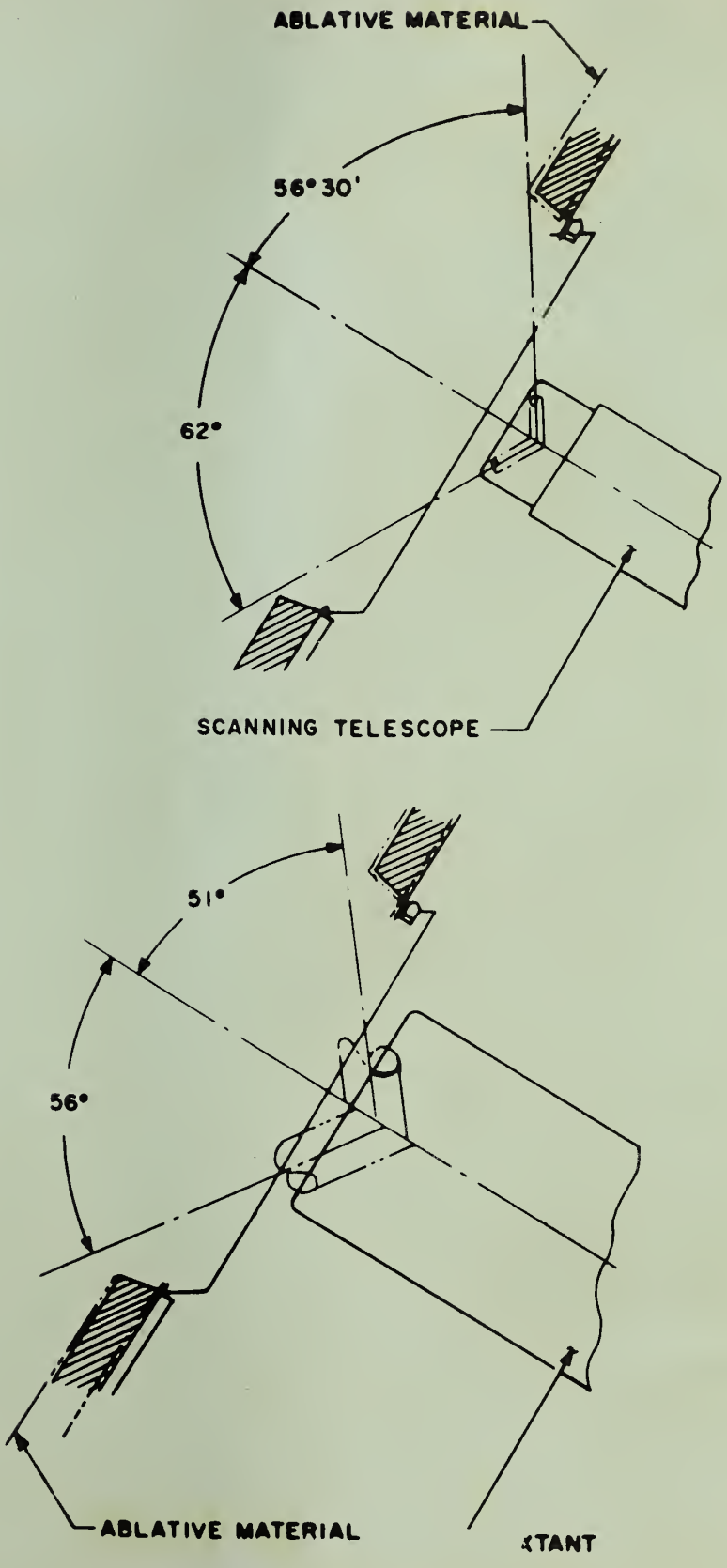


Figure 11-2. Vertical Optical Limits

1. Eyepiece window
2. Eyepiece prism housing assembly
3. Electrical connector
4. Relay lens assembly
5. Ball bearing (outer telescope tube assembly)
6. Outer telescope tube assembly
7. Optical base
8. Inner telescope tube assembly
9. Pechan prisms
10. Ball mount (3)
11. Ball bearing (outer telescope tube assembly)
12. Trunnion drive worm shaft
13. Dove prism and mount assembly
14. SCT head cover
15. Anti-backlash cam
16. Anti-backlash spring and cam follower
17. Objective lens assembly
18. Reticle assembly
19. Housing and lamp assembly
20. Shaft drive gear box
21. Cluster gear assembly
22. Shaft angle counter
23. Eyepiece assembly

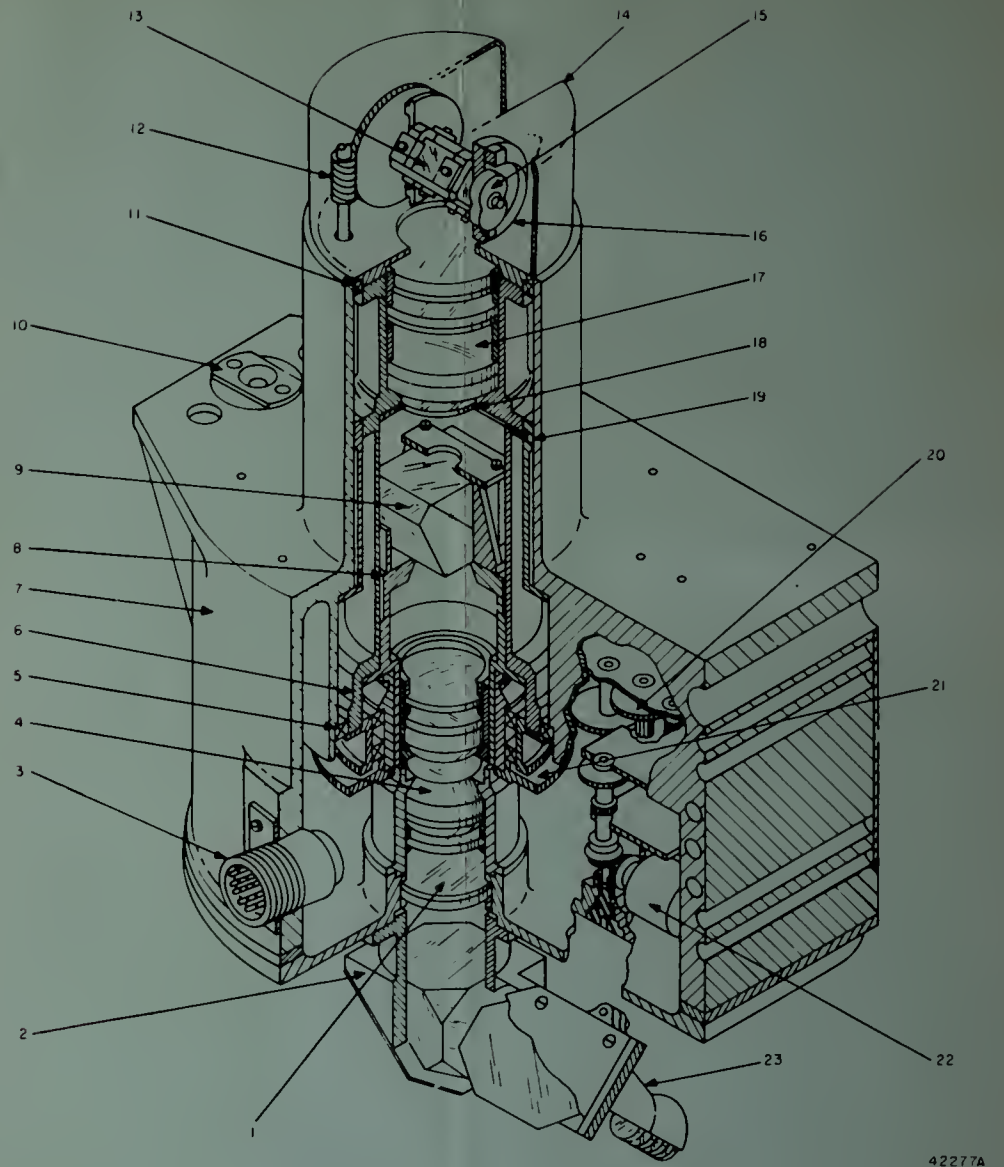


Figure 11-3. Scanning Telescope Cutaway

1. SXT panel assembly
2. Shaft axis assembly
3. Coolant passages (not used)
4. Optical base
5. Tracker and horizon sensor power supplies (not used)
6. Ball mount (3)
7. Horizon sensor mirror (not used)
8. SXT right angle mirrors
9. Horizon sensor objective lens and filter housing (not used)
10. Trunnion resolvers
11. SXT head cover
12. Star tracker right-angle mirrors (not used)
13. Threaded rod (cover support) (2)
14. Tuning fork drive amplifiers (not used)
15. Indexing mirror and mount assembly
16. Tracker head electronics (not used)
17. Tracker tuning fork resonator (not used)
18. Star tracker photomultiplier and lens housing (not used)
19. Horizon sensor head electronics (not used)
20. Trunnion drive gear box
21. Horizon sensor photomultiplier and lens housing (not used)
22. Horizon sensor tuning fork resonator (not used)
23. SXT objective lens holder assembly
24. SXT telescope intermediate lens assembly
25. Reticle assembly
26. Shaft resolvers
27. Eyepiece window
28. Shaft drive gear box
29. Eyepiece prism assembly

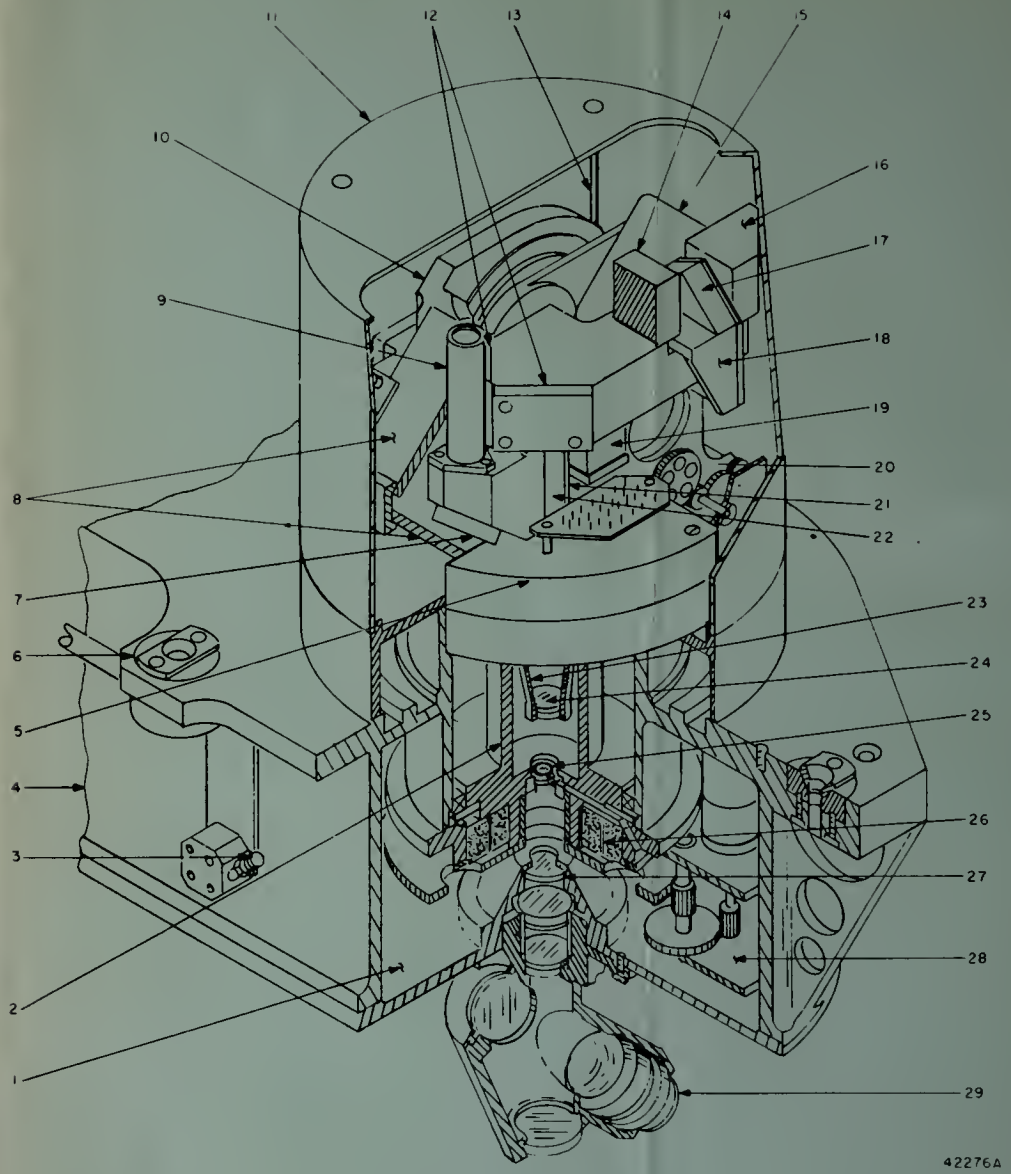


Figure 11-4. Sextant Cutaway

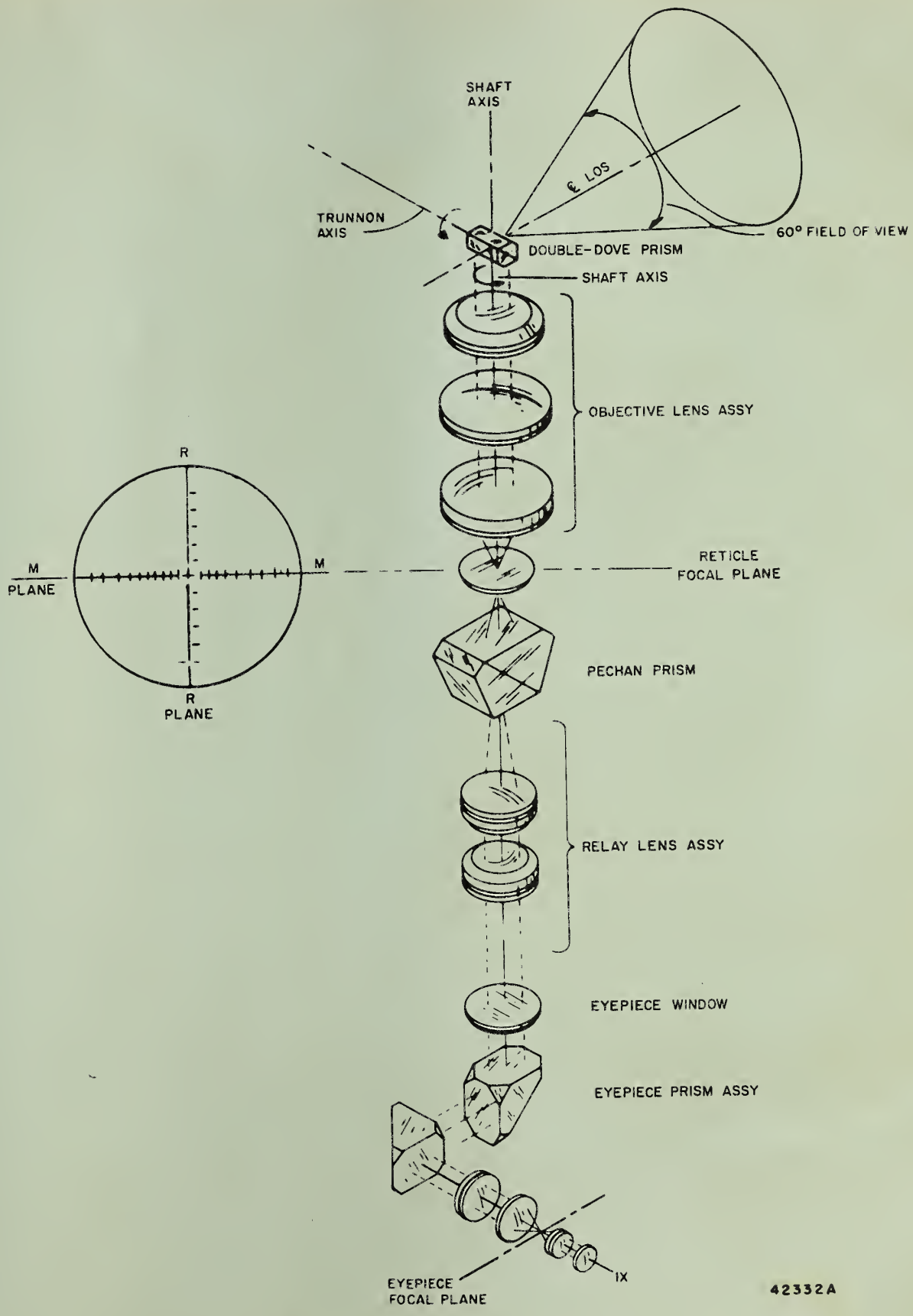


Figure 11-5. SCT Optical Schematic

11.1.2.1 Double Dove Prism. The double dove prism contains two dove prisms which are optically matched and cemented together. This is the first optical element in the SCT to pick up the target image. The target image is inverted by the prism and transmitted to the objective lens assembly.

The prism is driven by a worm gear and shaft which extends up the SCT tube. The mechanical gearing of the SCT is shown in figure 11-6. The worm gear shaft is driven by a motor generator in the SCT trunnion gear box which is located in the optical base. Positional accuracy is made possible by the use of an anti-backlash device.

This mechanism is also used to drive the trunnion axis section about the shaft axis by the use of a separate motor generator. The shaft and trunnion axes drives are linked by a differential shaft assembly. The purpose of the differential gear assembly, as shown in figure 11-7, is to permit shaft axis rotation without introducing errors in the trunnion axis and vice versa. The shaft drive gear is pinned to the differential shaft. The trunnion gears rotate freely about the differential shaft. The trunnion drive and positioning gears are connected by a planetary system which is pinned to the differential shaft. This makes (1) rotation of the shaft drive gear possible without the introduction of an error into the trunnion positioning and (2) trunnion drive possible without affecting the shaft drive gear. Two identical counters, displaying the SCT's shaft and trunnion angular position, are located in the optical base. The counters are viewed through lighted windows in the SCT panel and are calibrated to display readouts from 0^{o} to 359.98^{o} with $.002^{o}$ graduations. Manual positioning of the SCT is possible if the electronics fail.

11.1.2.2 Objective Lens Assembly. The objective lens assembly transmits the inverted image from the double dove prism and focuses this image on the reticle plane. The objective lens assembly consists of the cemented double lens fitted into the upper end of the outer tube giving the set a 60^{o} field of view.

11.1.2.3 Reticle. The reticle is located in the outer tube adjacent to the objective lens. It is accurately positioned in the focal plane so that the collimated light from the target image is viewed without any apparent parallax. The reticle cross hair intersection, as shown in figure 11-5, is the reference for the target image. The reticle is illuminated from the edge by four incandescent lamps. Three light-transmitting rods, assembled 120^{o} apart in the reticle plane, direct light from the lamps to the reticle and provide a uniform illumination at any shaft angle.

11.1.2.4 Pechan Prism. The pechan prism, figure 11-8, is located in the end of the inner telescope tube assembly that faces the reticle assembly. This prism erects and transmits the image inverted by the double dove prism. The pechan prism consists of two sections which are spearated by a gap.

11.1.2.5 Relay Lens Assembly. The relay lens assembly consists of two groups of lenses: The first group is attached to the inner telescope tube opposite the pechan prism; the second group is secured to the inside face of the telescope panel.

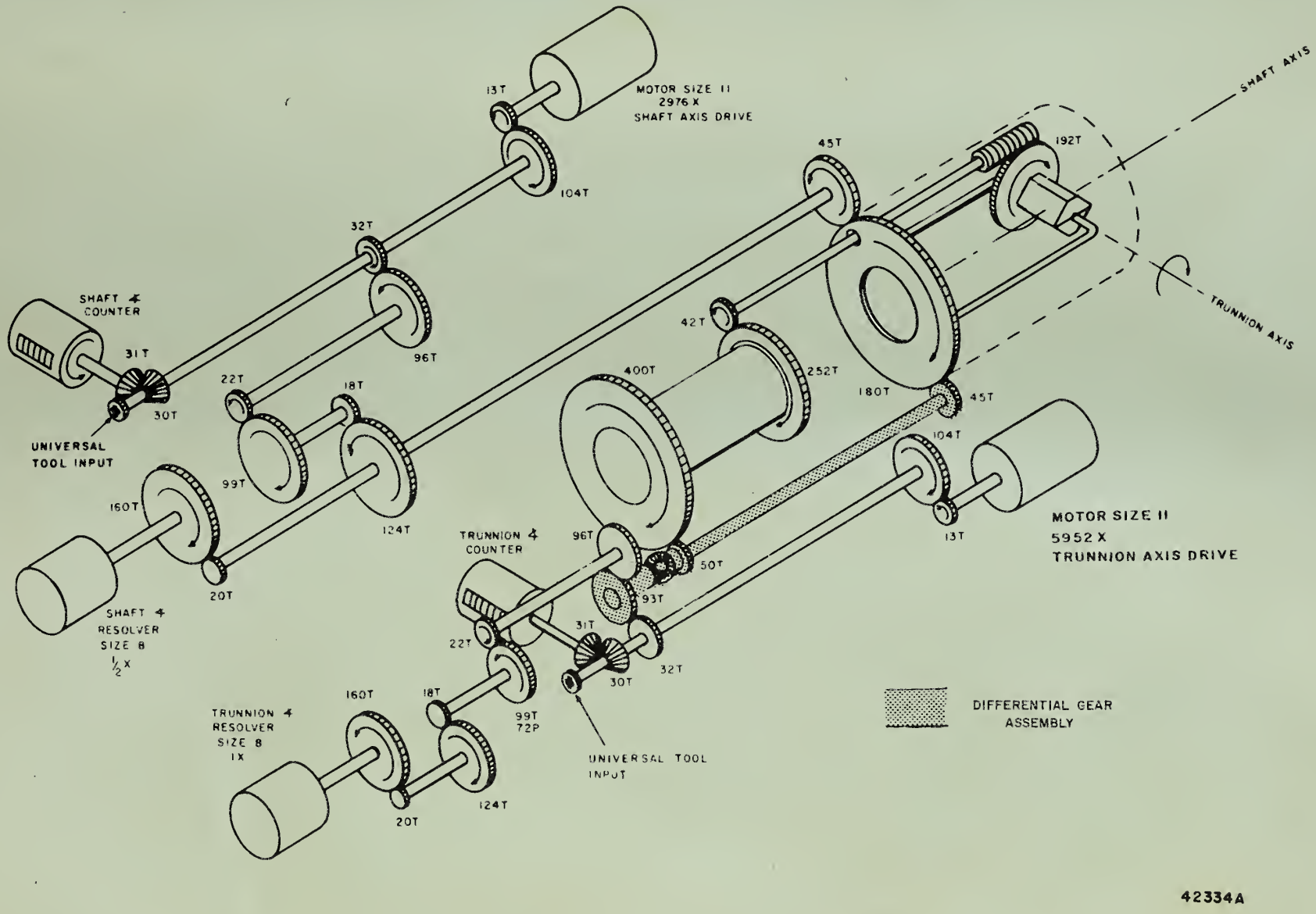


Figure 11-6. SCT Gearing

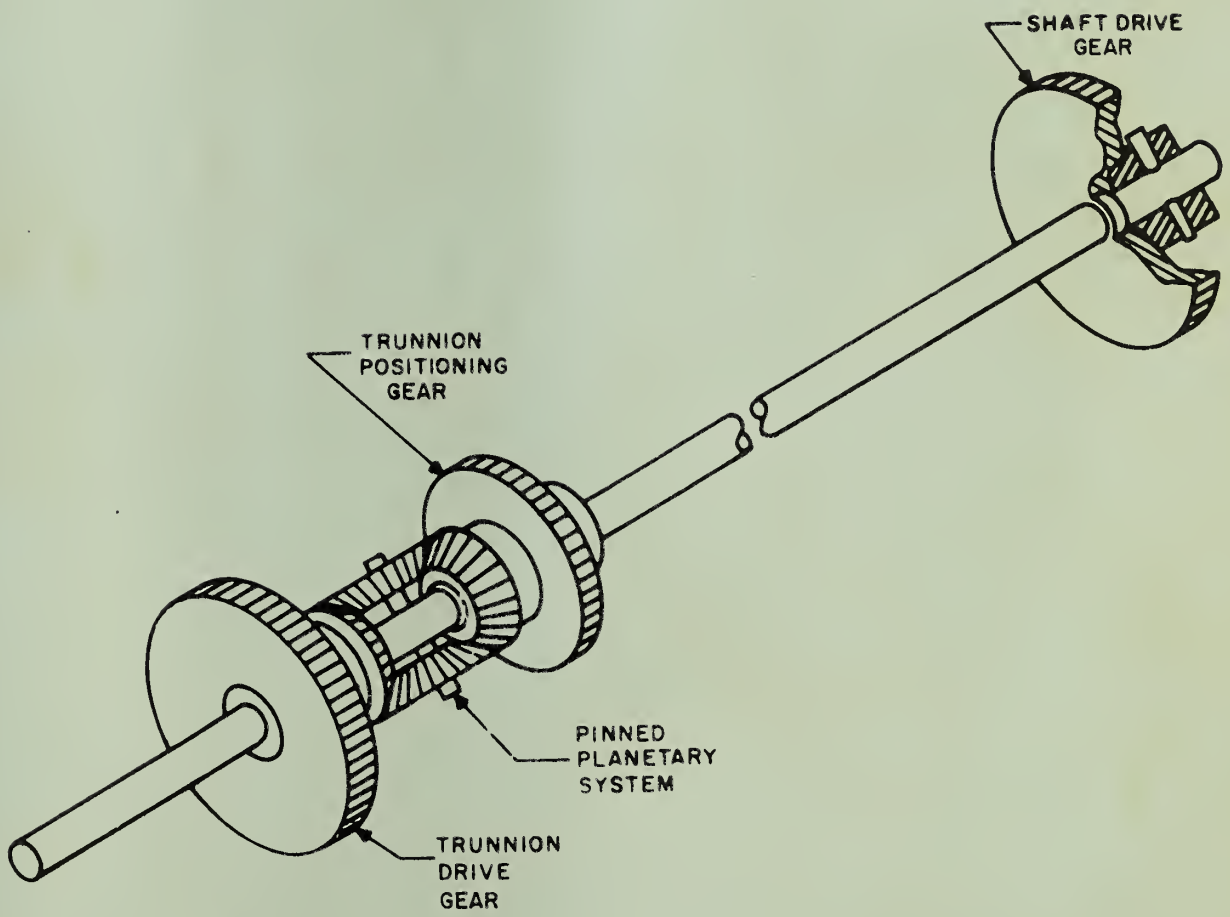


Figure 11-7. Differential Gear Assembly

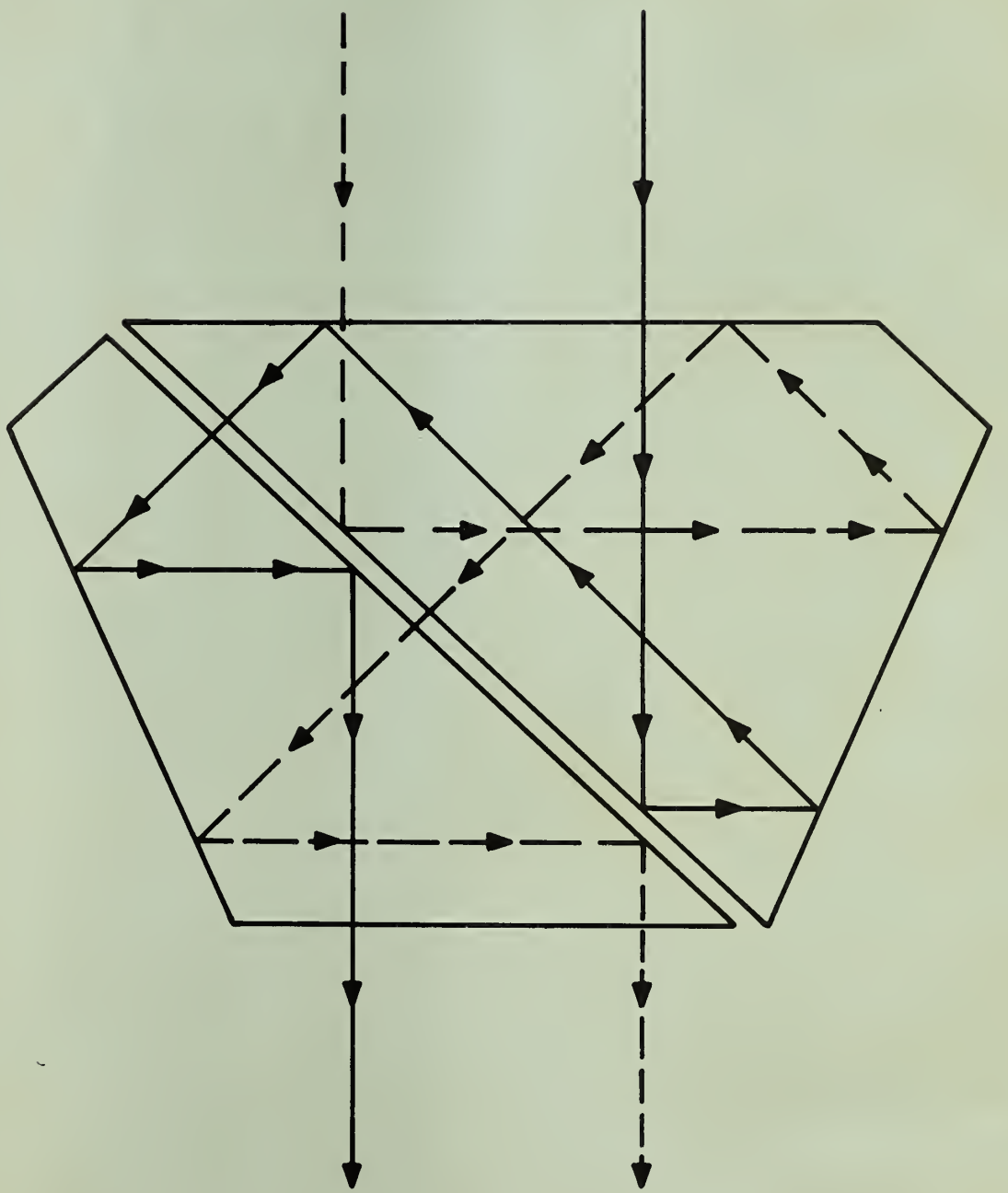


Figure 11-8. Pechan Prism

11.1.2.6 Eyepiece Window and Prism Assembly. The eyepiece window is attached to the SCT panel and provides a seal between the eyepiece components and the SCT components which are exposed to the environmental conditions outside the spacecraft. The window has no optical effect and transmits the target image directly from the relay lens assembly to the eyepiece prisms. The eyepiece prisms transmit the image to the eyepiece lens along a new line of sight (see figure 11-5) so that the center line of the eyepiece lens is not normal, but horizontal, to the optical panel.

11.1.2.7 SCT Eyepiece Assembly. The SCT eyepiece is secured to the SCT prism housing assembly. It consists of three lens assemblies secured into the eyepiece housing. An eye guard assembly made of non-toxic synthetic rubber is attached to the eyepiece housing. The eye guard is adjustable in an axial direction to allow for differences in facial contours.

An SCT long eye relief eyepiece assembly is also provided for use by the astronaut when wearing the helmet of the pressure suit. This unit will allow the astronaut to use the SCT while in the suited condition. The long eye relief eyepiece completely replaces the standard eyepiece and has a rubber guard attached to it which is contoured to match the pressure suit helmet.

11.1.2.8 SCT Optics Light Transmission. When a beam of light passes through an optical instrument, the light intensity will decrease. This decrease in intensity is primarily due to adsorption and secondly to scattering. The light losses in the SCT are approximately 30% to 40% of the light impinging on the double dove prism.

11.1.3 SEXTANT. The structure of the SXT is shown on figure 11-4. The SXT is mechanized with two axes, shaft and trunnion. The SXT operates so that the index head portion of the unit rotates about the shaft axis. The components which rotate about the trunnion axis are also located in the index head and include (1) the indexing mirror and its associated trunnion drive motor, (2) resolvers, and (3) gearing.

The SXT is limited to $\pm 270^{o}$ of rotation about the shaft axis and to between -5^{o} through $+ 50^{o}$ of rotation about the trunnion axis. The SXT is a multiple line-of-sight (LOS) electro-optical instrument with a 28X magnification and a 1.8^{o} visual field of view. The optical schematic of the SXT is shown in figure 11-9.

The lines-of-sight of the SXT are the star line-of-sight (SLOS) and the landmark line-of-sight (LLOS). The LLOS is fixed within the SXT while the SLOS is moveable as a function of the motion of the indexing mirror about the trunnion and shaft axes. The SXT hardware is divided into two units, the index head assembly and the base section.

The index head assembly contains (1) the index mirror and associated trunnion drive components, (2) the right angle mirrors and (3) a beam splitter.

The base section houses the shaft axis assembly and corresponding drive components such as motor generator, resolver and gearing. It also contains the SXT telescope lens and the reticle. Attached to the base section is the SXT panel assembly which contains the eyepiece window and provides for the mounting of the SXT eyepiece.

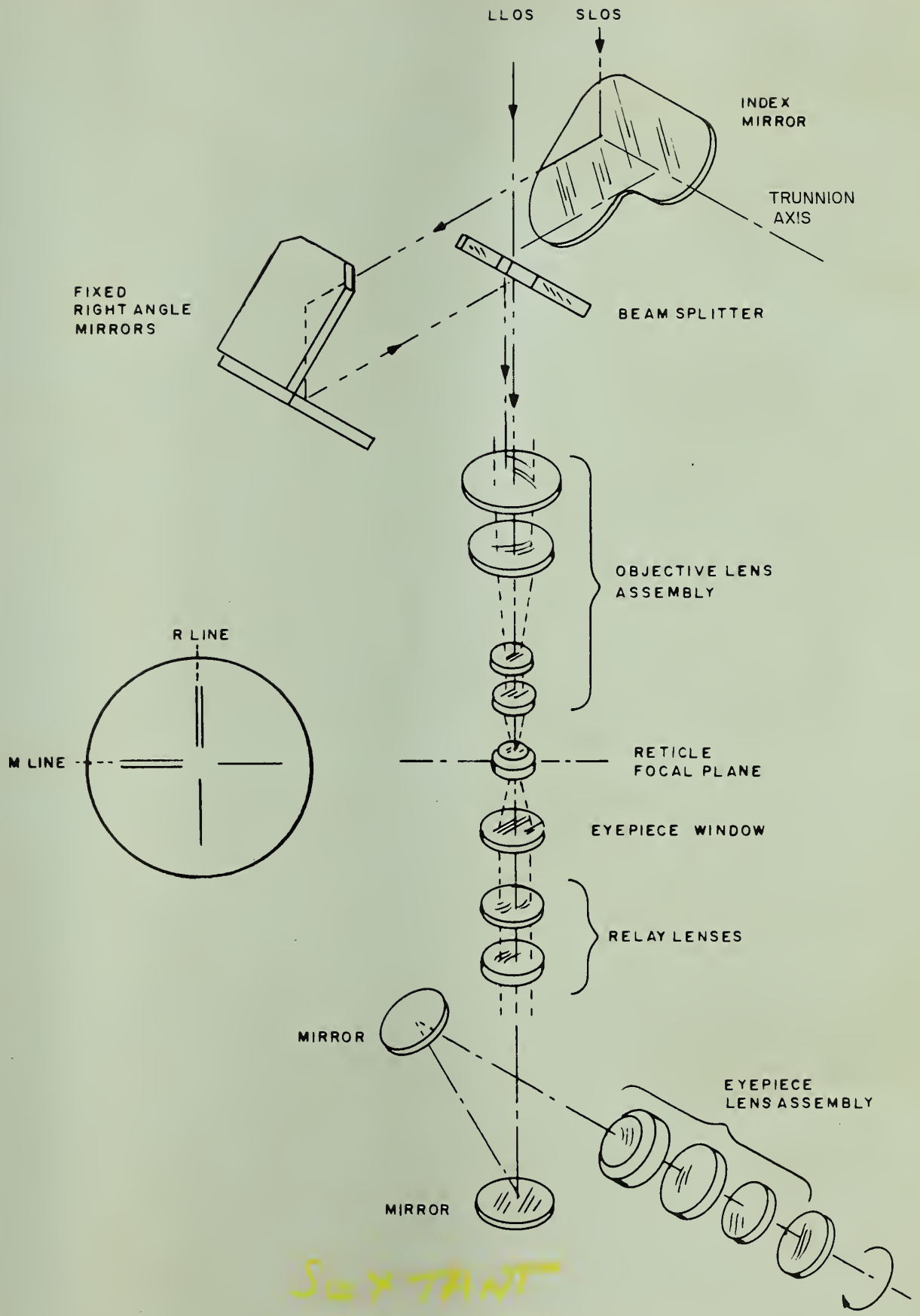


Figure 11-9. SXT Optical Schematic

42331A

11.1.3.1 Indexing Mirror Assembly. The indexing mirror is constructed of beryllium with a reflecting surface coated with silicon monoxide. The mirror is lightened, balanced, and pivoted on ball bearings to insure accurate operation. The star image is reflected into the right angle mirrors by the indexing mirror which is controlling the star LOS. As the indexing mirror moves there is an optical multiplication of the angle through which the SLOS moves, i.e., for each one degree of motion of the indexing mirror, there is two degrees of motion of the SLOS (see figure 11-10). In figure 11-10a, the light from the star is reflected at a 10^{o} angle to the incident light. In figure 11-10b, the mirror which has been moved by 5^{o} now has the star image reflected at an angle of 20^{o} to the incident light, i.e., an increase of 10^{o}. Therefore, it can be seen that the LOS angle increases twice as rapidly as the mirror angle.

11.1.3.2 Right Angle Mirrors. Two mirrors are fixed at right angles to each other and reflect the star image onto the reflective underside of the beam splitter. Both mirrors are fabricated from beryllium with aluminized reflecting surfaces and a silicon monoxide coating.

11.1.3.3 Beam Splitter. As mentioned previously, the SXT has two visual lines-of-sight, the SLOS and the LLOS, which are viewed simultaneously by the astronaut. When viewed directly, the landmark has a greater intensity of illumination than that produced by the star. For this reason, the star would be obscured by the landmark's brightness. The beam splitter's purpose is, therefore, to transmit both the star and landmark images simultaneously into a common eyepiece in such fashion that they both can be seen. The beam splitter's construction provides for the transmission of one image by total reflection from one surface; the second image is reduced in intensity by partial refraction through the beam splitter. As can be seen in figure 11-7, the landmark light is refracted through the beam splitter, and the star light is reflected from the bottom of the beam splitter. This introduces both images into the objective lens assembly.

11.1.3.4 SXT Telescope Optics. The SXT telescope optics consists of an objective lens assembly, a reticle and an eyepiece window. The objective lens assembly consists of two objective lenses and two intermediate lenses which form a telephoto-type lens system. The reticle, as shown in figure 11-9, is positioned in the focal plane of the objective lens. The illumination of the reticle is provided by four lamps which emit light onto three transmitting rods spaced evenly around the reticle edge. The eyepiece window has no optical effect on the SXT optics and serves as a seal in the SXT panel.

11.1.3.5 SXT Eyepiece Assembly. The eyepiece assembly consists of the eyepiece objective lens, two mirrors and the eyepiece ocular lens. The objective lens, also called relay lens, relays the images to the two fixed mirrors. The mirror provides a change in direction of the lines-of-sight and thereby facilitates the astronauts' use of the SXT. The eyepiece assembly provides 3.4 power magnification of the total 28 power magnification of the SXT.

11.1.3.6 SXT Optics Light Transmission. In the SXT, the light impinging on the indexing and fixed mirrors is decreased by approximately 4% at each mirror which results in about 88% of star light remaining to be reflected by the beam splitter. The beam splitter further reduces the light by approximately 18% with an additional loss of about 52% through the telescope and eyepiece. The net result is a total light transmission of about 35% for the SLOS.

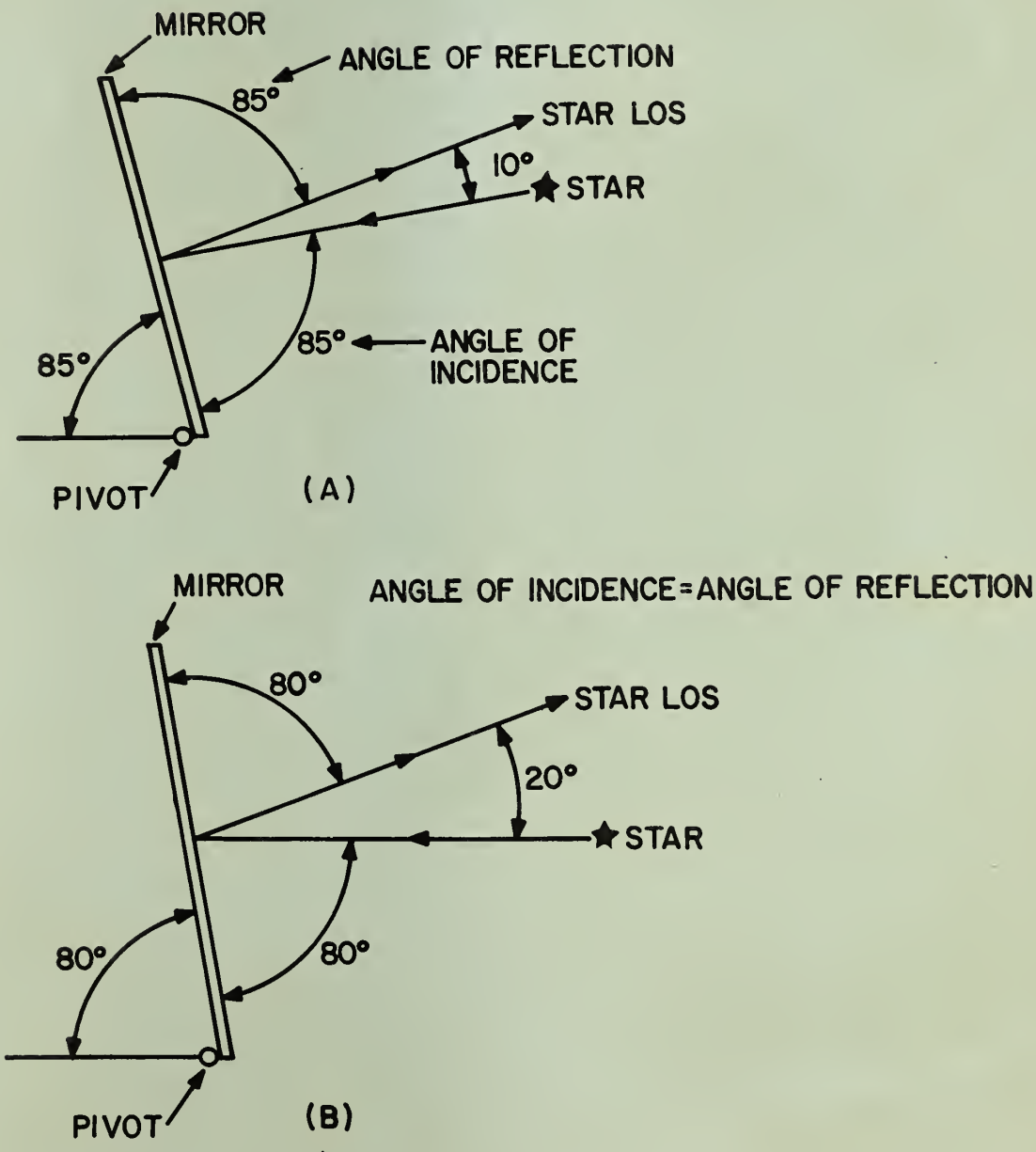


Figure 11-10. Motion of Indexing Mirror

In the LLOS, a loss of 89% occurs in the beam splitter. The remaining 11% is further attenuated by 52% which results in an overall transmission of about 5% in the LLOS.

11.1.4 OPTICAL SUBSYSTEM AXES. The shaft and trunnion axes of the optical subsystem must be related to the axes of the navigation base in order to define orientation with respect to the spacecraft. As discussed in the inertial subsystem hardware section and shown figure 3-14, the navigation base orientation in the spacecraft is such that the Y_{nb} axis is parallel to the Y_{sc} axis while the remaining axes, X_{nb} and Z_{nb}, are displaced by 33^{o} from the X_{sc} and Z_{sc} axes respectively.

The Z_{nb} axis is normal to the outside surface of the spacecraft. The shaft axes of both instruments, SCT and SXT, are fixed within the optical assembly which is mounted to the navigation base; therefore, the shaft axes are parallel to the Z_{nb} axis which makes the LLOS parallel to the Z_{nb} axis. The trunnion axes within the SCT and SXT are perpendicular to the shaft axes. Prior to each utilization of the optics, it is required that they be driven to an initial or zero orientation. At this time, the shaft axes are driven to a position which is defined as "zero" when the trunnion axes are parallel to the Y_{nb} axis. The orientation of the SXT reticle at this time is as shown in figure 11-9. The trunnion axes are likewise driven to a "zero" orientation. In this position, the SLOS is parallel to the Z_{nb} axis. The axes relationships can be tabulated as follows:

1) Shaft Axes (SA) // Z_{nb} // LLOS

2) Trunnion Axes (TA) $\perp$ SA

3) When Optics are "zeroed"

   a) TA // Y_{nb} // Y_{sc}

   b) SLOS // LLOS // Z_{nb}.

11.2 ASSOCIATED OPTICAL EQUIPMENT

The following equipment is associated with the optical unit assembly:

a. Navigation Base (NB)

b. Bellows (2)

c. G&N Indicator Control and associated electronics

d. Coupling Display Units (CDU's) (2 required)

e. Power Servo Assembly (PSA) (portions).

11.2.1 NAVIGATION BASE. The navigation base (NB), figure 11-11, is a structural part of the guidance and navigation system. The navigation base is designed to provide: 1) a rigid supporting structure for the IMU and optical assembly to retain a precision alignment of these units, and 2) mounting of the IMU and optical assembly to the spacecraft. The navigation base is machined from a hot-pressed beryllium billet and lightened by machining cavities between the webs of the structural members. The final machining is accomplished on the IMU and optical assembly mounting points so the IMU and optical assembly mounting planes will be parallel within five arc-seconds. Three mounts, two at the upper end and one at the lower end, attach the navigation base, IMU, and optics to the spacecraft.

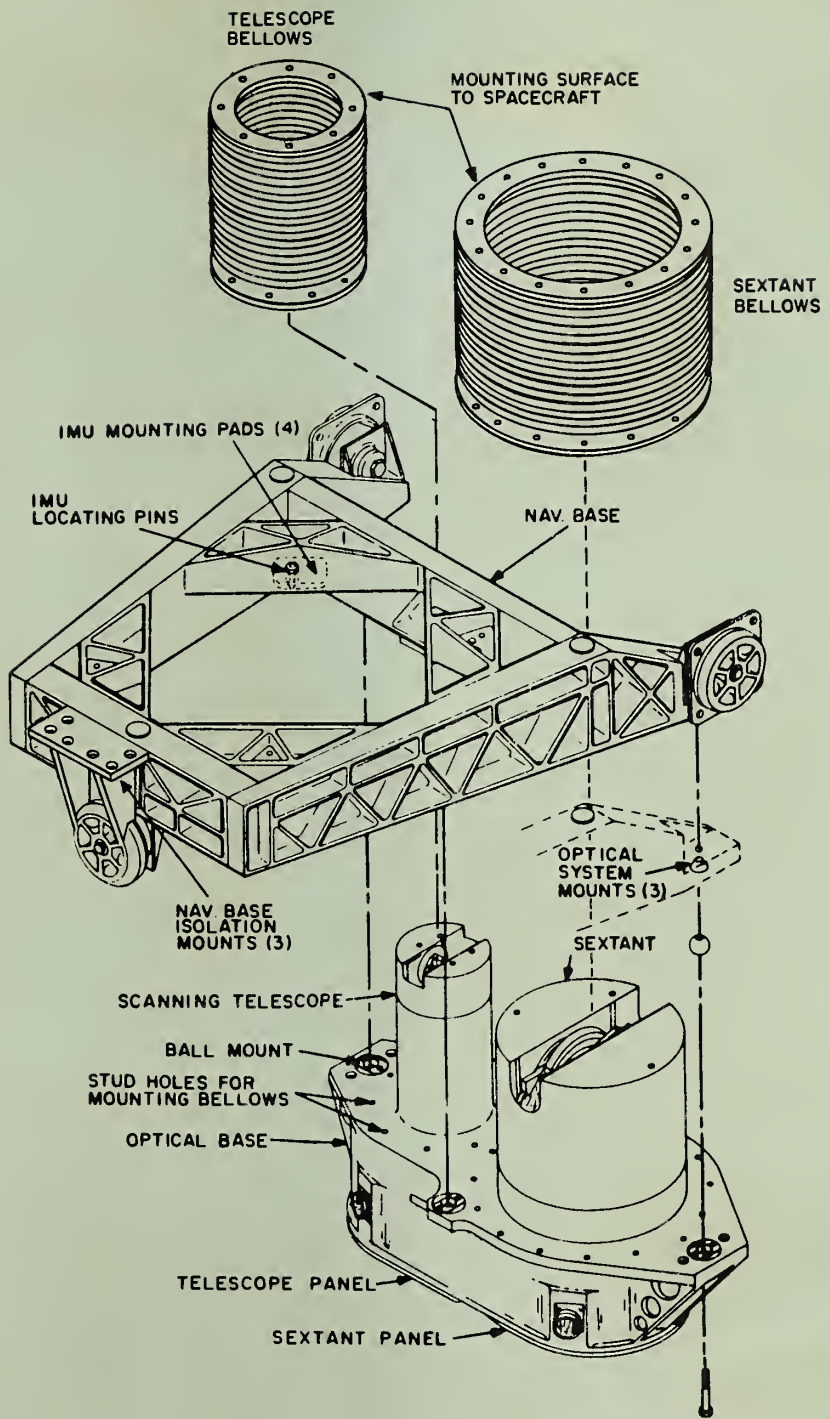


Figure 11-11. Optical Unit, Navigation Base and Bellows

11.2.2 BELLOWS. The optical instruments must protrude through the wall of the spacecraft pressure vessel in order to make the accurate navigational sightings. The opening provided for this purpose exposes the interior of the spacecraft to the vacuum of space. Therefore, some means of sealing is required. This sealing is accomplished by stainless-steel, double-walled flexible bellows assemblies figure 11-11). A separate bellows is required for each of the optical instruments. The bellows are bolted to the optical base assembly and individually encompass the SXT and SCT. The upper end of the bellows is then bolted to the spacecraft with sealing provided by "O" rings at the mating surfaces.

11.2.3 G&N INDICATOR CONTROL PANEL. The G&N Indicator Control Panel has been previously discussed in the inertial subsystem portion of the study guide along with its associated electronics.

The G&N Indicator Control Panel is shown again in figure 11-12 with the controls associated with the optical subsystem indicated. These include the optics hand controller, the optics moding controls, the attitude impulse controls and the MARK and MARK REJECT buttons. These are the only controls for the operation of the SXT and the primary controls for the SCT. A manual secondary control for the SCT is provided on the SCT panel by the use of the universal tool.

The optics hand controller has two degrees of freedom and is used to input electrical signals to the SXT shaft and trunnion drive loops in order to position the optical lines-of-sight. The optics moding controls consist of: a three position rotary switch which selects major modes; a three position toggle switch which modifies the operation of the SCT trunnion axis; a three position toggle switch which controls the voltages applied by hand controller; a two position toggle switch which modifies the manual mode of operation. The detailed functions of these switches will be described in the discussion on moding.

The attitude impulse controller has three degrees of freedom. It is used for fine rate control of the spacecraft in pitch, yaw and roll. The controller contains microswitches which provide discrete outputs. A twist of the controller will provide yaw rate changes. Up and down movements of the controller affect spacecraft pitch rate, while right and left movements of the controller affect roll rate.

The two position toggle switch associated with the above mentioned switch is used to enable the attitude control function by disabling the attitude holding functions of the SCS.

The MARK button is used by the astronaut when manually completing an optical sighting. It directs the AGC to record the position of the CDU's along with the time of the sighting. This information is used in navigational calculations. An erroneous sighting may be cancelled by the MARK REJECT button.

The display and control electronics, figure 7-4, affect the OSS through the panel brightness control (paragraph 7.3.1). The control electronics are associated with the optics in that they contain the mark relay which is controlled by the MARK button.

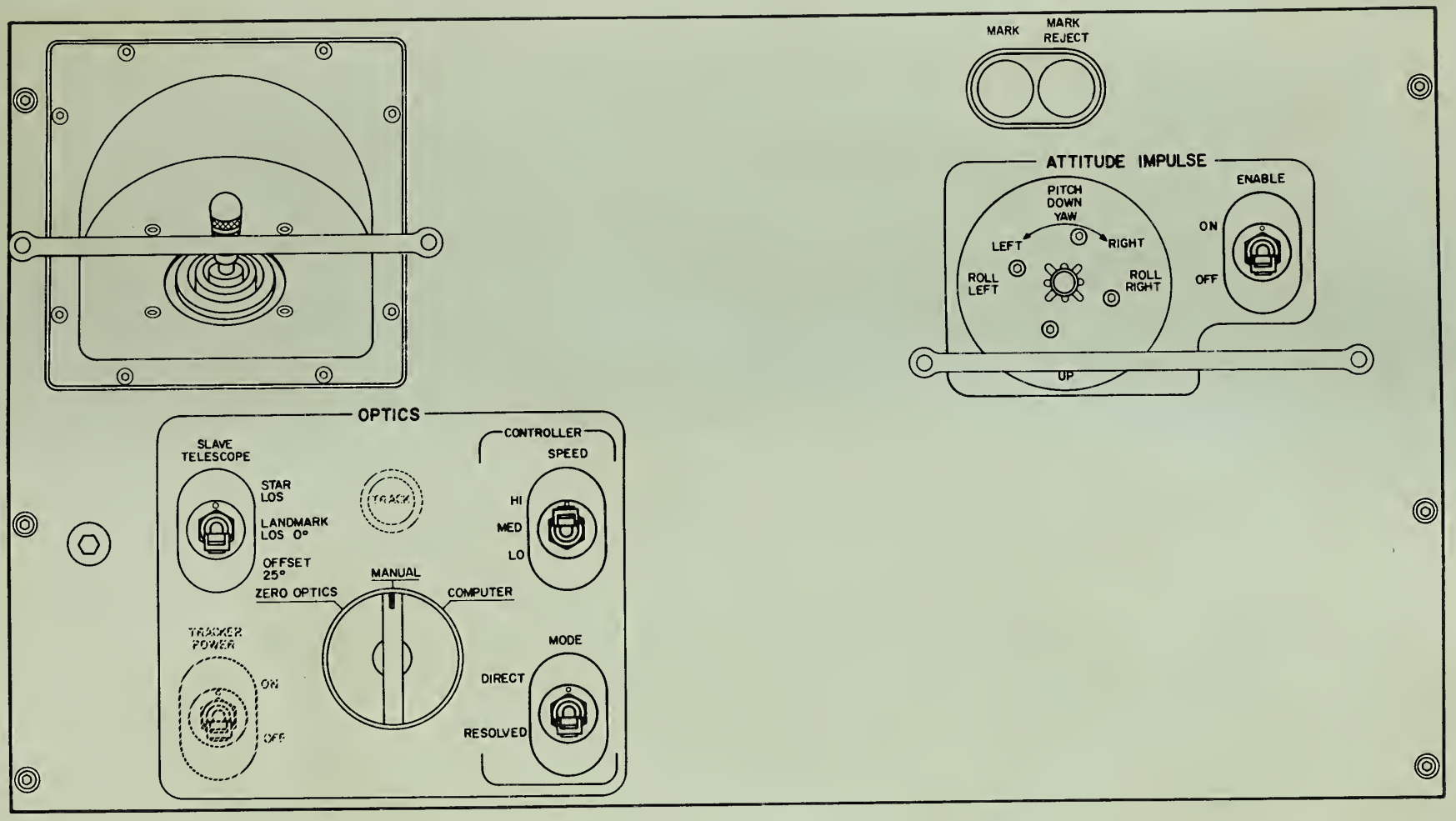


Figure 11-12. G&N Indicator Control Panel

11.2.4 COUPLING DISPLAY UNITS. Two coupling display units are required for operation with the OSS, one for the shaft axes and one for the trunnion axes. These CDU's are physically similar to the CDU's used in the ISS but, because of small changes, are neither functionally nor electrically interchangeable with the ISS CDU's. The discussion of the CDU's as presented in the ISS section of this study guide, Section IV, is applicable as is the information presented concerning the motor drive amplifiers, digital encoder electronics and digital to analog converter (DAC) electronics. The unique changes to the OSS CDU's are (1) the motor generator flywheels have been removed and the motor generators have been changed to provide a more rapid response and (2) the electrical connections have been changed to prevent operation if installed in the ISS. A mechanical block diagram of the CDU as used in the OSS is shown in figure 11-13. The CDU's are located as shown in figure 10-1. The electrical mechanization of the shaft and trunnion CDU's will be discussed in Section XII.

When used as the trunnion CDU, the 16X and 1/4X resolvers function as receiving resolvers in an angular data transmission loop. The 1/2X resolver in the trunnion CDU, in conjunction with the cosecant amplifier, functions as a variable gain computing resolver. The encoder electronics are mechanized to generate two digital pulses per gear tooth, or a total of 2^{18} pulses per revolution of the 1/4X resolver. This results in an encoder granularity of approximately 5 sec trunnion movement/pulse or 10 sec SLOS movement/pulse because of the optical multiplication described previously. When used as the shaft CDU, the 16X and 1/2X resolvers function as receiving resolvers in an angular data transmission loop. The 1X resolver in the shaft CDU resolves polar coordinates into rectangular coordinates. The encoder electronics provide only one pulse per gear tooth or a total of 2^{15} pulses per revolution of the 1X resolver. This provides an encoder granularity of approximately 40 sec of shaft movement/pulse.

11.2.5 POWER AND SERVO ASSEMBLY. The majority of the electronics that are used to mechanize the OSS are located in the Power and Servo Assembly (PSA) as was described in Section VIII.

11.3 SUMMARY

The optical assembly consists of an optical base upon which are mounted the scanning telescope and sextant. Two coupling display units are required for use with the optical assembly along with portions of the G&N Indicator Panel, the power and servo assembly, the display and control electronics, and the control electronics. Bellows are required to seal the openings in the spacecraft pressure vessel that are provided for the sextant and scanning telescope.

The scanning telescope is a low power refracting optical instrument which provides a single 60^{o} field of view. It is used to locate and acquire the desired landmarks and stars on a gross basis. Two axes, the shaft axis and the trunnion axis, are used to define the movement of the SCT field of view.

The sextant is a high power (28X) optical instrument which is used for more accurate navigational sighting. The SXT has two visual lines-of-sight, the star LOS, and the landmark LOS, each of which has a 1.8^{o} field of view. The star and landmark images are made to appear in a single reticle pattern through a system of mirrors and lens. The landmark LOS is fixed parallel to the SXT shaft axis while the star LOS is moveable by rotation about both the shaft and trunnion axes.

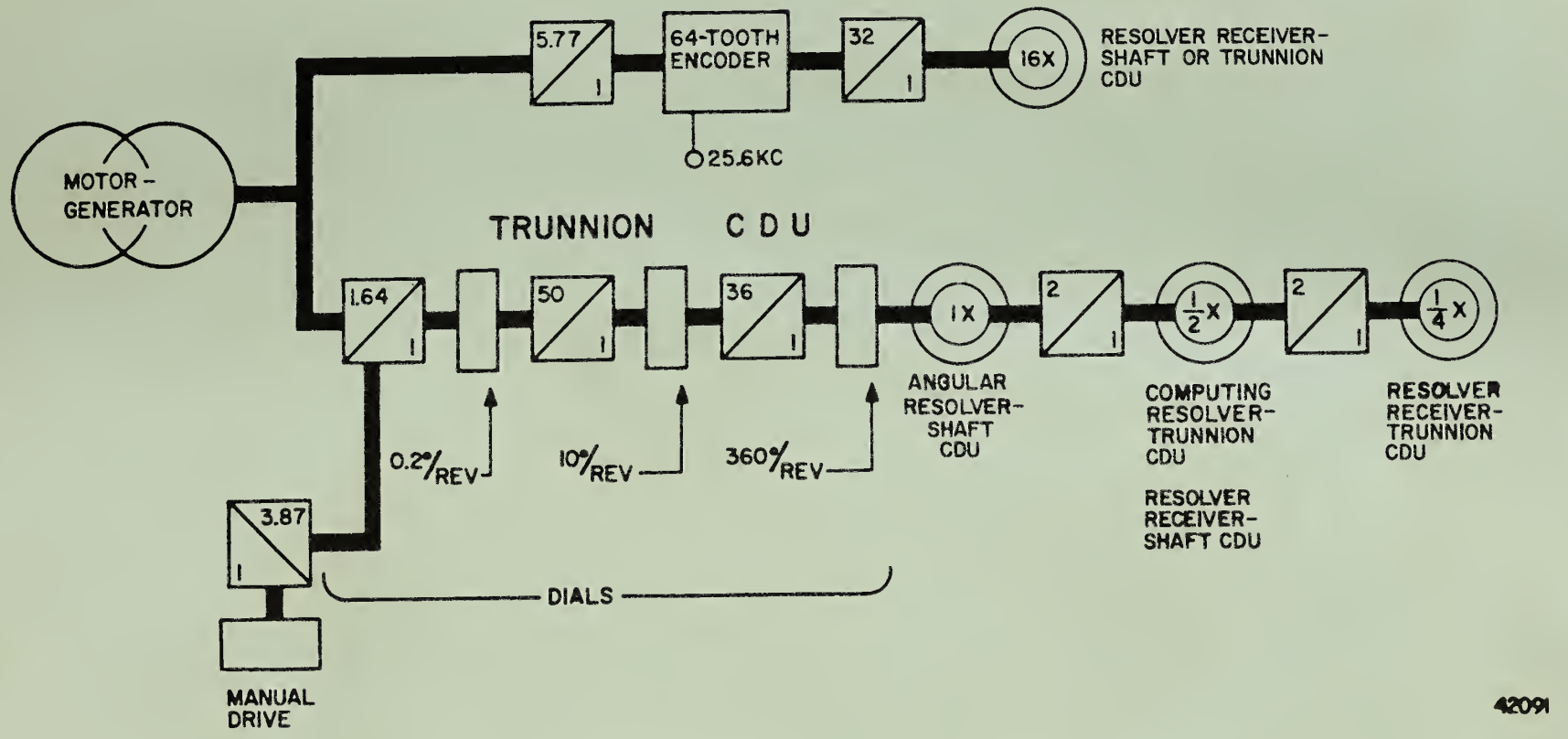


Figure 11-13. CDU Block Diagram

REVIEW QUESTIONS FOR SECTION XI

T F 1. The bellows provide a seal between the interior of the spacecraft and the vacuum of space.

T F 2. The sextant has a field of view of 60^{o}.

T F 3. The pechan prism is used in the scanning telescope.

T F 4. The SXT shaft is limited to the $\pm 270^{o}$ of movement.

5. The SXT shaft axis is:

   a. Parallel to the S/C Y axis.

   b. Parallel to the N/B Y axis.

   c. Parallel to the N/B Z axis.

   d. None of the above.

6. The SXT has a field of view of:

   a. 1.8^{o}

   b. 0.5^{o}

   c. 58^{o}

   d. 60^{o}

7. What provisions have been made for utilization of the optics if there is a malfunction in the electronics?

8. Explain why the OSS and ISS CDU's are not interchangeable.

SECTION XII

OPTICAL SUBSYSTEM MECHANIZATION

INTRODUCTION

This section explains the functional loops and describes the modes of operation of the optical subsystem.

12.1 OPTICAL LOOP MECHANIZATION

The simplified mechanization of the optical loops is shown in figure 12-1. This mechanization will be broken down in later figures to define the specific modes of operation. The SXT is the primary optical instrument and is therefore under the direct control from two possible inputs, the hand controller and the computer via the DAC. The electronics associated with the control of the SXT are defined as the integrating servo loops for the trunnion axis and shaft axis. The shaft and trunnion CDU's are slaved to the SXT operation as are the SCT shaft and trunnion axes. The CDU and SCTmechanizations are referred to as the position servo loops. Resolvers in the CDU's are used as part of the integrating servo loops. The SCT shaft is always slaved to the SXT shaft, but the SCT trunnion may operate independent of the SXT shaft in various optical modes, as selected by the astronaut.

The integrating servo loops utilize a selected input to the motor drive amplifier (MDA) to drive a motor in the SXT to position either the SXT shaft or trunnion. A tachometer feedback is provided. In order to inform the computer of the position of the SXT axes, a digital input to the computer must be provided. For this purpose the CDU's, which can provide a digital output via the encoder, are slaved to the SXT by a coarse-fine resolver loop. The SXT trunnion axis contains a 1X and a 64X transmitter resolver. These resolvers provide an output voltage proportional to trunnion position to 1/4X and 16X receiver resolvers in the trunnion CDU. The outputs of the receiver resolvers are then utilized to drive the CDU to the same position as the trunnion axis, and to provide an input to the computer.

The SXT shaft axis and shaft CDU operate in a similar manner but utilize 1/2X and 16X transmitter resolvers on the SXT shaft and 1/2X and 16X receiver resolvers in the shaft CDU.

The SCT position loop is a coarse resolver system only, with the 1X SXT trunnion transmitter resolver providing an input to the 1X receiver resolver in SCT trunnion and the 1X SXT shaft transmitter resolver providing an input to the 1X receiver resolver in the SCT shaft.

The CDU also provides a visual readout for the astronauts. The shaft CDU provides a direct reading of the angular position of the SXT shaft from zero, while the trunnion CDU provides a readout which is four times the trunnion angle and two times the SLOS angle from the zero position.

The relays as shown in figure 12-1, do not necessarily represent a single relay, but could be a number of simultaneously energized relays. The electronics that are shown along with the majority of the relays are located in PSA.

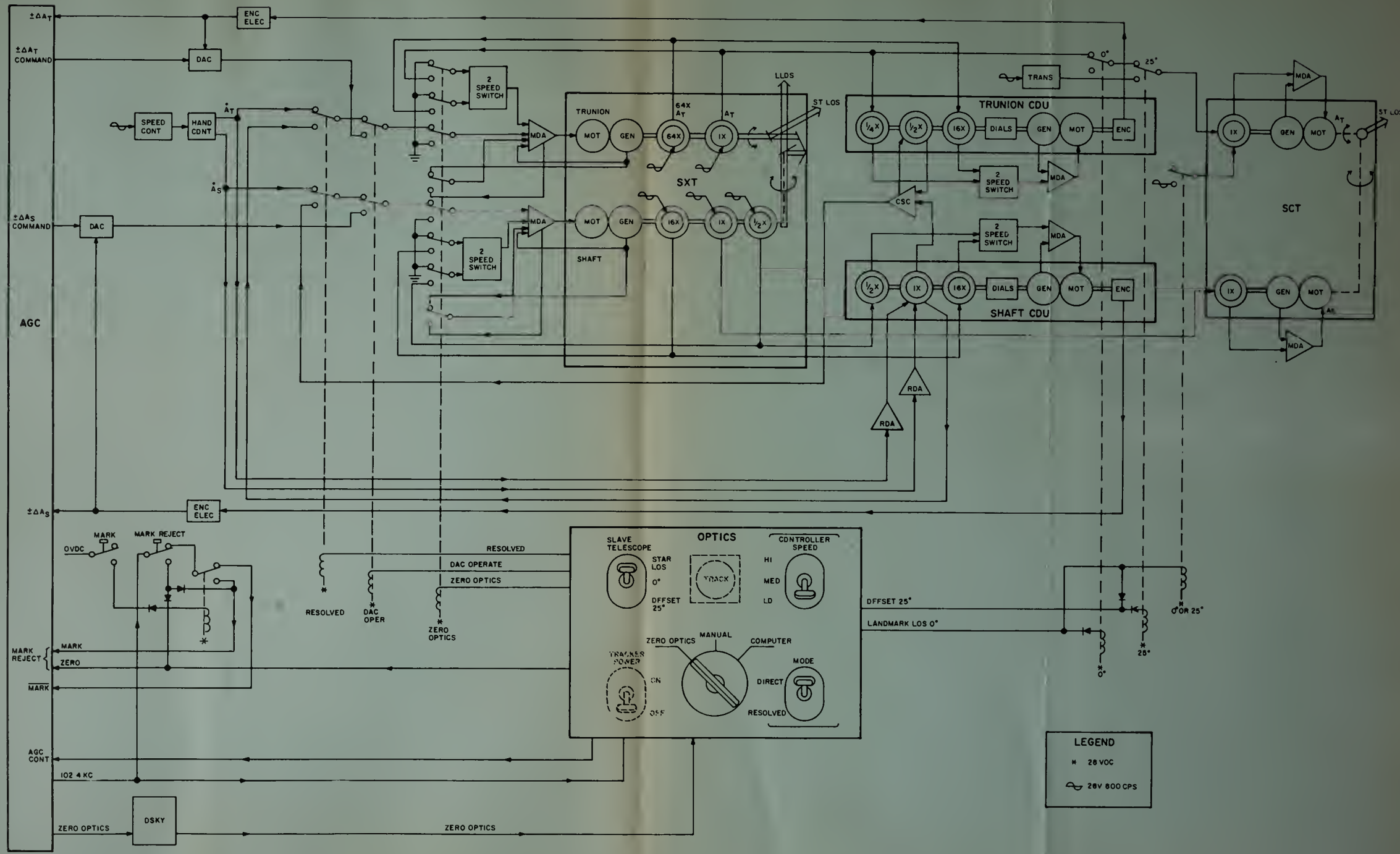


Figure 12-1. Optics Mechanization

The mark and mark reject controls on the G&N indicator panel are utilized to inform the computer when a navigation fix has taken place and instructs the computer to record or reject the CDU angles and time. The mark command is generated manually by the astronaut. When the mark relay is energized, it transmits a signal to the computer. If an erroneous mark is made, the mark reject button is depressed which will generate both a "mark" and "zero" command to the computer which will interpret them as a "Mark reject" command.

12.2 MODES OF OPERATION

The modes of operation for the optics are selected by the astronaut using the controls located on the G&N indicator control panel. There are three major modes of operation for the OSS:

1. Zero Optics
2. Manual Control
3. Computer Control

Within each of these modes there are variations which will be discussed as a part of that mode description.

12.2.1 ZERO OPTICS MODE. During the zero optics mode the shaft and trunnion axes of the SXT are driven to their zero positions by taking the outputs of the transmitting resolvers and feeding them, through the two-speed switches to the motor drive amplifier (MDA) which drives the loops to a null position (see figure 12-2). The two optical CDU's and the SCT shaft and trunnion axes follow to null positions. After a period of 72 seconds the computer will initialize its shaft and trunnion counter in preparation for receiving new data from the CDU encoders.

The zero optics mode can be selected either manually by the astronaut, or by the computer after the astronaut has selected the computer mode of operation. The computer selects zero optics by energizing a DSKY relay, which will in turn energize the appropriate OSS relays. The computer is notified of the zero optics mode via a return signal from the mode switching.

12.2.2 MANUAL MODE OPERATION. The manual mode can be operated in either the direct or resolved condition. Independent control of the SCT trunnion is possible in either condition.

12.2.2.1 Manual Direct Operation. The manual direct mode mechanization is shown in figure 12-3. When in this mode the hand controller outputs are applied directly to the SXT shaft and trunnion motor drive amplifiers. Forward and backward motion of the hand controller command increasing and decreasing trunnion angles, and right and left motion of the hand controller command increasing and decreasing shaft angles respectively. See figure 12-4 for a tabular presentation of the motion of the SXT in various modes. The target image motion is in the R-M coordinate system, the position of which is dependent upon the position of the SXT shaft.

The apparent speed of the image motion can be regulated by the astronaut through the selction of either low, medium or high controller speed on the G&N indicator panel. This regulates the voltage applied to the optics hand controller and therefore the shaft and trunnion input drive rates A_S and A_t , respectively.

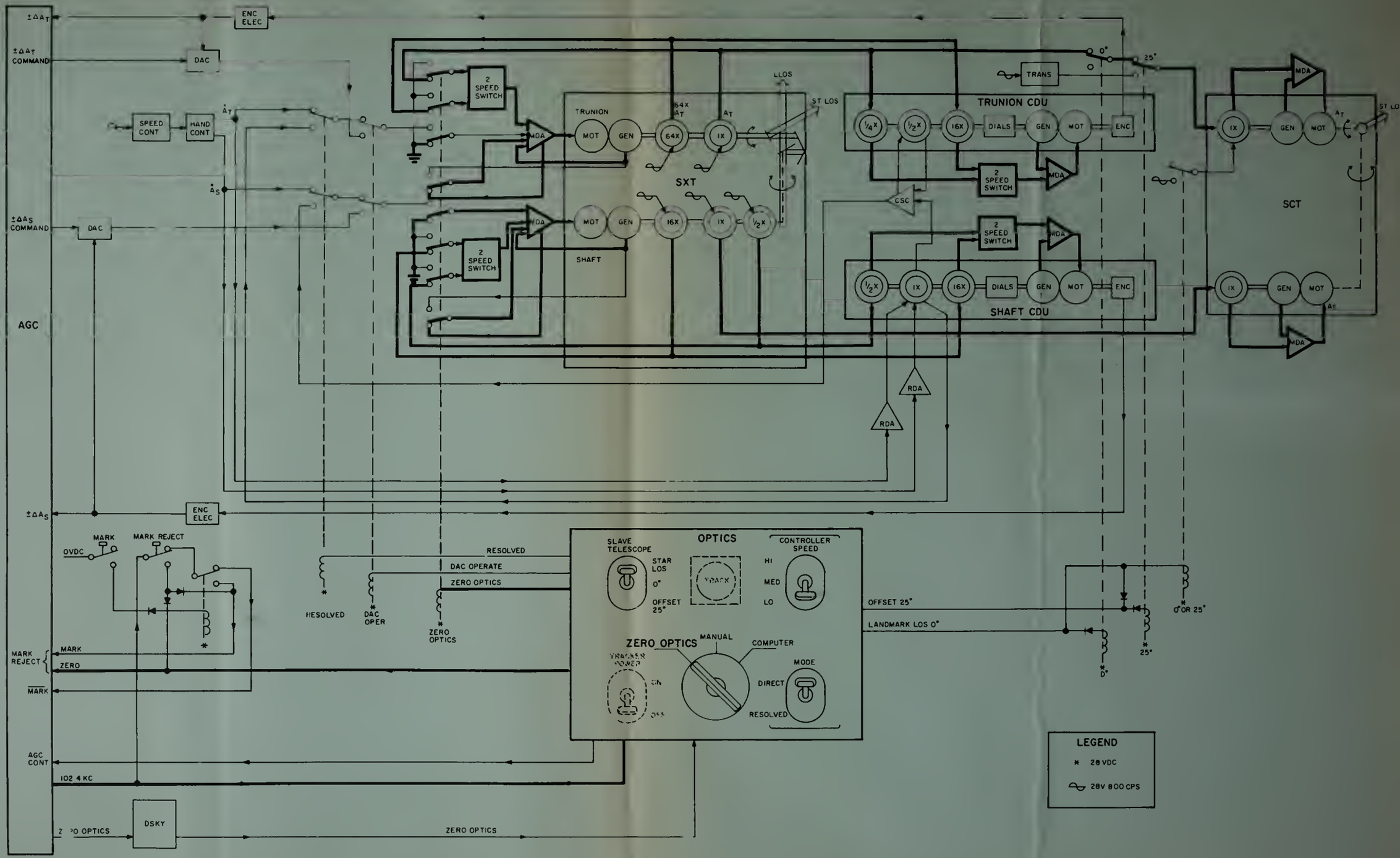


Figure 12-2. Zero Optics Mode

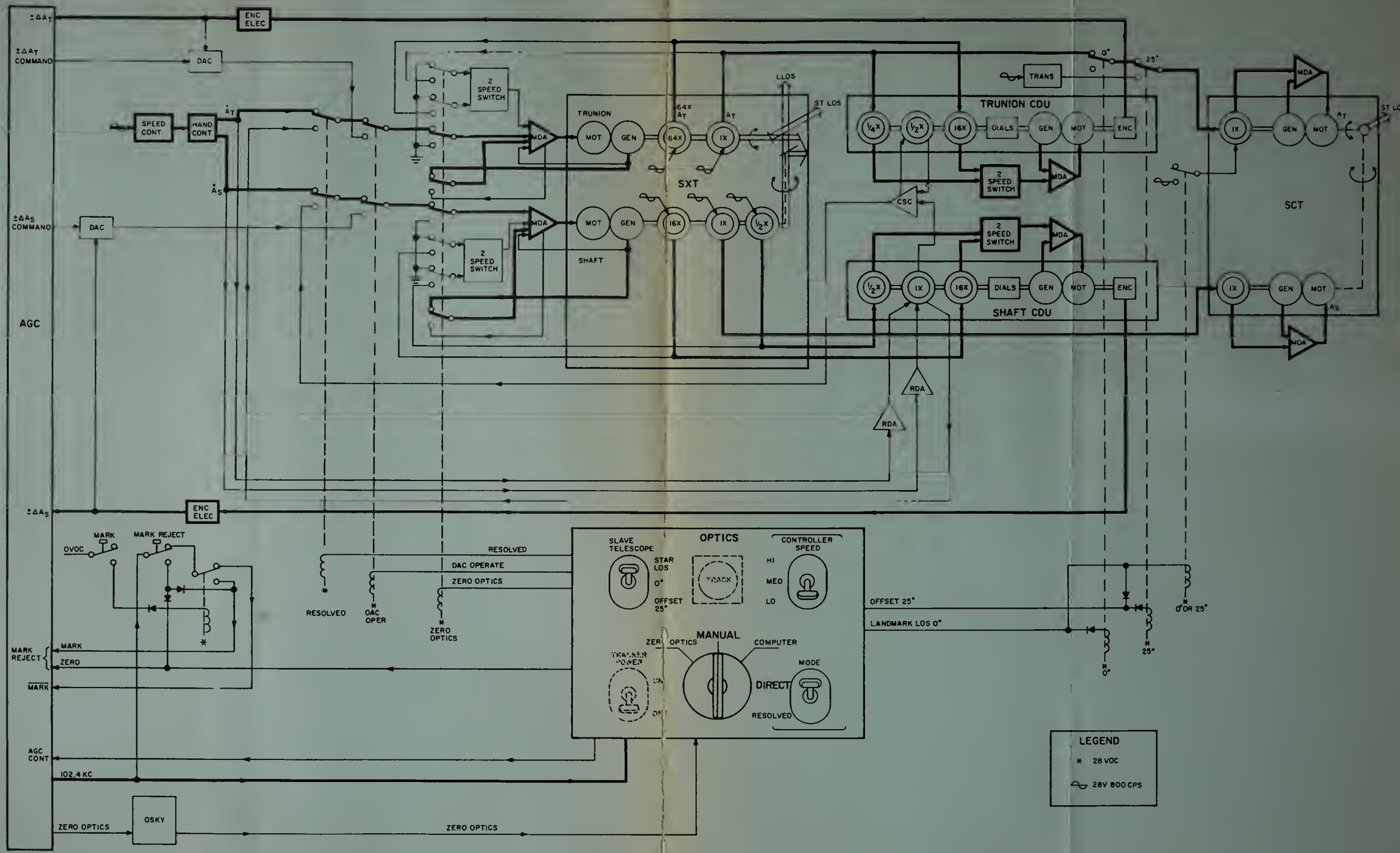
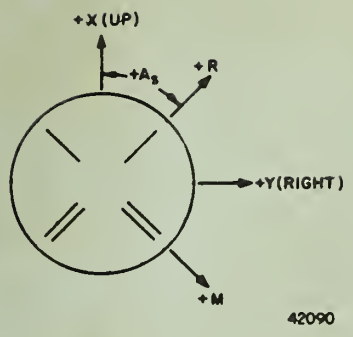


Figure 12-3. Manual Direct Mode



Controller Mode	Controller Motion	Apparent Target Image Motion	CDU Trunnion Readout and SXT Trunnion Angle	CDU Shaft Readout and SXT Shaft Angle
Direct Mode	Down	+ R	Decrease	
	Up	- R	Increase	
	Left	+ M		Decrease
	Right	- M		Increase
Resolved Mode	Down	- X	Increase	Decrease
	Up	+ X	Decrease	Increase
	Left	- Y	Increase	Increase
	Right	+ Y	Decrease	Decrease

In direct mode: Movement is along a coordinate system that is rotated through angle A_S.

In resolved mode: Movement is along an X-Y axis (independent of A_S).

Figure 12-4. Sextant Image Motion

12.2.2.2 Manual Resolved Operation. The manual resolved mode mechanization is shown in figure 12-5. When in this mode, the hand controller outputs are routed through a matrix transformation prior to being directed to the shaft and trunnion motor drive amplifiers. The matrix transformation makes the image motion correspond directly to the hand controller motion. That is, up, down, right and left motions of the hand controller commands the target image to move up, down, right and left, respectively, in the field of view. In other words, the image motion is in the X-Y spacecraft coordinate system. The matrix transformation takes place in two steps. The outputs of the hand controller are routed to the resolver drive amplifiers (RDA) and then to the 1X resolver in the shaft CDU. Here the drive signals $\dot{A}_S$ and $\dot{A}_t$, are transformed by the sine and cosine functions of the shaft angle (A_S). One of the two outputs of the 1X resolver is sent to the SXT trunnion motor drive amplifier. The second output is then resolved through the trunnion angle (A_t) so that the target image motion will be independent of trunnion angle. This is accomplished by the cosecant computing amplifier (CSC) and the 1/2X computing resolver in the trunnion CDU. See figure 12-6 for a simplified diagram of the shaft drive gain variations. The net result is that the shaft drive rate, $\dot{A}_S$ is inversely proportional to the sine of the trunnion angle A_t. The speed controller is also operational in this mode.

12.2.2.3 Slave Telescope Modes. The slave telescope modes provide for alternate operation of the telescope trunnion while the SXT is being operated. The alternate modes are selected by the slave telescope switch on the mode control panel. There are three possible selections, star LOS, 0^o and OFFSET 25^o. With this switch in the star LOS position the SCT trunnion axis is slaved to the SXT trunnion and is the normal operating position for the SCT. With the switch in the 0^o position, the SCT trunnion is driven to a zero degree position by the application of a fixed voltage to the SCT trunnion 1X receiving resolver. This will cause this position loop to null in a zero orientation. Therefore, the center line of the SCT 60^o field-of-view is held parallel to the LLOS of the SXT.

With the switch in the 25^o offset position, an additional external voltage is applied to the same 1X receiving resolver which will cause the SCT trunnion position loop to null out so that the center line of the 60^o field-of-view is offset 25^o (A_t of SCT at 12.5^o) from the LLOS of the SXT. This position of the SCT trunnion will allow the landmark to remain in the 60^o field-of-view while still providing a total possible field-of-view of 110^o if the SCT shaft is swept through 360^o.

12.2.3 COMPUTER MODE OPERATION. The computer controlled operation is selected by placing the moding switch in computer position. The mechanization of this loop is shown in figure 12-7. The functional operation to be performed by the optics is then chosen by the computer program that has been selected by the astronaut. In the computer mode, the optics can be zeroed or the SXT trunnion and shaft can be positioned under computer control. The selection of zero optics as commanded by the computer requires that specific relays in the DSKY be selected by the computer which initiates the zero optics mode as describe in paragraph 12.2.1. The operation of the SXT under computer control is accomplished by activating the digital to analog converters (DAC). The computer can then provide a direct input to the shaft and trunnion MDA's via the DAC. The DAC's (previously described in ISS paragraph 4.2.3) accept digital pulse trains from the computer and convert this pulse train to 800 cycle signals which are used as inputs to the MDA. The MDA then positions the SXT and the CDU's follow the position of the SXT. The encoders in the CDU's provide digital outputs proportional to the amount of SXT movement. These encoder digital outputs are used for two purposes, (1) they provide a digital input to the

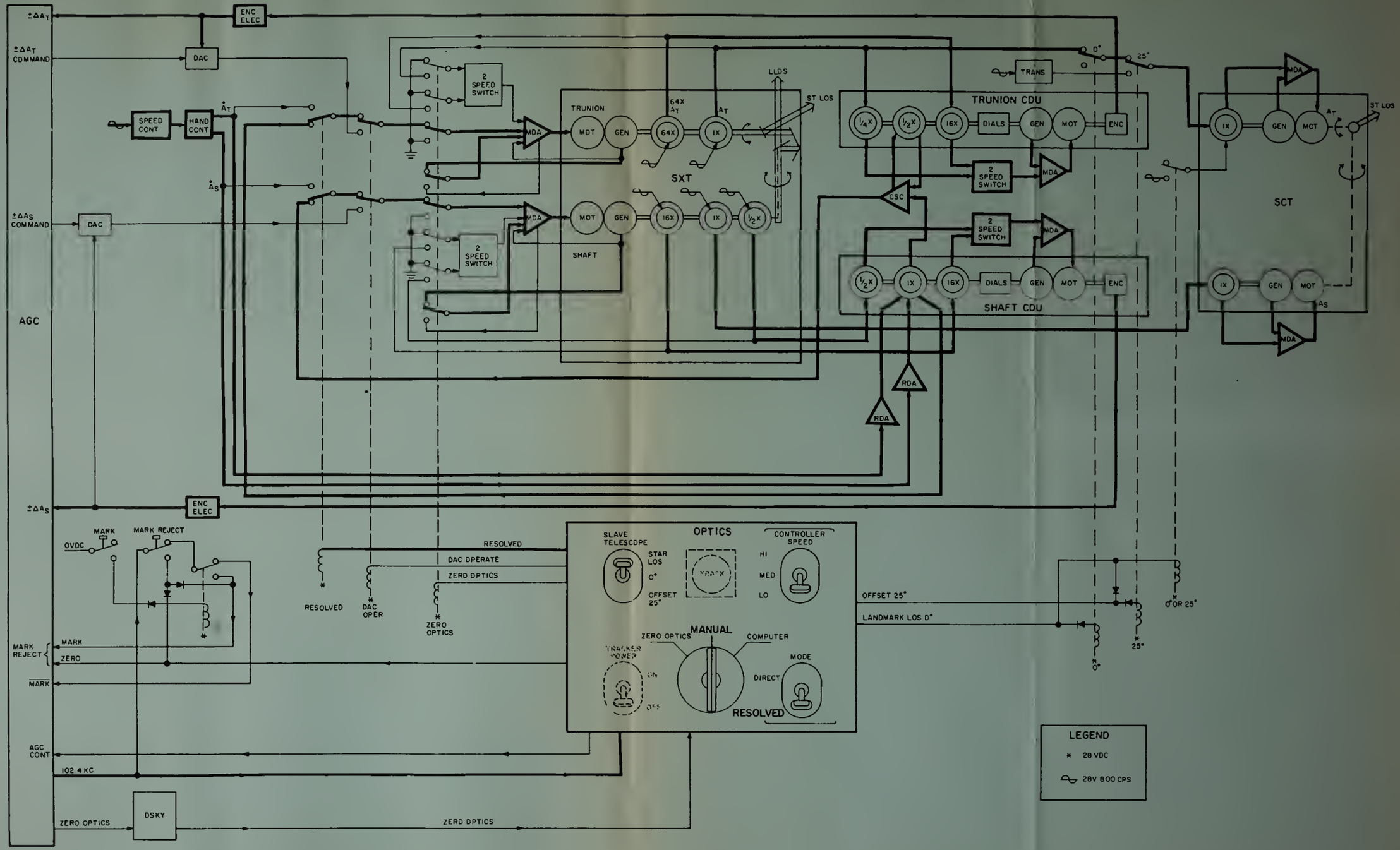
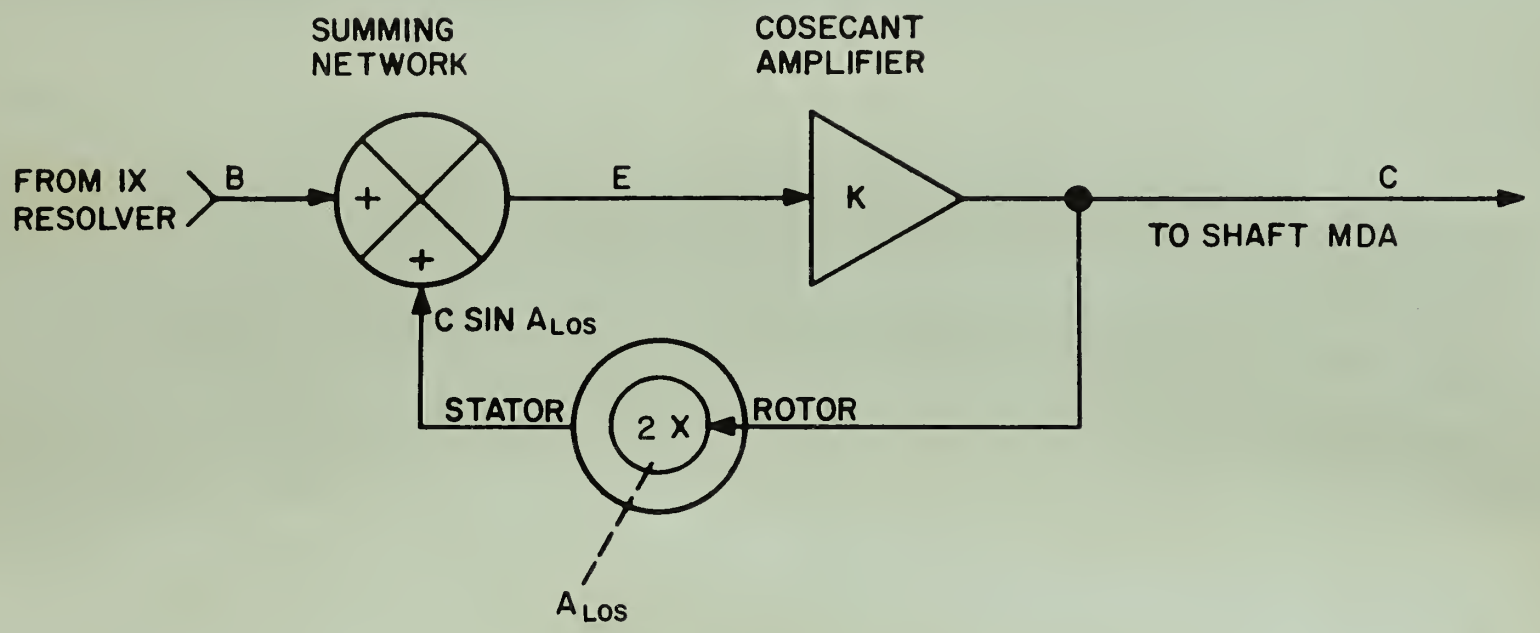


Figure 12-5. Manual Resolved Mode



$$B = \dot{A}_t \text{ Sin } As - \dot{A}s \text{ Cos } As$$

$$E = B + C \text{ Sin } A_{LOS}$$

$$C = KE$$

$$C = K(B + C \text{ Sin } A_{LOS}) = KB + KC \text{ Sin } A_{LOS}$$

$$C - KC \text{ Sin } A_{LOS} = KB$$

$$C\ (1 - K \text{ Sin } A_{LOS}) = KB$$

$$C = \frac{KB}{1 - K \text{ Sin } A_{LOS}}$$

$$C = \frac{B}{1/K - \text{Sin } A_{LOS}} \quad (K \longrightarrow \infty)$$

$$C = \frac{-B}{\text{Sin } A_{LOS}} = \frac{\dot{A}s \text{ Cos } As - \dot{A}_t \text{ Sin } As}{\text{Sin } A_{LOS}}$$

Figure 12-6. Gain Variation-Simplified Diagram

computer to record the position of the SXT, and (2) they provide a feedback to the DAC, for the purpose of maintaining linear operation of the loop. That is, each pulse that is supplied to the DAC by the AGC in turn receives a like pulse from the encoder which would decrease the DAC output proportionally. This mode is used when the astronaut desires to look at a specific star for which the computer has the corresponding star coordinates. The computer will also know the attitude of the spacecraft from inputs from the ISS CDU's and will therefore be able to calculate the position of SXT axes that are required to acquire the star. The computer, having calculated these positions, can then torque the SXT shaft and trunnion axes the required amount via the DAC.

12.3 SUMMARY

The optical mechanization consists of SXT trunnion and shaft integrating servo loops which position the SXT lines of sight in response to inputs from either the hand controller or the AGC. In response to SXT movements, position servo loops drive the trunnion and shaft CDU's and the SCT trunnion and shaft axes, so as to maintain the same angular orientation as the SXT trunnion and shaft axes. Controlling switches are located on the G&N indicator panel and allow the selection of three primary modes, zero optics, manual operation and computer operation.

The purpose of the zero optics mode is to drive the optical equipment to an initial orientation prior to their utilization in taking an optical sighting. This allows the computer to clear the optical counters which are to be incremented with new data during the process of taking an optical sighting.

The manual mode allows the astronaut to control the SXT operation via the hand controller. There are two variations of this mode, manual direct and manual resolved. In manual direct, the star image moves in the variable R-M coordinate system, while in the manual resolved mode, the star image moves in a fixed X - Y coordinate system.

The computer mode is selected by the astronaut to provide for computer control of the optics. The AGC can then zero the optics and drive the SXT via program control.

REVIEW QUESTIONS FOR SECTION XII

T F 1. The SCT is under the direct control of the optics hand controller.

T F 2. The CDU's are slaved to the SXT shaft and trunnion axes by coarse-fine resolver systems.

T F 3. When the "Mark" button is pressed, a relay is energized which completes a circuit to the AGC indicating that the position of the CDU's should be recorded.

4. Explain briefly the purpose of the zero optics mode.

5. Explain the manual resolved mode of operation.

SECTION XIII

INTRODUCTION TO THE APOLLO GUIDANCE COMPUTER

INTRODUCTION

The computer subsystem (CSS) consists of the Apollo Guidance Computer (AGC), the navigation panel display and keyboard (navigation panel DSKY) and the main panel display and keyboard (main panel DSKY). These units are shown in figures 13-1 and 13-2. The AGC is a digital computer and is the major unit of the CSS. The DSKY's provide a two way communication interface between the astronauts and the AGC. For the most part, the DSKY's are functionally identical. They will be discussed in detail in Section XV.

13.1 BRIEF AGC FUNCTIONAL DESCRIPTION

The AGC (figure 13-1) is the processing center of the G&N System. It is both a general purpose and control computer. The AGC performs calculations and control functions according to a series of instructions which are a result of conditions both internal and external to the AGC.

13.1.1 AGC CAPABILITIES. The AGC provides the following capabilities for the Apollo Mission:

1. It solves the guidance and navigation problems required for all phases of the Apollo Mission. This falls under the "general purpose" category.

   A. Orbital Integration. Given pertinent data, the AGC can calculate, at time T_N, the state vector of the spacecraft at time T_X where $X > N$.

   B. Thrust Vector Control Calculations. During a thrust maneuver, the AGC can calculate V_G (velocity-to-be-gained), $\dot{V}_G$ (acceleration-to-be-gained) and form their cross product. The cross product is then used by the G&N System and other spacecraft systems to steer the spacecraft to a given point in space at a given time.

2. It controls the G&N System and other spacecraft systems. This falls under the "control" category.

EXAMPLES

The AGC -

A. positions the stable member,

B. positions the optical unit,

C. turns the SPS engine ON and OFF,

D. generates timing waveforms which are used throughout the spacecraft for synchronization purposes.

3. It maintains cognizance of its own operation, i.e., the AGC can detect many of its own malfunctions.

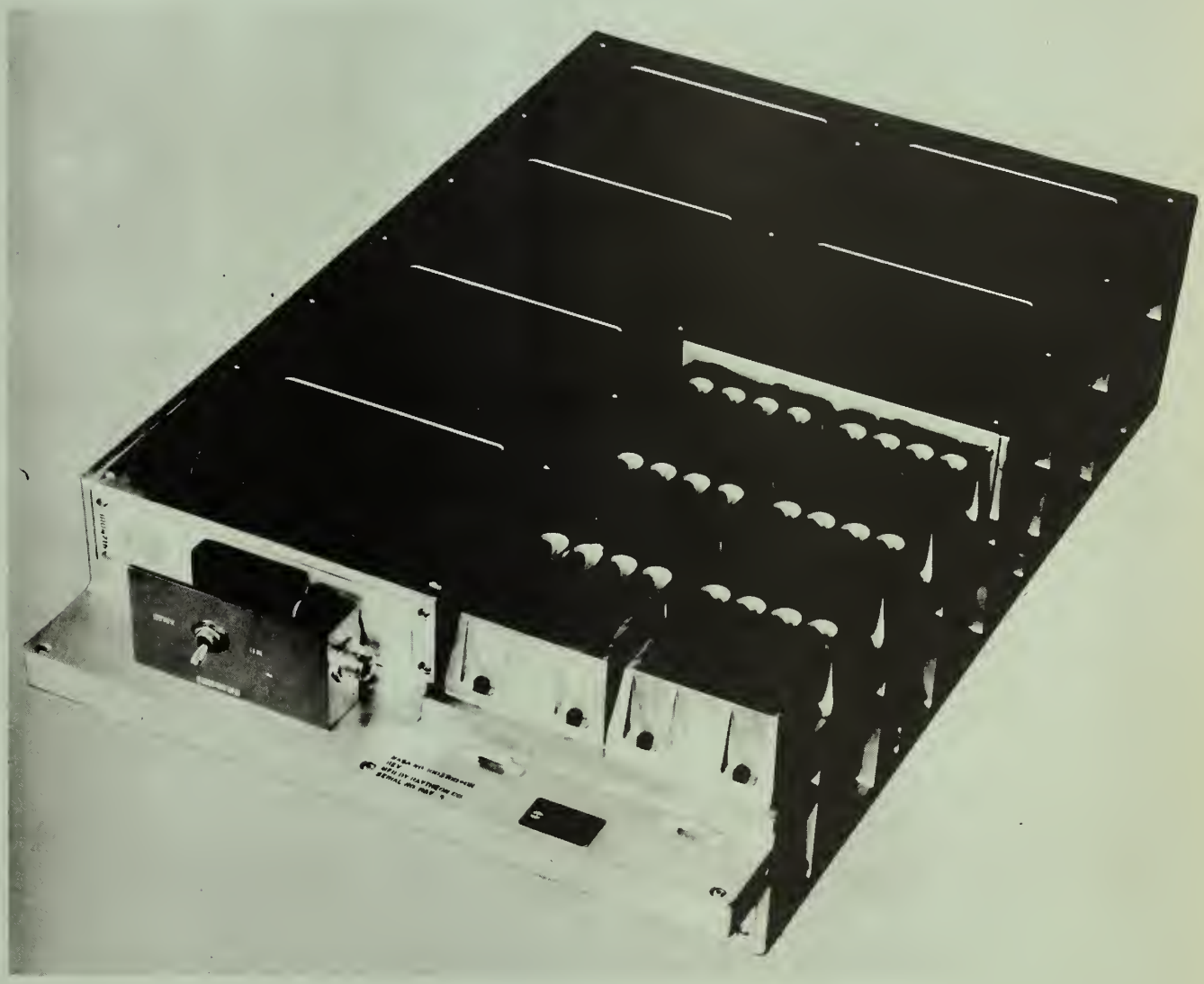
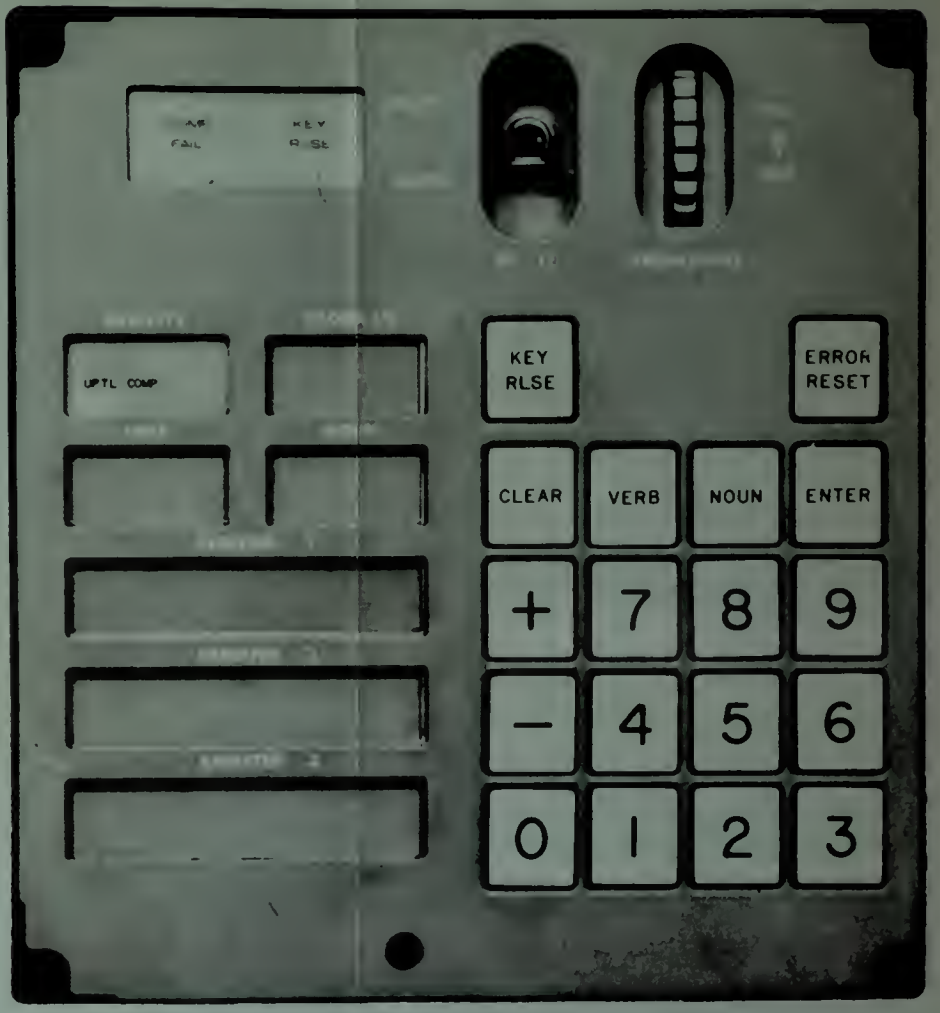


Figure 13-1. Apollo Guidance Computer

NAVIGATION
PANEL DSKY



MAIN PANEL DSKY

Figure 13-2. Display and Keyboards

13.2 BRIEF AGC PHYSICAL DESCRIPTION

The AGC measures 22 x 15 x 5.5 inches and weighs 88 pounds. It contains approximately 4300 logic gates and consumes 120 watts of power. It is located beneath the PSA and is mounted on a coldplate base made of aluminum alloy. The base is a honeycombed structure which is cooled by water glycol. Its function is to dissipate heat generated by the AGC.

The AGC consists of a logic tray assembly and a memory tray assembly which are mounted back to back (figures 13-3 and 13-4). A tray assembly consists of a tray and the modules and connectors mounted on it. The modules contain the AGC's circuitry. The connectors provide the AGC with a hardware interface. When the AGC is mounted in the spacecraft, the memory tray assembly sits above the logic tray assembly.

13.2.1 LOGIC TRAY A. The following modules and connectors are mounted on logic tray A (figure 13-3):

1. 36 Logic Modules. These modules contain the AGC's logic circuitry.

2. 4 Interface Modules. These modules contain the circuits which condition the AGC's inputs and outputs.

3. 360 Pin Front Connector. This connector provides a hardware interface between the AGC, DSKY's and other areas of the spacecraft.

4. 126 Pin Front Connector. This connector is used while the AGC is being tested on the ground. It is not connected during flight.

5. 172 Pin Rear Connector. This connector provides the interface between the logic tray assembly and the memory tray assembly.

13.2.2. MEMORY TRAY B. The following modules and connectors are mounted on memory tray B (figure 13-4):

1. 25 Modules. These modules contain the circuitry associated with the AGC's memory and power supplies.

2. 19 Pin Front Connector. This connector provides the hardware interface between the AGC and the +28 VDC prime power source.

3. 172 Pin Rear Connector. This connector provides the interface between the memory tray assembly and the logic tray assembly.

There is a STBY/ON (standby/on) switch mounted on the front of this tray. This switch provides a standby mode of operation for conservation of power.

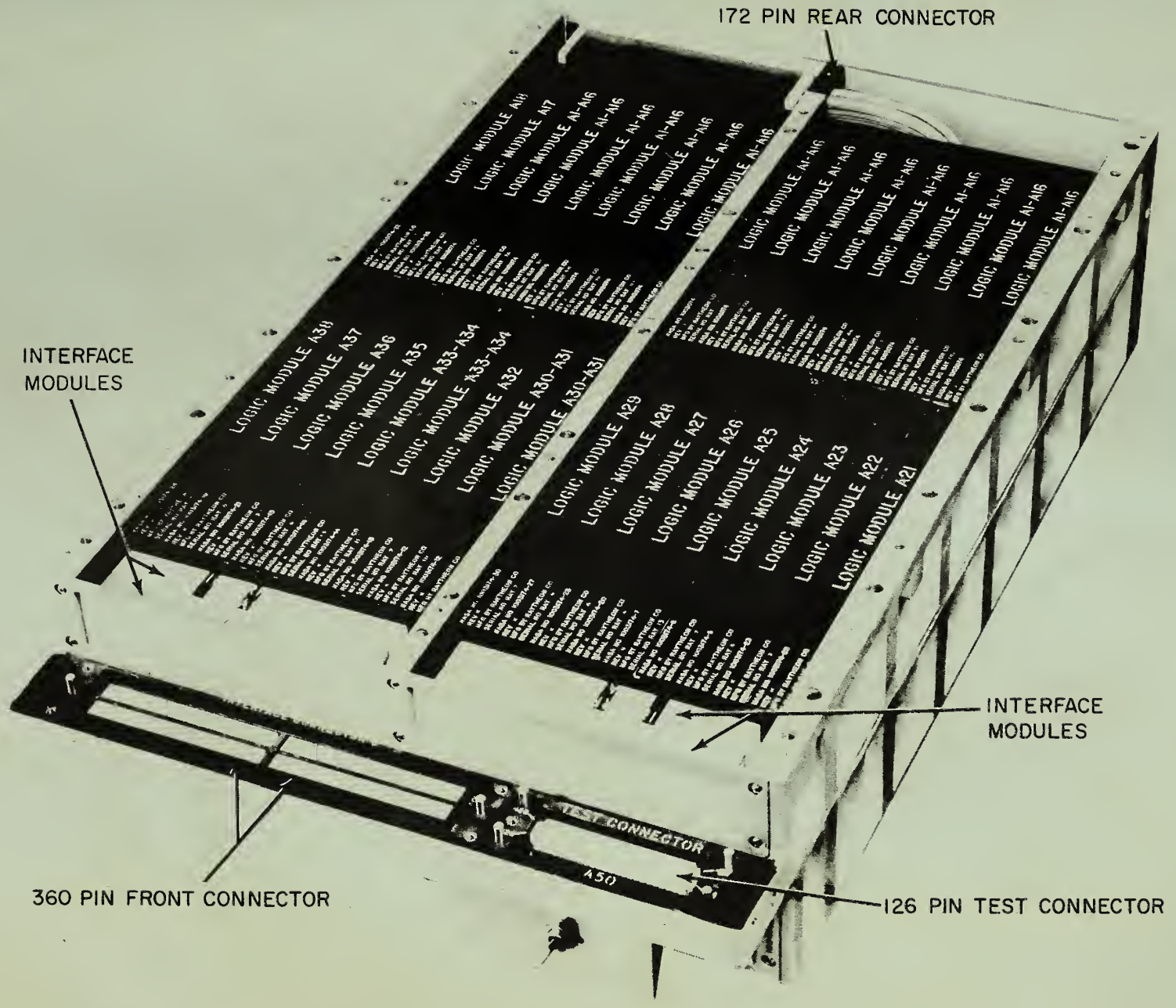


Figure 13-3. Logic Tray A

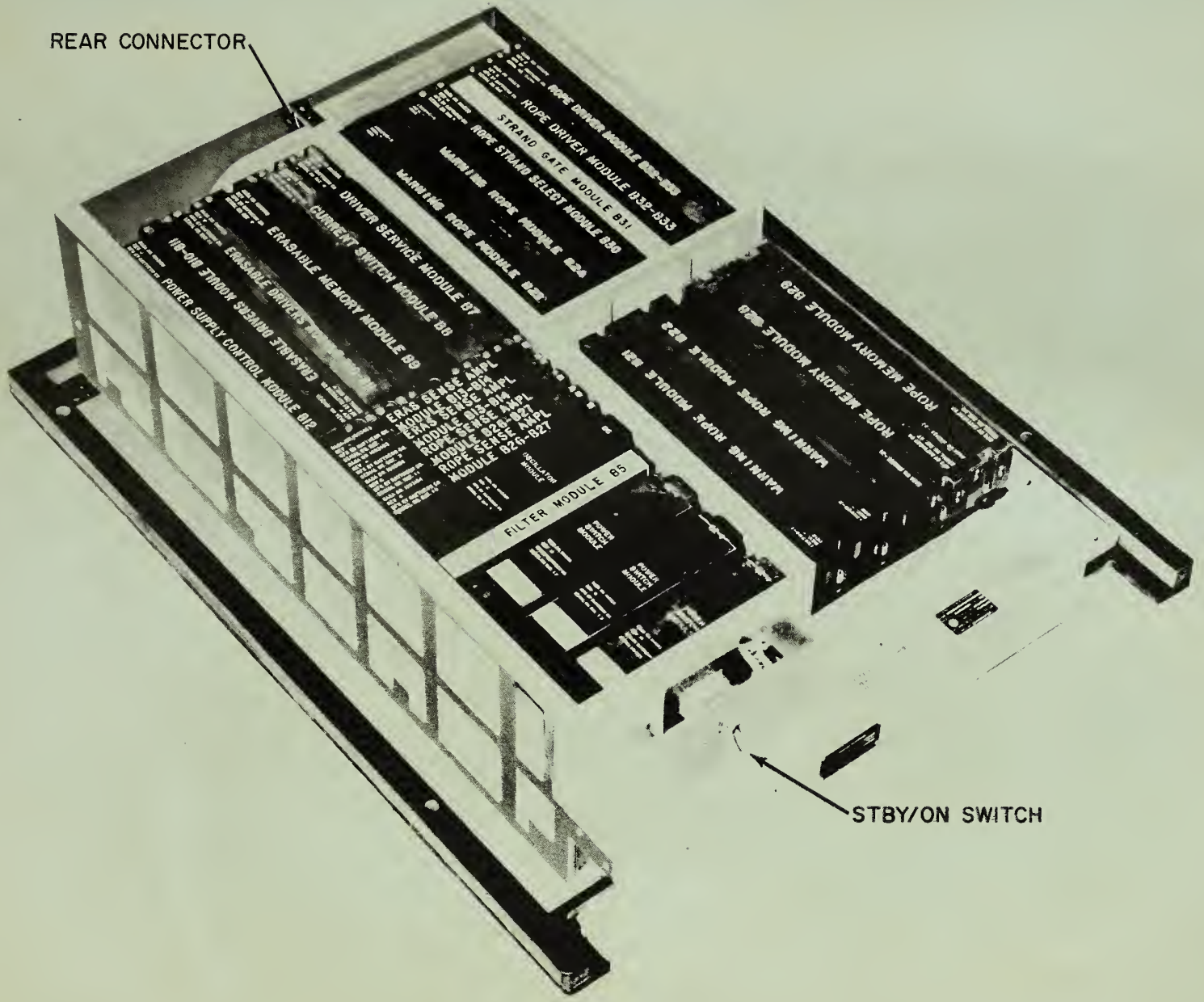


Figure 13-4. Memory Tray B

13.3 AGC ORGANIZATION

Figure 13-5 is a gross block diagram of the AGC. This diagram should be referenced while reading 13.3, 13.4 and 13.5. In Section XIV, the AGC will be shown in greater detail.

The AGC is functionally divided into seven blocks:

1. Timer
2. Sequence Generator
3. Central Processor
4. Memory
5. Priority Control
6. Input - Output
7. Power

13.3.1 TIMER. The timer generates all the necessary synchronization pulses to insure a logical data flow from one area to another within the AGC. It also generates timing waveforms which are used by (1) the AGC's alarm circuitry and (2) other areas of the spacecraft for control and synchronization purposes.

13.3.2 SEQUENCE GENERATOR. The sequence generator directs the execution of machine instructions. It does this by generating control pulses which logically sequence data throughout the AGC. The control pulses are formed by combining the order code of an instruction word with synchronization pulses from the timer.

13.3.3 CENTRAL PROCESSOR. The central processor performs all arithmetic operations required of the AGC, buffers all information coming from and going to memory, checks for correct parity on all words coming from memory and generates a parity bit for all words written into memory.

13.3.4 MEMORY. Memory provides the storage for the AGC and is divided into two sections: erasable memory and fixed memory. Erasable memory can be written into or read from; its readout is destructive. Fixed memory cannot be written into and its readout is nondestructive.

13.3.5 PRIORITY CONTROL. Priority control establishes a processing priority of operations which must be performed by the AGC. These operations are a result of conditions which occur both internally and externally to the AGC. Priority control consists of counter priority control and interrupt priority control. Counter priority control initiates actions which update counters in erasable memory. Interrupt priority control transfers control of the AGC to one of six interrupt subroutines (priority programs) stored in fixed memory.

13.3.6 INPUT - OUTPUT. The input - output section routes and conditions signals between the AGC and other areas of the spacecraft.

13.3.7 POWER. This section provides voltage levels necessary for the proper operation of the AGC.

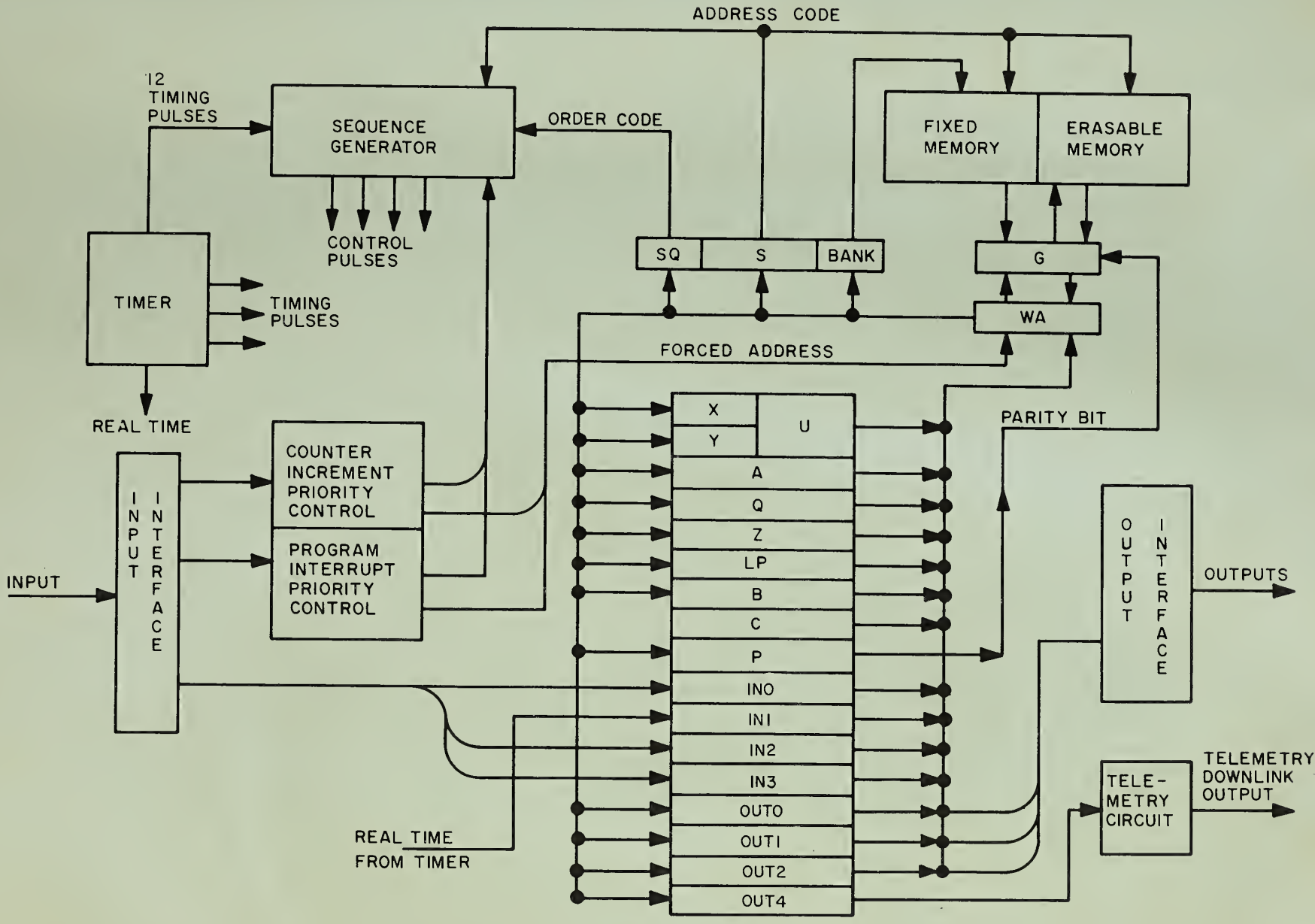


Figure 13-5. AGC Block Diagram

13.4 PERTINENT AGC CHARACTERISTICS

The following is a brief discussion of several AGC characteristics listed in table 13-1. All the characteristics will be discussed in detail in Section XIV.

1. Internal Transfer. Parallel internal transfer implies that all bits of a word are transferred simultaneously when a word is routed from one area to another within the AGC.

2. Hardware Registers. A hardware register is a flip-flop register. Most of the AGC's hardware registers consist of 16 flip-flops and their associated read and write gates.

3. Machine Instructions. A machine instruction is one the AGC can directly interpret and execute. Machine instructions are divided into three groups: regular, involuntary and miscellaneous. Regular instructions consist of an order code and a relevant address. They are divided into two groups: basic and extra-code. Involuntary instructions are associated with priority control. Miscellaneous instructions are associated with testing the AGC on the ground. All machine instructions consist of one or more subinstructions. A subinstruction takes one MCT to perform.

4. Counters. A counter is a 16 bit (word) location in erasable memory which is updated when certain conditions (counter interrupts) occur. A counter is not a flip-flop register.

5. Logic. The AGC employs positive logic. Positive logic implies that the voltage level associated with a logic 1 is algebraically higher than the voltage level associated with a logic 0.

6. Parity. The AGC uses odd parity; i.e., all words stored in memory contain an odd number of logic 1's. This condition makes it possible for the AGC to detect a malfunction when a word is incorrectly transferred from memory.

13.5 AGC INFORMATION FLOW

The main functions of the AGC are implemented through the execution of programs stored in memory. Programs are written in basic instructions. The order code defines data flow within the AGC. The relevant address selects data that is to be used for computations. The order code of each instruction is entered into the sequence generator which controls data flow and produces a different sequence of control pulses for each instruction. Each instruction is followed by another instruction. In order to specify the sequence in which consecutive instructions are to be executed, the instructions are normally stored in successive memory locations. By adding +1 to the address of an instruction being executed, the address of the next instruction is obtained. Execution of an instruction is complete when the order code of the next instruction is transferred to the sequence generator and its relevant address is in the central processor.

The central processor consists primarily of flip-flop registers. It performs arithmetic operations and data manipulations on information accepted from memory, the input registers and priority control. Arithmetic operations are performed using the binary ones complement numbering system. All operations within the central processor are performed under control of pulses generated by the sequence generator.

The AGC has provisions for six priority programs: T3 RUPT, RUPT 2, T4 RUPT, KEYRUPT, UPRUPT, DOWNRUPT. The T3 RUPT and T4 RUPT interrupt subroutines are initiated under program control at specified time intervals. The DOWNRUPT subroutine is used when converting parallel information to serial information for downlink telemetry. The remaining program interrupts are initiated by inputs external to the AGC.

Table 13-1. Pertinent AGC Characteristics

Characteristics	Description
Computer type	automatic, electronic, digital, general purpose and control
Internal transfer	parallel
Memory	random access (primarily)
Erasable	coincident current core type, capacity = 1024 words
Fixed	core-rope type, capacity = 24,576 words
Word length	16 bits
Number system	binary ones complement
Hardware registers	22 total
Circuitry type	NOR micrologic
Machine instructions	21 total
Priority program options	6 total
MCT (memory cycle time)	11.7 μ seconds = 12 "action" times
Add time	23 μ seconds (2 MCT's)
Multiply time	117 μ seconds (10 MCT's)
Counters	20 total
Basic clock oscillator	2.048 mc
AGC power supplies	+3 VDC +13 VDC
Logic	positive: logic 1 = +3 VDC, logic 0 = 0 VDC
Parity	odd

Before a priority program can be executed, the current program must be interrupted; however, certain information about the current program must be preserved. This information includes the program counter contents and any intermediate results contained in the central processor. The program counter is a register in the central processor which contains the address of the next instruction to be performed. The priority control produces an interrupt request signal which is sent to the sequence generator. This signal causes the execution of an instruction that transfers the current contents of the program counter and any intermediate results to memory. In addition, the control pulses transfer the priority program address to the central processor and then to memory. As a result, the first instruction word of the priority program is entered into the central processor from memory and the execution of the priority program is begun. The last instruction of each priority program restores the AGC to normal operation if no other interrupt request is present. This is done by transferring the previous program counter and intermediate results from their storage locations in memory back to the central processor.

Certain data pertaining to the flight of the spacecraft is used to solve the guidance and navigation problems required for the Apollo Mission. This data which includes real time, acceleration and IMU gimbal angles (via the CDU's) is stored in the erasable memory counters which are updated as soon as new data becomes available. An incrementing process which changes the contents of the counters is implemented by priority control between the execution of subinstructions. Data inputs to counter priority control are called incremental pulses. Each incremental pulse produces a counter address and a priority request signal which is sent to the sequence generator where it functions as an order code. The control pulses produced by the sequence generator transfer the counter address to memory. In addition, the control pulses enter the contents of the addressed counter into the central processor. The contents of the counter are then incremented or decremented.

Real time plays a major role in solving guidance and navigation problems. Real time is maintained within the AGC by the main time counter. The main time counter consists of two erasable memory counters. Incremental pulses are produced in the timer and sent to priority control for incrementing the main time counter every 10 milliseconds.

Continuous drive pulses originate in the AGC's timer. Rate signals, which are bursts of these drive pulses, are used to drive the inertial CDU's, the gyros and the optical CDU's. Rate signals are also used for controlling the attitude of the spacecraft. The number of pulses in each burst and occurrence of each burst are controlled by the program. The destination of the various rate signals, as well as the type of rate signals, are also selected by the program. The continuous drive signals are also sent to other areas of the spacecraft where they are used for synchronization and control purposes.

The uplink word from the spacecraft telemetry system is supplied to the AGC as incremental pulse inputs to priority control. As these words are received, priority control produces the address of the uplink counter in memory and requests the sequence generator to execute the instructions which perform the serial-to-parallel conversion of the uplink word. When the serial-to-parallel conversion is complete, the parallel word is transferred to a storage location in memory by the UPRUPT subroutine.

With the DSKY keyboard, the astronaut can load information into the AGC, receive and display information contained in the AGC and initiate any program stored in memory. A keycode is assigned to each keyboard pushbutton. When a keyboard pushbutton on either DSKY is depressed, the keycode is produced and sent to the AGC where it produces the address of a priority program (KEYRUPT) stored in memory and a priority request signal which is sent to the sequence generator. The priority request signal functions as an order code and initiates an instruction for interrupting the program in progress and executing the priority program stored in memory. A function of this program is to decode and process the keycode. A number of keycodes are required to specify an address or a data word. The program initiated by a keycode converts the information from the DSKY keyboard to a coded display format which is transferred to the display portion of the DSKY. The display informs the astronaut that the keycode was received, decoded and properly processed by the AGC.

13.6 SUMMARY

The CSS consists of the AGC, the navigation panel DSKY and the main panel DSKY. The AGC is a digital computer and is the major unit of the CSS. The DSKY's provide a two way communication interface between the astronauts and the AGC.

The AGC is both a general purpose and control computer which performs calculations and control functions according to a series of instructions which are a result of conditions both internal and external to the AGC. The AGC performs three major tasks for the Apollo Mission: it solves all the guidance and navigation problems, it controls the G&N System and parts of other spacecraft systems, it provides its own malfunction detection.

The AGC is divided into seven functional blocks: timer, sequence generator, central processor, memory, priority control, input - output and power. The timer generates the synchronization pulses which insure a logical data flow from one area to another within the AGC. The sequence generator directs the execution of machine instructions. The central processor performs all arithmetic operations required of the AGC and checks for correct parity. The memory provides the AGC's storage. Priority control establishes a processing priority of operations which must be performed by the AGC. The input - output routes and conditions signals between the AGC and other areas of the spacecraft. The power functional block provides voltage levels necessary for the proper operation of the AGC.

With a DSKY, the astronaut can load information into the AGC, receive and display information contained in the AGC and initiate any program stored in the AGC's memory.

REVIEW QUESTIONS FOR SECTION XIII

1. The CSS consists of three units. List them.

   A.

   B.

   C.

2. Where is the AGC located?

3. List the seven functional blocks of the AGC.

   A.

   B.

   C.

   D.

   E.

   F.

   G.

4. Why aren't the counters located in fixed memory?

5. The AGC uses the _____ numbering system.

6. How can the astronauts load information into the AGC?

SECTION XIV

APOLLO GUIDANCE COMPUTER

INTRODUCTION

This section of the study guide describes (1) the AGC hardware and its organization, (2) the instructions used by the AGC and (3) the AGC's interface with other areas of the spacecraft. The text and illustrations have been generated to give the reader a thorough functional knowledge of AGC's hardware.

14.1 WORD FORMATS

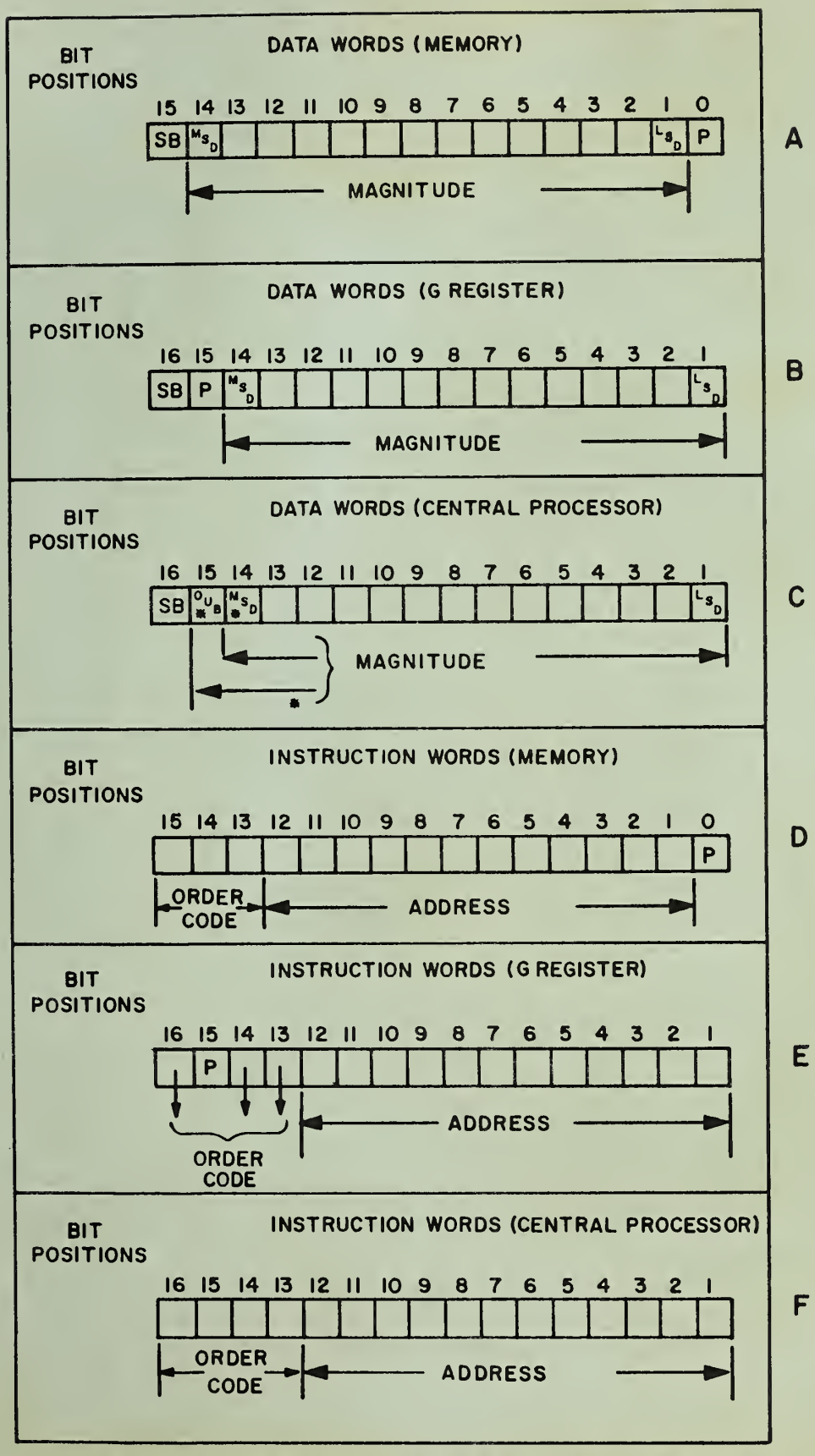
There are two types of words associated with the operation of the AGC: data words and instruction words. These words are 16 bits long and are located in memory and the central processor registers. Figure 14-1 shows the word formats in these areas. Note that the bit positions in memory are labeled 0 through 15 and that the bit positions in the central processor registers are labeled 1 through 16. When a word is transferred from memory to the central processor, bit 15 of the memory word is sent to bits 15 and 16 of the central processor register. Bits 14-1 of the memory word are routed to bits 14-1 of the central processor register. After the central processor word has been manipulated, bits 15 and 16 may differ. Figure 14-1 details the format of the G register which is a central processor register. Note that its format differs from those of the other central processor registers. The G register will be discussed in 14.5. The text under headings 14.1.1 and 14.1.2 will refer primarily to A, C, D and F of figure 14-1.

14.1.1 DATA WORDS. In memory, data words contain a parity bit, 14 magnitude bits and a sign bit. A logic 1 in the sign bit indicates a negative number; a logic 0 in the sign bit indicates a positive number. Bit position 1 contains the least significant digit (LSD) of the magnitude; bit position 14 contains the most significant digit (MSD) of the magnitude. The parity bit is a logic 1 if bit positions 1 through 15 contain an even number of logic 1's; the parity bit is a logic 0 if bit positions 1 through 15 contain an odd number of logic 1's.

In the central processor, data words contain a sign bit, overflow/underflow bit and 14 or 15 magnitude bits. The overflow/underflow bit is used, in some cases, as a magnitude bit after the data word has been manipulated in the central processor. Bit position 1 contains the LSD and bit position 14 or 15 contains the MSD. Note that the parity bit is included in the G register but not the other central processor registers.

14.1.2 INSTRUCTION WORDS. In memory, instruction words contain a three bit order code (op code), a parity bit and a twelve bit address code. The order code defines an operation that is to be performed. The address code specifies the location of data to be used in this operation.

In the central processor, instruction words contain a four bit order code and a twelve bit address code. The extra bit in the order code enables the definition of eleven rather than eight regular instructions. Again note that there is not a parity bit in the central processor registers.



* AFTER MANIPULATION, BIT POSITION 15 SOMETIMES CONTAINS MSD

Figure 14-1. Word Formats

14.2 ADDITION SCHEMES

The AGC performs angular data addition and non-angular data addition. The processes involved with these manipulations differ slightly.

14.2.1 NON-ANGULAR DATA ADDITION. The AGC uses the binary ones complement numbering system. In this system, a negative number is the complement of the corresponding positive number. Assume that the AGC uses five bit data words. Figure 14-2 shows how +7 through -7 would be represented by words in memory and the central processor.

The AGC can only add. In order to subtract, the AGC adds the complement of a number. Multiplications are performed by successive additions and shiftings; divisions are performed by successive additions of complements and shiftings.

All adding is performed in the central processor. The AGC's adder consists of the X, Y and U registers. The X and Y registers are the adder's input registers, i.e., the registers to which the augend and addend are applied. The U register is the adder's output register, i.e., the register at which the sum is found. An overflow occurs during addition when the overflow/underflow bit of the U register is a logic 1 and the sign bit is a logic 0; an underflow occurs when the overflow/underflow bit is a logic 0 and the sign bit is a logic 1.

Figure 14-3 shows the various addition schemes employed by the AGC for manipulating non-angular data. Note in the first case of Example C that the AGC performs (+5) + (-3) and not (+5) - (+3). Example A shows a case of overflow. Example B illustrates end-around-carry and underflow. End-around-carry is a characteristic of the binary ones complement numbering system: it is the result of a carry being generated during the addition of the last two binary bits. When this happens, +1 is added to the LSD of the subsum and the sum is then formed. Underflow results when a sum is negative and has a magnitude larger than that expressable with the assigned magnitude bits. End-around-carry and overflow/underflow conditions are mechanized by the AGC. When overflow/underflow occurs, a special counter is incremented or decremented to prevent loss of data.

Summarizing: If the SB and OUB of the sum are identical, then the sign of the sum is determined by the SB, and the magnitude of the sum is determined by the assigned magnitude bits, i.e., the OUB is not taken into consideration; if the SB and OUB of a sum are not identical, then the sign of the sum is determined by the SB, and the magnitude of the sum is determined by the assigned magnitude bits and the OUB. In this case, the OUB becomes the MSD.

One important fact should be noted: the configuration of the magnitude 0 (zero) is not unique but has signs associated with it, i.e.,+0 = 00000 and -0 = 11111 in the central processor registers.

14.2.2 ANGULAR DATA ADDITION. The AGC receives pulses indicative of angular displacements from the optical and inertial CDU's. These pulses enter the AGC through the input interface and are then applied to the counter priority control circuitry. One counter is associated with each CDU.

SB	M	M	M	P	
0	1	1	1	0	+7
0	1	1	0	1	+6
0	1	0	1	1	+5
0	1	0	0	0	+4
0	0	1	1	1	+3
0	0	1	0	0	+2
0	0	0	1	0	+1
0	0	0	0	1	+0
1	1	1	1	1	-0
1	1	1	0	0	-1
1	1	0	1	0	-2
1	1	0	0	1	-3
1	0	1	1	0	-4
1	0	1	0	1	-5
1	0	0	1	1	-6
1	0	0	0	0	-7

MEMORY

SB	OUB	M	M	M	
0	0	1	1	1	+7
0	0	1	1	0	+6
0	0	1	0	1	+5
0	0	1	0	0	+4
0	0	0	1	1	+3
0	0	0	1	0	+2
0	0	0	0	1	+1
0	0	0	0	0	+0
1	1	1	1	1	-0
1	1	1	1	0	-1
1	1	1	0	1	-2
1	1	1	0	0	-3
1	1	0	1	1	-4
1	1	0	1	0	-5
1	1	0	0	1	-6
1	1	0	0	0	-7

CENTRAL PROCESSOR

Figure 14-2. Number Representation

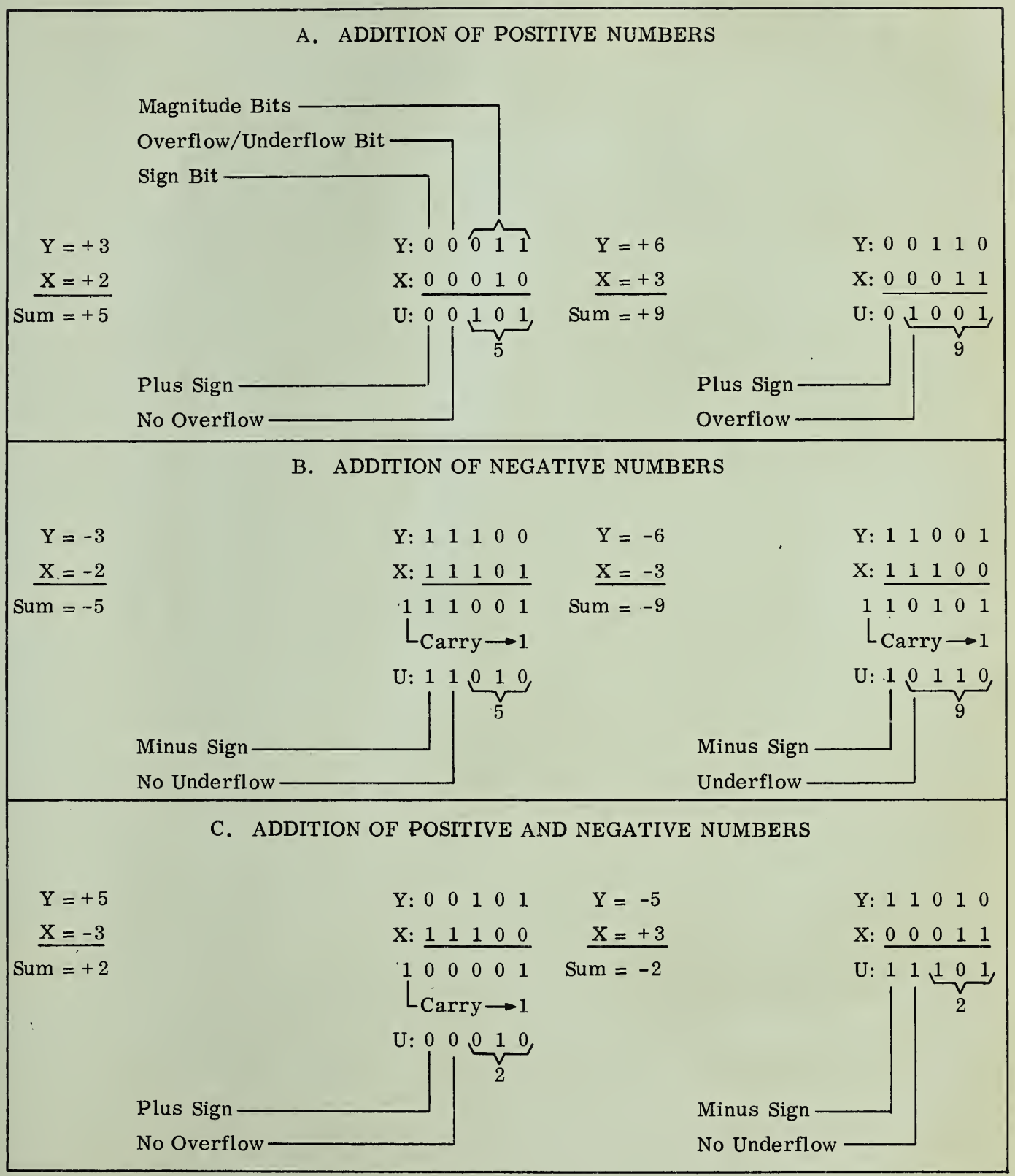


Figure 14-3. Addition Schemes for Non-Angular Data

If the AGC receives a $\Delta\theta$ pulse from a CDU, the contents of the counter in erasable memory associated with this CDU will be incremented or decremented by 1. These pulses arrive one at a time; therefore, the AGC only has to add +1 or -1 to the contents of the proper counter. This addition is performed in the adder of the central processor, i.e., the same place where non-angular data is added.

There is no minus sign associated with angular data, i.e., all angles are considered to be positive. Assume five bit counters in erasable memory including the sign bit and parity bit; therefore, four bits are available to determine the granularity of angular data: three magnitude bits and the sign bit. Using four bits, the granularity of a $\Delta\theta$ pulse would be 22.5^{o}, i.e., $360^{o}/16$.

Table 14-1 shows the 16 possible counter configurations using a five bit counter. Each configuration corresponds to an angular displacement range. For instance, if a CDU were nulled and then driven $+83^{o}$ from the null position, the counter associated with that CDU would have a configuration of 00111. This would mean that the AGC had received three $+\Delta\theta$ pulses from the CDU encoder.

The following two examples functionally illustrate the addition of angular data.

Addition of a $+\Delta\theta$ Pulse (figure 14-4)

1. Assumptions:

   A. X ISS CDU counter has a configuration of 01110.

   B. A $+\Delta\theta$ pulse is generated by the X ISS CDU and sent to the AGC.

2. Operation:

   A. The Y register is cleared, i.e., it is set to 00000.

   B. The content of the X ISS CDU counter is transferred from erasable memory to the X register of the adder. The content of the X register after this transfer is, therefore, 00111.

   C. A forced end-around-carry is generated.

   D. The contents of the X register, Y register and the +1 produced by the forced end-around-carry are all added together.

   E. The content of the U register is 01000. It is now time to send the updated information back to the X ISS CDU counter in erasable memory.

   F. The information in the SB of the U register is inhibited from entering the sign bit of memory. Instead, the OUB of the U register is sent to the sign bit of the memory location.

   G. The OUB and three magnitude bits of the U register are transferred to the sign bit and three magnitude bits of the X ISS CDU counter. The parity block generates the proper parity and sends it to the parity bit of the counter.

Table 14-1. Angular Data Representation

Angle In Degrees	Word In Memory					Word in Central Processor				
	SB	MAG	MAG	MAG	P	SB	OUB	MAG	MAG	MAG
0	0	0	0	0	1	0	0	0	0	0
22.5	0	0	0	1	0	0	0	0	0	1
45	0	0	1	0	0	0	0	0	1	0
67.5	0	0	1	1	1	0	0	0	1	1
90	0	1	0	0	0	0	0	1	0	0
112.5	0	1	0	1	1	0	0	1	0	1
135	0	1	1	0	1	0	0	1	1	0
157.5	0	1	1	1	0	0	0	1	1	1
180	1	0	0	0	0	1	1	0	0	0
202.5	1	0	0	1	1	1	1	0	0	1
225	1	0	1	0	1	1	1	0	1	0
247.5	1	0	1	1	0	1	1	0	1	1
270	1	1	0	0	1	1	1	1	0	0
292.5	1	1	0	1	0	1	1	1	0	1
315	1	1	1	0	0	1	1	1	1	0
337.5	1	1	1	1	1	1	1	1	1	1
0 or 360	0	0	0	0	1	0	0	0	0	0

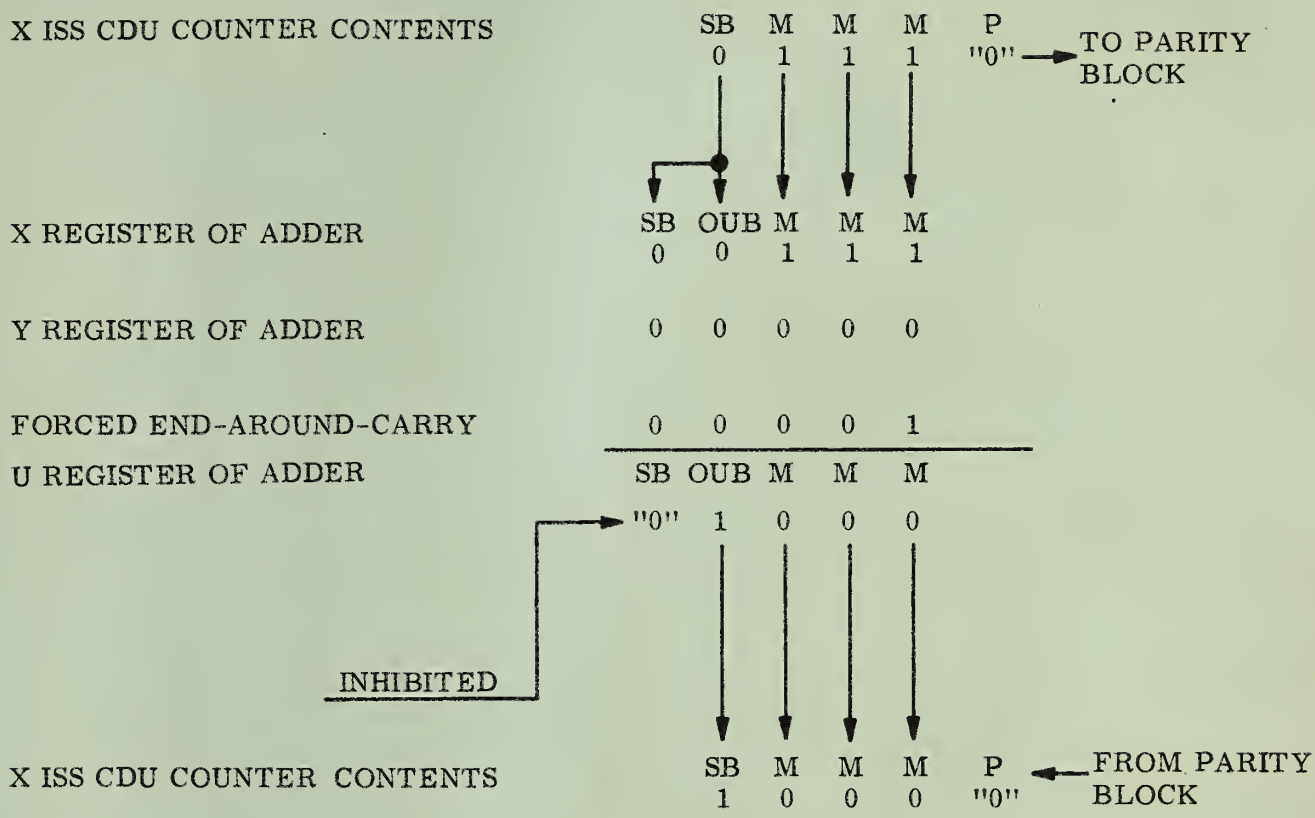

X ISS CDU COUNTER CONTENTS
SB M M M P
0 1 1 1 "0"
TO PARITY BLOCK
X REGISTER OF ADDER
SB OUB M M M
0 0 1 1 1
Y REGISTER OF ADDER
0 0 0 0 0
FORCED END-AROUND-CARRY
0 0 0 0 1
U REGISTER OF ADDER
SB OUB M M M
"0" 1 0 0 0
INHIBITED
X ISS CDU COUNTER CONTENTS
SB M M M P
1 0 0 0 "0"
FROM PARITY BLOCK

Figure 14-4. $+\Delta\theta$ Pulse Addition

Addition of a $-\Delta\theta$ Pulse (figure 14-5)

1. Assumptions:

   A. X ISS CDU counter has a configuration of 00010.

   B. A $-\Delta\theta$ Pulse is generated by the X ISS CDU and sent to the AGC.

2. Operation:

   A. The Y register is set to 11110.

   B. The content of the X ISS CDU counter is transferred from erasable memory to the X register of the adder. The content of the X register after the transfer is, therefore, 00001.

   C. A forced end-around-carry is generated.

   D. The contents of the X register, Y register and the +1 produced by the forced end-around-carry are all added together. Note that the end-around-carry generated by this addition is inhibited because one end-around-carry has already been produced.

   E. The content of the U register is 00000. It is now time to send the updated information back to the X ISS CDU counter in erasable memory.

   F. The information in the SB of the U register is inhibited from entering memory.

   G. The OUB and three magnitude bits of the U register are transferred to the SB and three magnitude bits of the X ISS CDU counter. The parity block generates the proper parity and sends it to the parity bit of the counter.

14.3 LOGIC IMPLEMENTATION

All logic modules in the AGC are built up from many micrologic elements. Micrologic elements are miniaturized semiconductor packages. The necessary resistors and transistors are diffused into a single silicon wafer. An entire three-input NOR gate is contained in a transistor can. Figure 14-6a shows the circuit contained in one micrologic element along with the accepted symbol and associated truth table. A truth table defines the output logic level (1 or 0) for all possible input combinations. The AGC uses positive logic throughout. A logic 1 is +3 VDC, a logic 0 equals 0 VDC. When input A, B or C equals a logic one in the NOR circuit, the associated transistor is biased to an on condition. This results in a path for current flow to ground. The output thus falls to nearly 0 VDC or a logic 0 as indicated by the truth table. If all three inputs equal a logic 0, output D becomes a logic 1.

Although the logic circuits of the AGC are comprised entirely of NOR gates, it is convenient to use the standard AND and OR logic gates to simplify the presentation of later material. Figure 14-6 (b, c and d) show the OR, AND and FLIP-FLOP circuits.

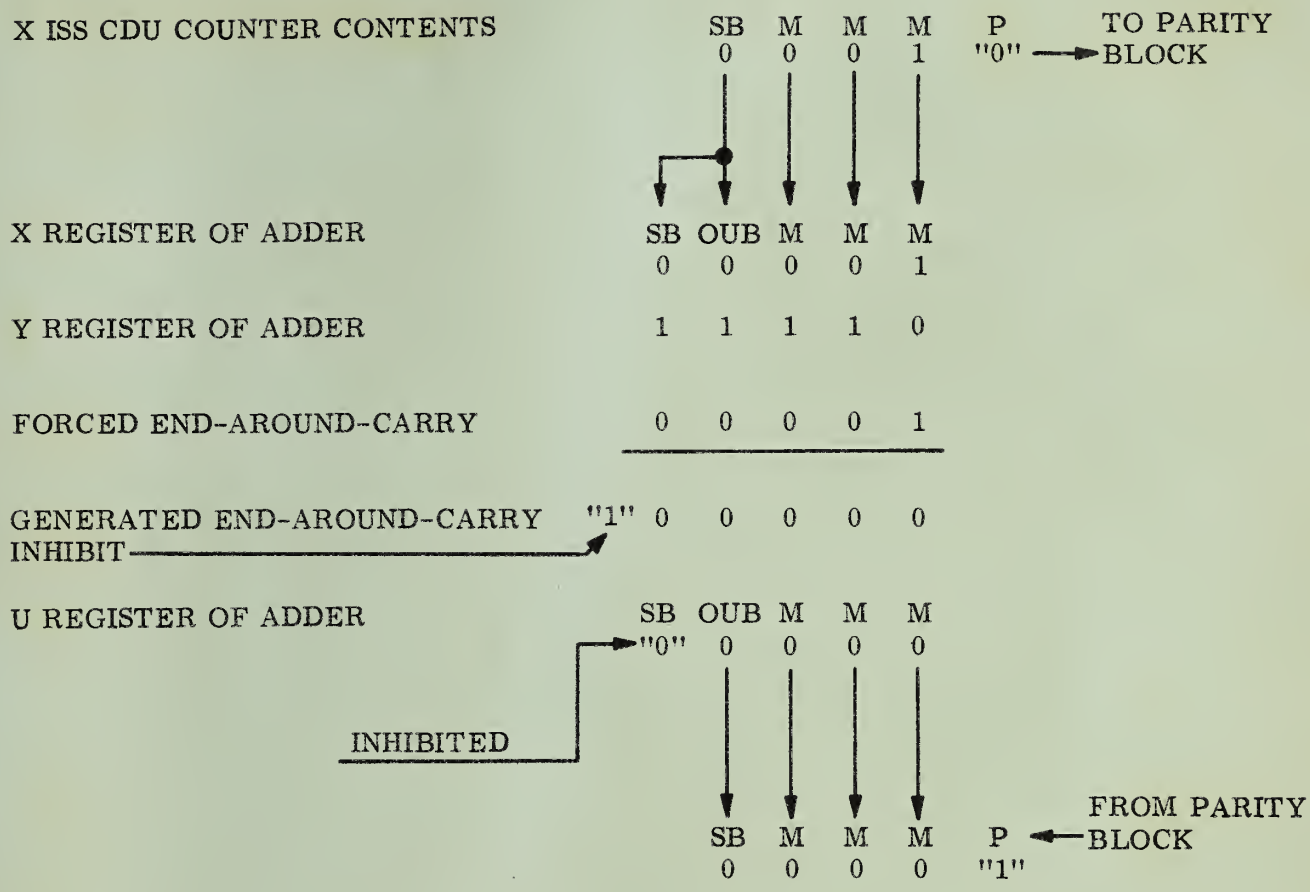
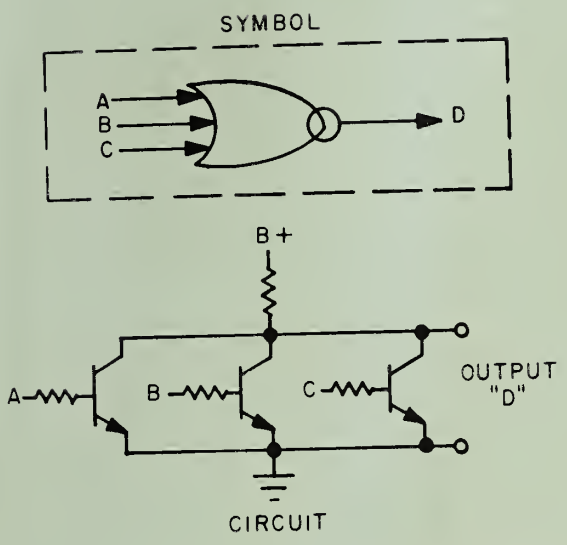

X ISS CDU COUNTER CONTENTS
SB M M M P TO PARITY
0 0 0 1 "0" BLOCK
X REGISTER OF ADDER
SB OUB M M M
0 0 0 0 1
Y REGISTER OF ADDER
1 1 1 1 0
FORCED END-AROUND-CARRY
0 0 0 0 1
GENERATED END-AROUND-CARRY "1" 0 0 0 0 0
INHIBIT
U REGISTER OF ADDER
SB OUB M M M
"0" 0 0 0 0
INHIBITED
FROM PARITY
SB M M M P BLOCK
0 0 0 0 "1"

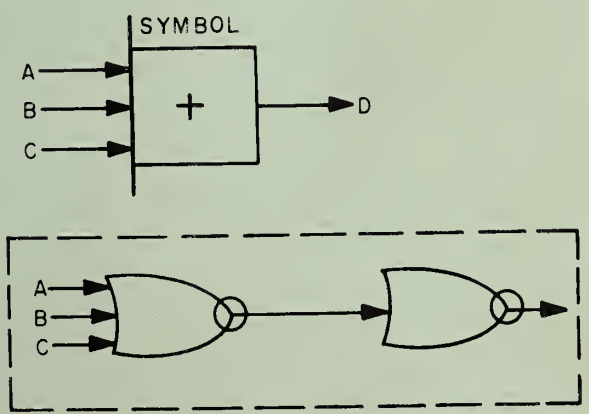
Figure 14-5. $-\Delta\theta$ Pulse Addition



A	B	C	D
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

TRUTH TABLE

(a) NOR CIRCUIT

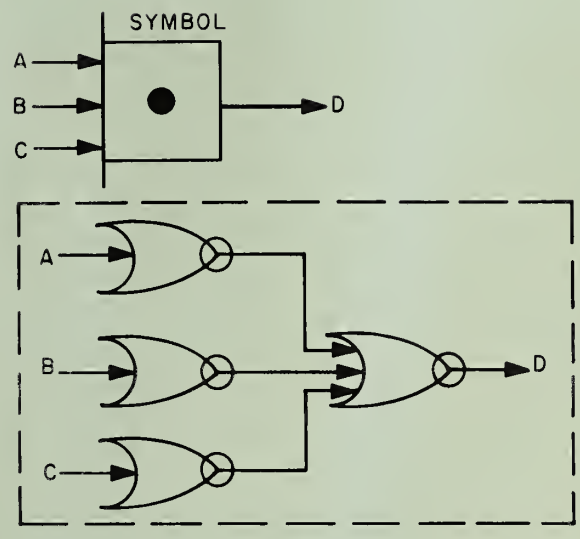


A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

TRUTH TABLE

(b) OR CIRCUIT

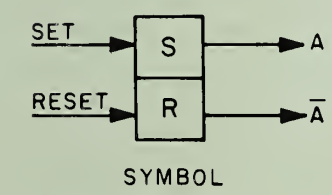
Figure 14-6. Logic Symbology (Sheet 1 of 2)



A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

TRUTH TABLE

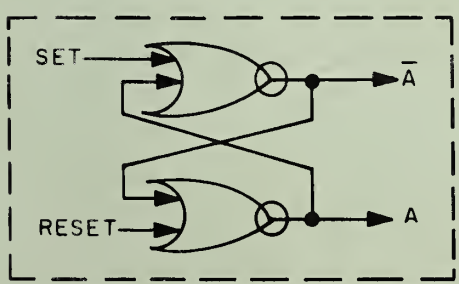
(c) AND CIRCUIT



SYMBOL

	A	$\overline{A}$
SET	1	0
RESET	0	1

TRUTH TABLE



(d) FLIP FLOP

Figure 14-6. Logic Symbology (Sheet 2 of 2)

The NOR gates within the dotted lines show the exact mechanization of the circuits in the simplified symbols. The reader should compare the truth tables included in the diagrams with the circuits. Note that a one input NOR gate is just an inverter. Note also that it is possible to have a logic 0 at both outputs of a flip-flop if both inputs are at a logic 1. Functional AND and OR gates are also used in later drawings in this section and the DSKY section.

14.4 HARDWARE REGISTERS

A hardware register is a device which accepts and stores parallel information. Most of the AGC's hardware registers are 16 bit registers, i.e., they are comprised of 16 storage elements.

14.4.1 STORAGE ELEMENT. A storage element consists of a write gate, storage flip-flop and a read gate (figure 14-7). A storage element can handle only one bit of information; consequently, sixteen of these elements are necessary to make a 16 bit hardware register. Information is written into the storage flip-flop via the write gate. Information is read from the storage flip-flop via the read gate. The information stored in the flip-flop is determined by the SET output; therefore, the line connecting the flip-flop to the read gate carries the complement of the information stored in the flip-flop. Signals $\overline{WG}$, CG and $\overline{RG}$ are named "write gate", clear gate" and "read gate" respectively. When the write gate is enabled, i.e., when it is desired to write information into the storage flip-flop, signal $\overline{WG}$ drops to a logic 0 for 3/4 μ second. When $\overline{WG}$ drops to a logic 0, CP automatically goes to a logic 1 as shown in figure 14-7. $\overline{WG}$ and CG always occur in pairs as shown in figure 14-7. When the read gate is enabled, i.e., when it is desired to read information from the storage flip-flop, signal $\overline{RG}$ drops to a logic 0 for 3/4 μ second.

The information that is to be written into the storage flip-flop is carried by signal $\overline{DATA}$. If a logic 1 is to be stored, $\overline{DATA}$ = 0; if a logic 0 is to be stored, $\overline{DATA}$ = 1.

Assume that a logic 0 is stored in the flip-flop and that it is desired to write a logic 1 into the flip-flop. If a logic 1 is to be written into the flip-flop, $\overline{DATA}$ = 0. When the write gate is enabled, $\overline{WG}$ and CG are generated as shown in figure 14-7. Since $\overline{DATA}$ = 0, the input to the flip-flop SET side will be a logic 1 while $\overline{WG}$ = 0; therefore, the flip-flop will be set and the RESET output will go to a logic 0. While CG = logic 1, the SET side output will also go to a logic 0 for 1/4 μ second; however, this makes no difference because the SET output will go to a logic 1 as soon as signal CP goes back to a logic 0. A logic 1 is now stored in the flip-flop.

Assume now that it is desired to read out the information stored in the flip-flop. The read gate will be enabled when $\overline{RG}$ = 0. When $\overline{RG}$ = 0, the output of the read gate will go to a logic 1. Therefore, a logic 1 has been read from the storage element. Note that readout is non-destructive, i.e., if $\overline{RG}$ dropped to a logic 0 again, a logic 1 would still be read out from the storage element.

The reader may feel that signal CP is not necessary for the proper operation of a storage element. However, CP is necessary when it is desired to write a logic 1 into a storage flip-flop which is presently storing a logic 0. The reader should verify this fact.

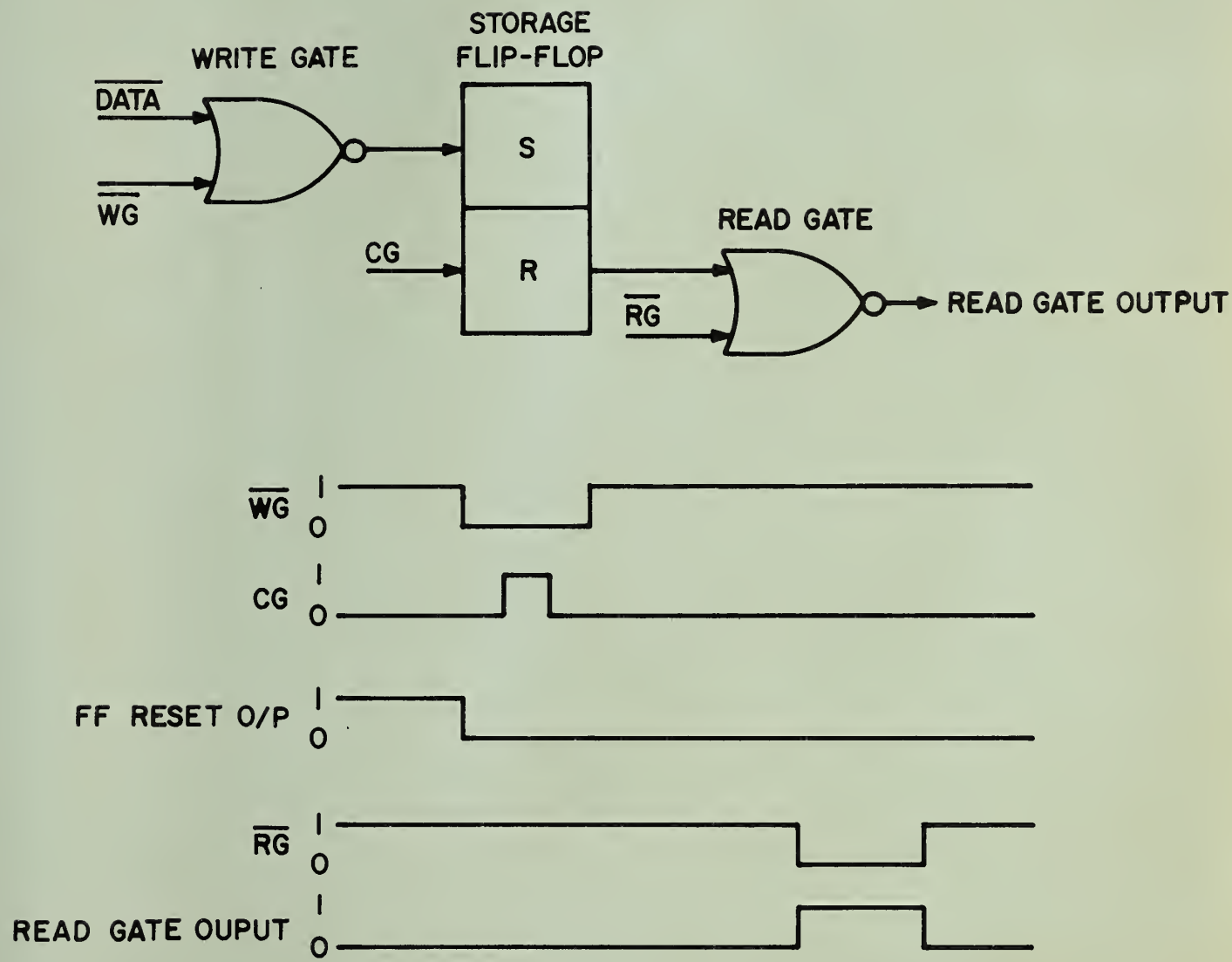


Figure 14-7. Basic Storage Element and Associated Waveforms

14.4.2 HARDWARE REGISTER INTERFACE. A great deal of information transfer takes place between the hardware registers. However, information is never transferred directly between registers. Assume it is desired to read the information stored in Register A into Register B. It is not possible to transfer this information directly. The contents of Register A must first be routed through 16 write amplifiers before it can be entered into Register B. The write amplifiers are simply large NOR gates, i.e., NOR gates with many inputs.

Assume there are only three hardware registers in the AGC, Registers A, B and Z. Bit position 2 of these registers would be connected as shown in figure 14-8. Note that the outputs of the read gates are all connected to a common write amplifier, i.e., Write Amplifier 2. Note also that the output of Write Amplifier 2 is connected to all three write gates. Signal $\overline{\text{WL02}}$ is comparable to $\overline{\text{DATA}}$ in figure 14-7. Signals $\overline{\text{WAG}}$, CBG and $\overline{\text{RZG}}$ are named "write A gate", "clear B gate" and "read Z gate" respectively.

The reader should try to get a complete picture of this interface in his mind before figure 14-8 is discussed in detail. Remember - - only bit position 2 of the registers is shown on figure 14-8. There are 15 other similar circuits for bit positions 1 and 3 through 16. The complete picture would show 16 write gates, 16 storage flip-flops and 16 read gates for each register. There would be a total of 16 write amplifiers, i.e., Write Amplifiers 1 through 16. Imagine 16 drawings like figure 14-8 stacked on each other so that the stack comes toward the reader. Figure 14-8 would be the second sheet in this stack. Signal $\overline{\text{WL07}}$ would be connected to and only to the write gates on the seventh sheet. Signal $\overline{\text{WL11}}$ would be connected to and only to the write gates on the eleventh sheet. The outputs of all the read gates on the ninth sheet would be connected to Write Amplifier 9. Signal $\overline{\text{WAG}}$ would be connected to the top write gate on each sheet and to no others. Signal $\overline{\text{RZG}}$ would be connected to the bottom read gate on each sheet and to no others. The other signals would be connected in a similar fashion.

Figure 14-9 shows the waveforms associated with information transfer between registers. In this figure, it is assumed that bit position 2 of Register B is storing a logic 1 and that this information is to be transferred to bit position 2 of Register A which is storing a logic 0. Remember, if bit position 2 of Register B has a logic 1 stored in it, then signal ④ is a logic 0. When it is time to transfer the information, $\overline{\text{RBG}}$ and $\overline{\text{WAG}}$ simultaneously drop to a logic 0. This enables the B read gate and the A write gate. It is left to the reader to verify the waveforms shown on figure 14-9.

Figure 14-10 is another waveform chart associated with figure 14-8. In this case, however, it is assumed that bit position 2 of Register B is storing a logic 0 and that this information is to be transferred to bit position 2 of Register A which is storing a logic 1. Again, it is left to the reader to verify the waveforms. The reader should note, in this case, the importance of the clear signal CAG.

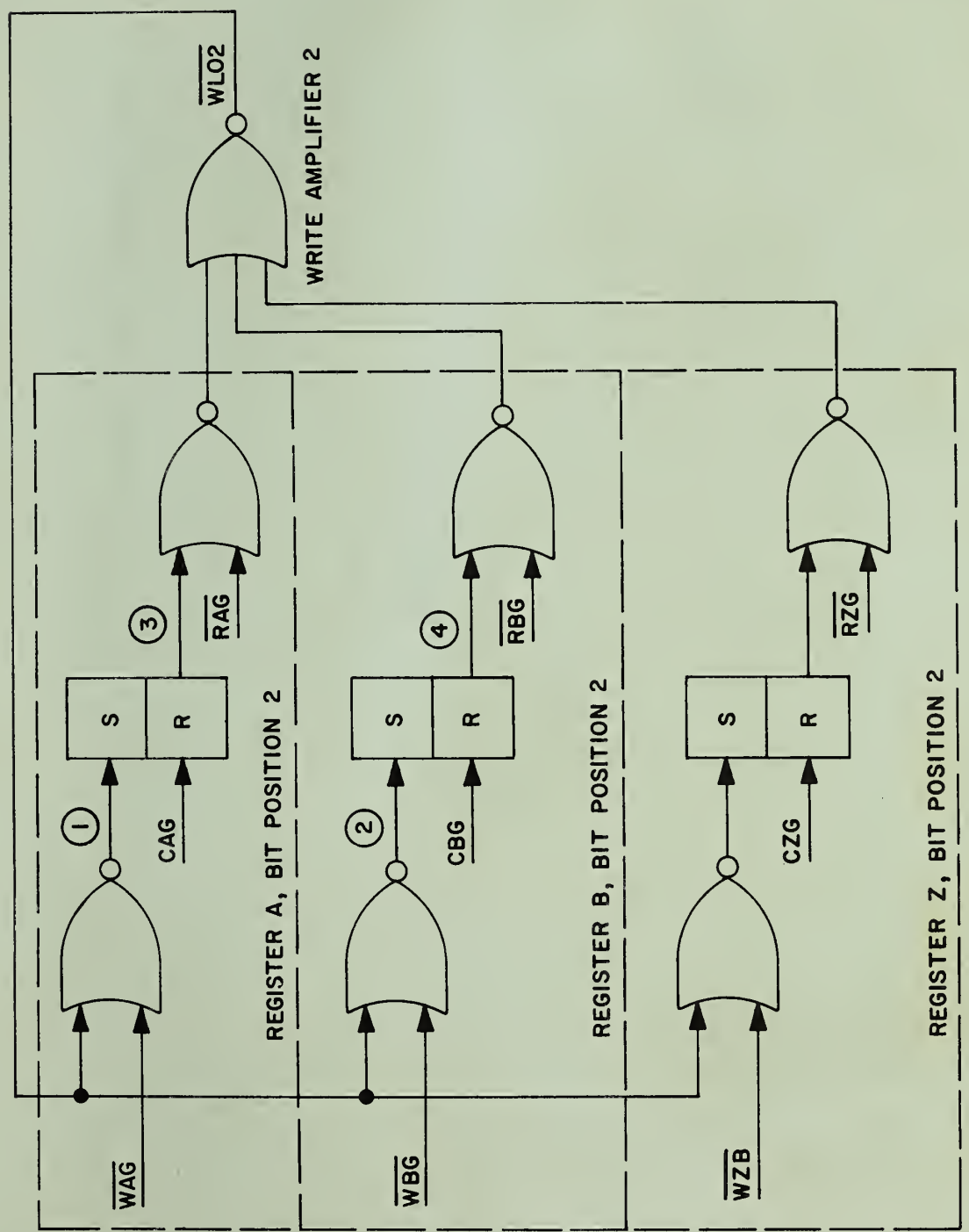


Figure 14-8. Hardware Register Interface

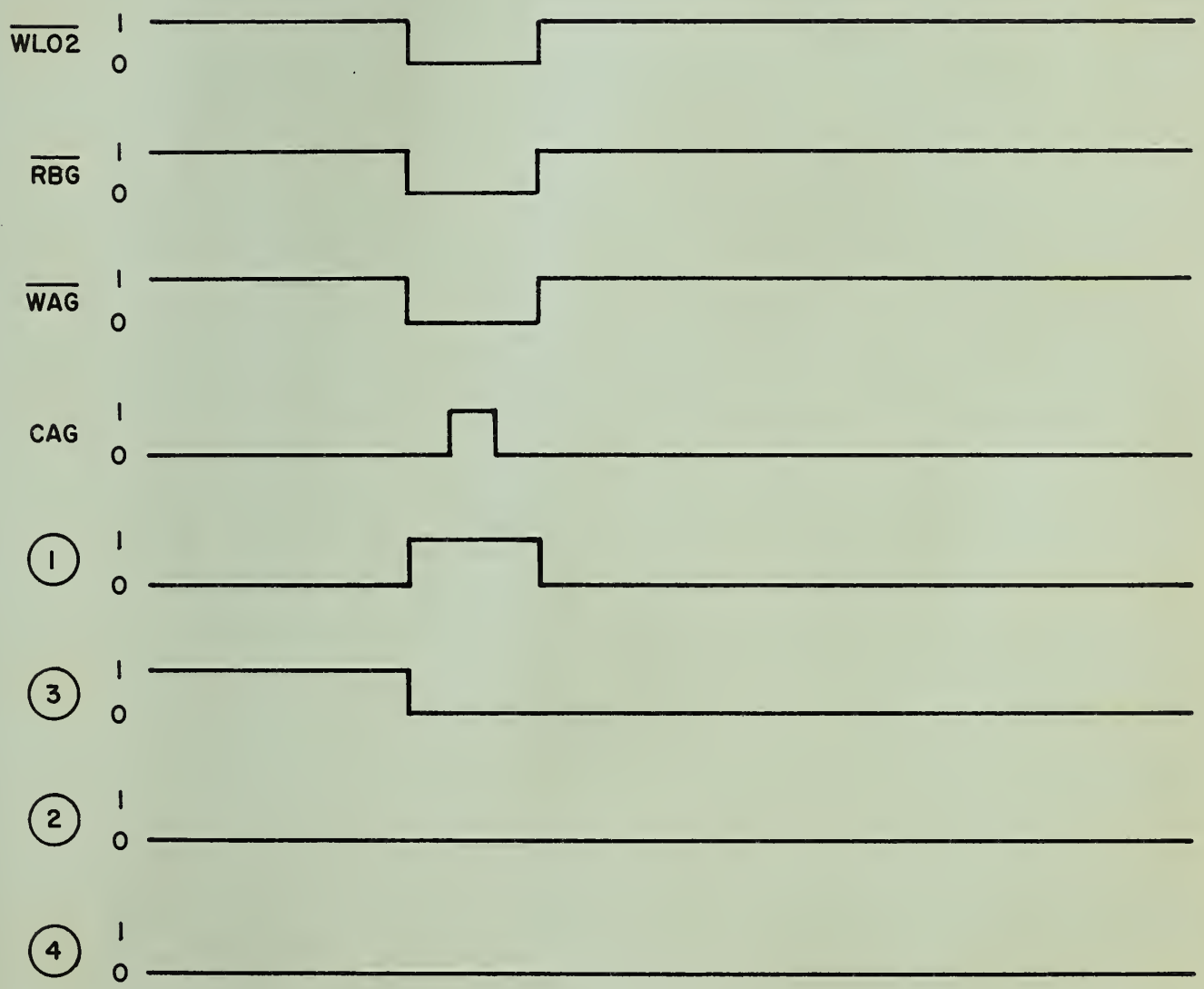


Figure 14-9. Register Data Transfer #1

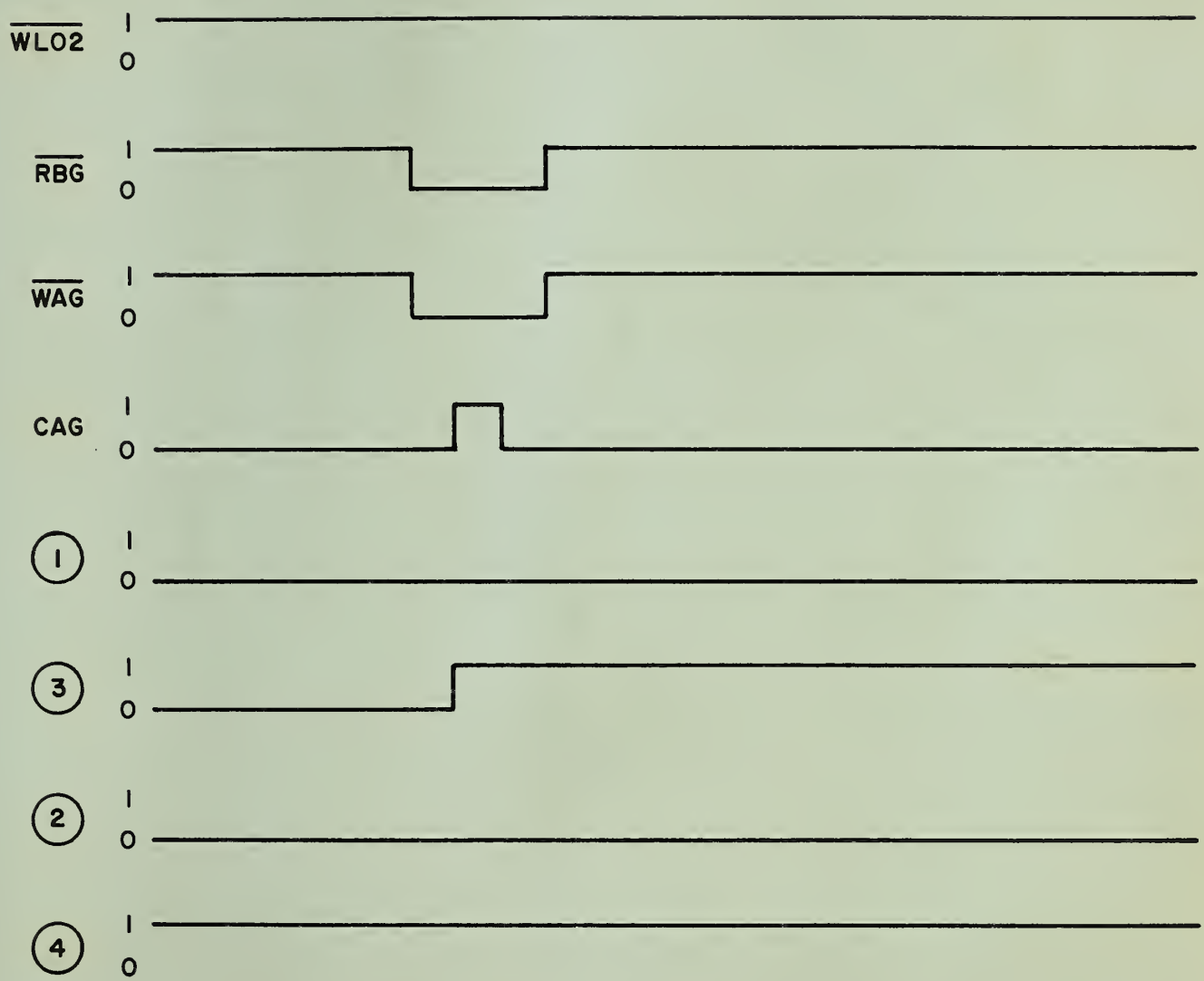


Figure 14-10. Register Data Transfer #2

14.5 TIMER

The timer generates all of the necessary synchronization pulses to insure a logical flow of data from one area to another inside the AGC. It also generates pulse trains which establish output rates to other spacecraft systems for control or synchronization purposes. In addition, it serves as a real time accumulator in conjunction with the IN 1 register. A 2.048 mc basic clock oscillator serves as the source of frequency for the timer. The basic clock is divided in frequency many times by frequency divider circuitry and a ring counter. Frequencies down to .78 cps are available for a variety of timing purposes. A portion of the timer called the "time pulse generator" produces a set of 12 one microsecond sequential timing pulses which define one memory cycle time (MCT). The one μ second time interval defines an "action time" which is the shortest time in which data can be manipulated. An MCT defines the time required to execute a subinstruction. Instructions are comprised of one or more subinstructions. The ADD instruction, for example, is made up of two subinstructions, each of which takes 12 μ sec to execute.

The timer performs the following specific functions:

a. Generates timing pulses and waveforms for use throughout the AGC and other spacecraft systems.

b. Generates 12 timing pulses defining action times within a memory cycle time (MCT).

c. Generates and aids in the accumulation of real time.

The timer is divided into the following areas:

a. Clock Countdown

b. Scaler A and Scaler B

c. Time Pulse Generator

d. Start/Stop Logic

14.5.1 CLOCK COUNTDOWN. The clock countdown (figure 14-11) consists of an oscillator, two binary dividers and a ring counter. The oscillator generates a 2.048 mc square wave. This square wave is sent to the first binary divider which generates 1.024 mc waveforms (figure 14-12). The second binary divider generates 512 kc waveforms (figure 14-13). The ring counter generates 102.4 kc waveforms (figure 14-13). Outputs P03 and P05 drive Scaler A. The other waveforms mentioned above are used to synchronize and sequence data throughout the AGC as well as generate certain AGC outputs.

14.5.2 SCALER A. Scaler A contains 17 identical binary divider stages (figure 14-14). Its input, as mentioned above, is 102.4 kc. Its outputs (table 14-2) range from 51.2 kc to .78125 cps. These waveforms are used throughout the AGC for various purposes. For example, the 3200 cps waveform is sent to the PSA where it is used by the 3200 cps power supply.

14.5.3 SCALER B. Scaler B contains 16 binary divider stages (figure 14-15). The input to Scaler B is from the last stage of Scaler A. Each stage divides the frequency of the previous stage by 2. Scaler B is used to provide a real time indication up to a maximum interval of 23.3 hours. Actually, the 16 stages define a 16 bit word which is applied to the main time counter in erasable memory. This is accomplished by read signal $\overline{\text{RVIG}}$ which is generated under program control. When $\overline{\text{RVIG}}$ is generated, the outputs of the 16 stages are routed to the write amplifiers. The outpus of the write amplifiers are then used to update the main time counter. Note that the IN 1 Register is nothing more than 16 NOR gates.

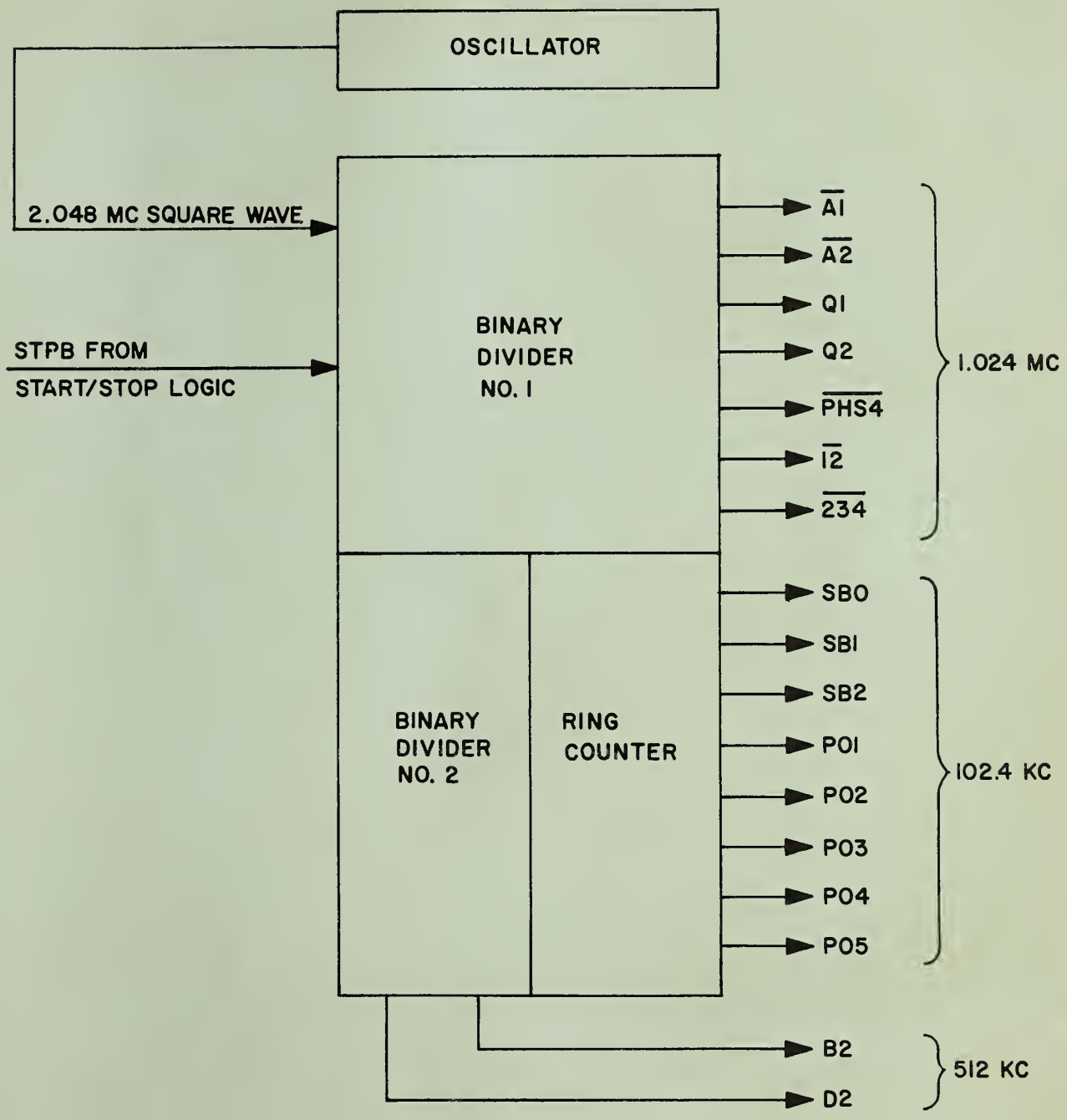


Figure 14-11. Clock Countdown

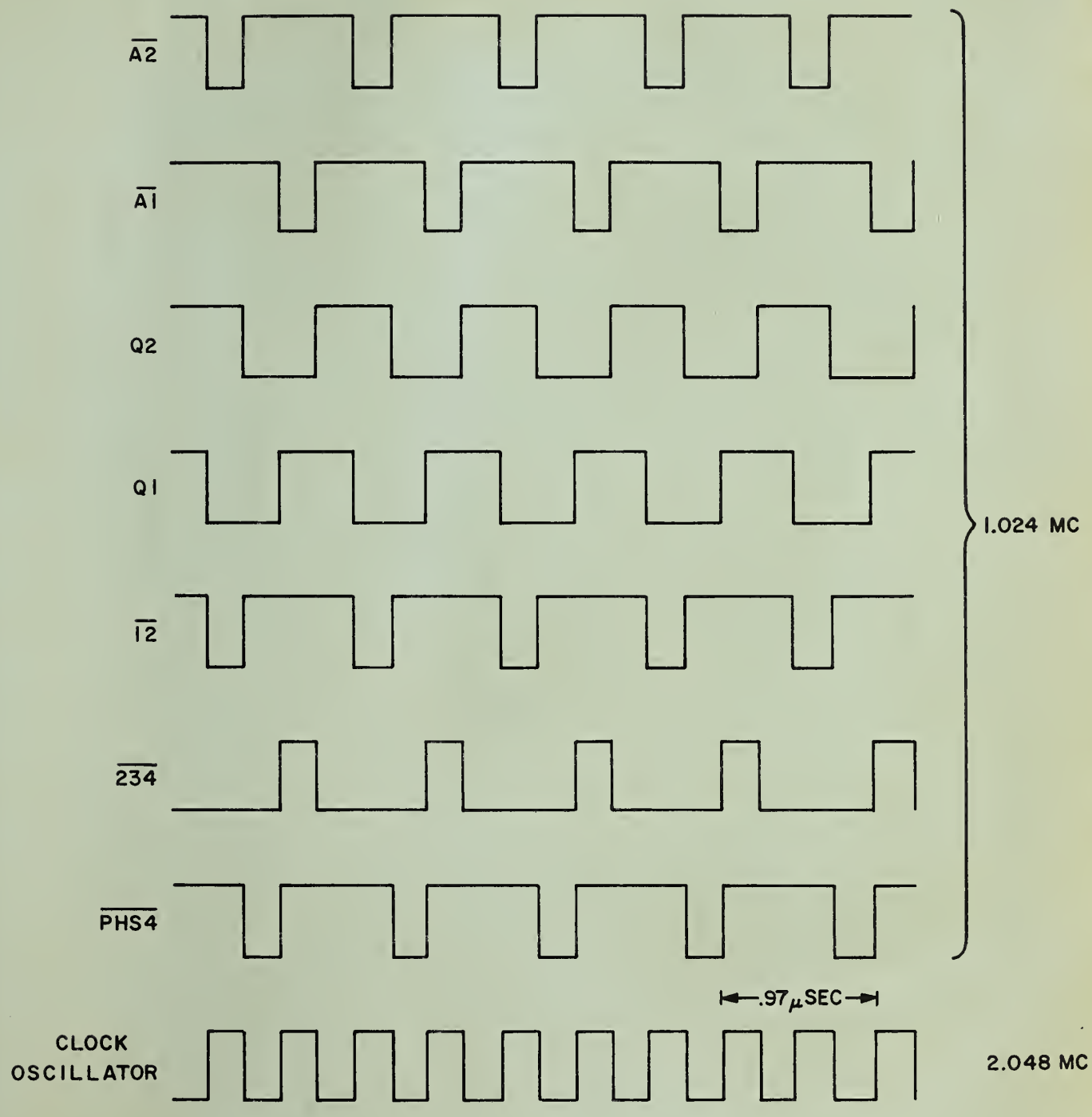


Figure 14-12. Binary Divider #1 Output Waveforms

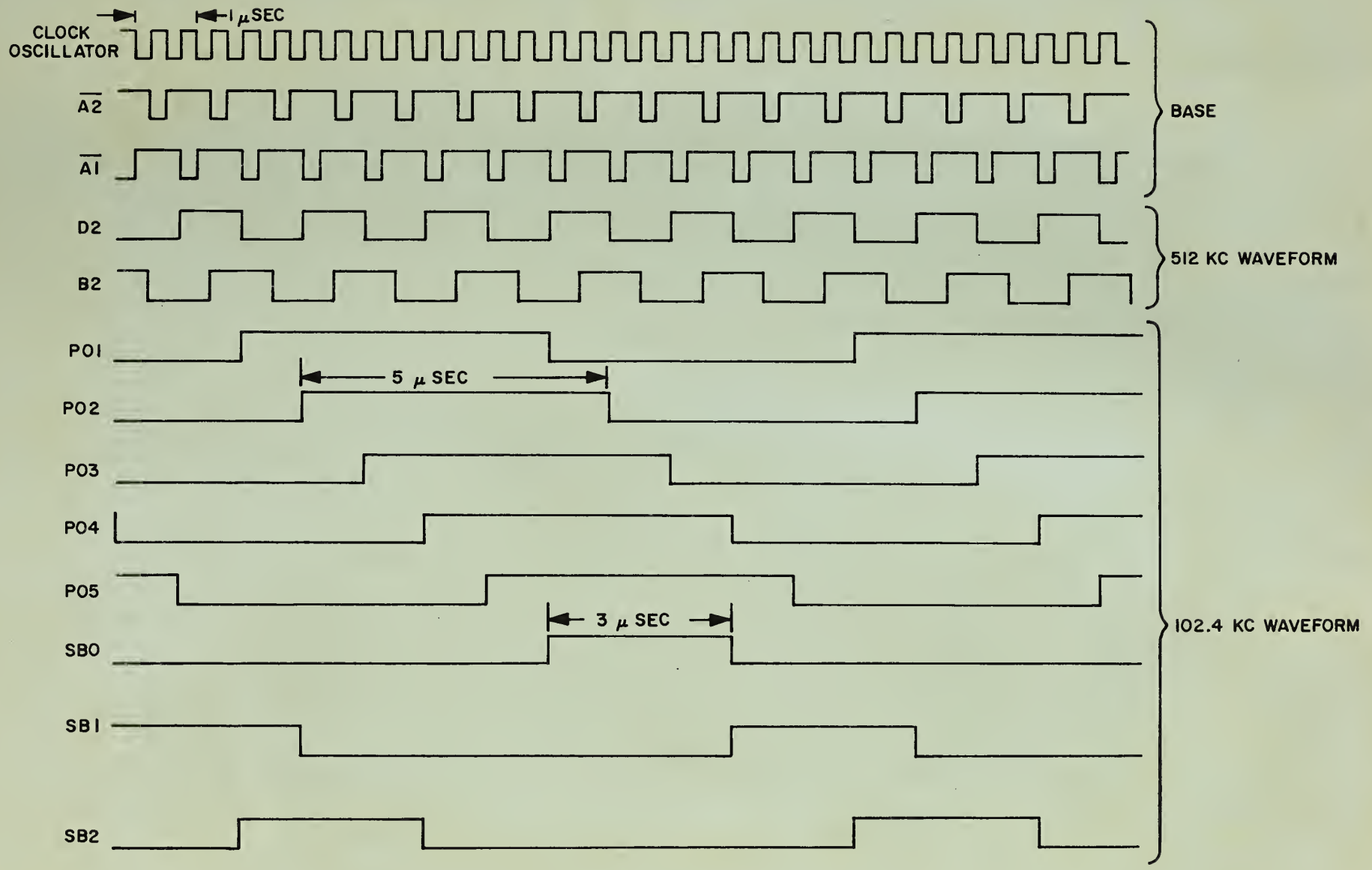


Figure 14-13. Binary Divider #2 and Ring Counter Waveforms

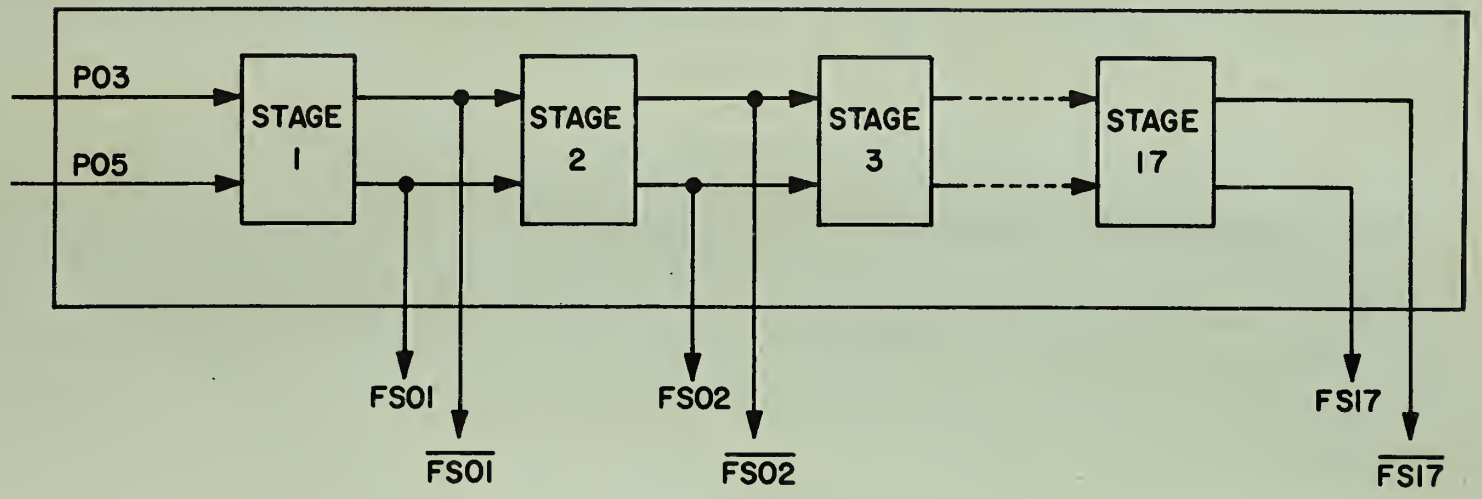


Figure 14-14. Scaler A

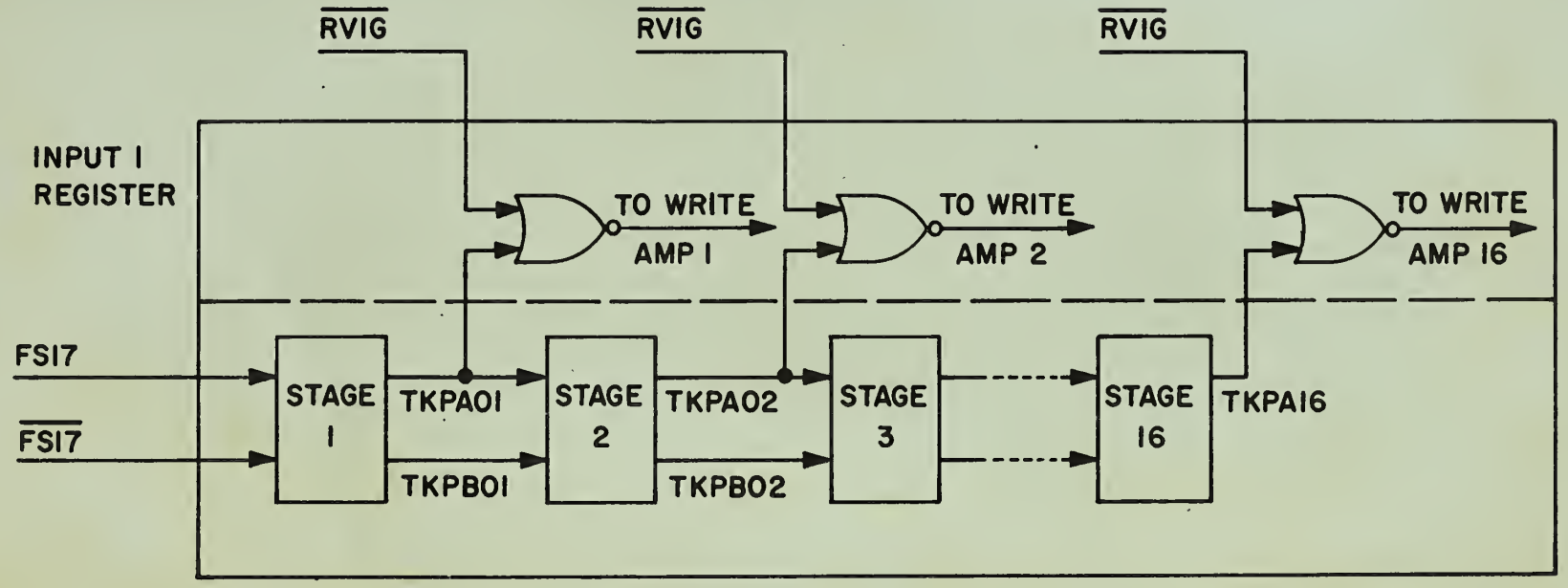


Figure 14-15. Scaler B

Table 14-2. Scaler A Outputs

Stage	Output Frequency	Signal
1	51.2 KC	FS01
2	25.6 KC	FS02
3	12.8 KC	FS03
4	6.4 KC	FS04
5	3.2 KC	FS05
6	1.6 KC	FS06
7	800 CPS	FS07
8	400 CPS	FS08
9	200 CPS	FS09
10	100 CPS	FS10
11	50 CPS	FS11
12	25 CPS	FS12
13	12.5 CPS	FS13
14	6.25 CPS	FS14
15	3.125 CPS	FS15
16	1.5625 CPS	FS16
17	0.78125 CPS	FS17

14.5.4 TIME PULSE GENERATOR. The time pulse generator generates the 12 basic timing pulses $\overline{T01}$ through $\overline{T12}$. These pulses are used throughout the AGC to control interval sequencing of data. Each pulse is .97 μ seconds long and defines an action time. A memory cycle time is defined by $\overline{T01}$ through $\overline{T12}$ and, consequently, is 11.7 μ seconds long. Signals $\overline{A1}$ and $\overline{A2}$ drive the time pulse generator. If signal STPB is generated by the start/stop logic, $\overline{A1}$ is inhibited and the time pulse generator is inhibited from generating the action time pulses. The time pulse generator and its output waveforms are shown in figure 14-16.

14.5.5 START/STOP LOGIC. The start/stop logic (figure 14-17) generates signals STPB and GOJAM. Signal STPB is applied to the clock countdown circuit and inhibits $\overline{A1}$ which, in turn, inhibits word flow within the AGC. An ALARM signal coincident with $\overline{T12}$ causes signal STPB to be generated. STPB causes GOJAM which is essentially a clear signal. Within the AGC, GOJAM inhibits access to memory, clears the output registers and generates a GO condition in the sequence generator. Signal STRT2 indicates a power failure.

14.6 CENTRAL PROCESSOR

The central processor performs the arithmetic and logical data manipulations required of the AGC. The central processor consists of the parity block, adder, write amplifiers and the S, SQ, A, B, Z, Q, LP and G hardware registers. The input, output and BANK registers are also hardware registers. Usually, the BANK register is considered part of fixed memory. The input and output registers are considered part of the input - output block.

14.6.1 G REGISTER. The G Register provides the interface between memory and the hardware registers. All data routed from memory to the hardware registers goes through the G Register. All data routed from the hardware registers to erasable memory goes through the G Register. It is in this register that the parity bit is removed and checked when words are read from memory. It is in this register that the generated parity bit is placed before a word is entered into erasable memory. The G Register also causes words to be moved to the left or right under program control. Figure 14-18 shows the information flow associated with the G Register when a word is read from memory into a hardware register. Note that the information in bit position 0 of the memory word is routed to bit position 15 of the G Register and then directly to the parity block. This information is not sent to a write amplifier. Observe that the data in bit position 16 of Register G is transferred to both Write Amplifer 15 and 16. This is why bits 15 and 16 of a hardware register are identical after information has been sent from memory. The reader should now refer back to figure 14-1 and compare the word formats to the data flow in figure 14-18.

Assume bit position 2 of a memory word is a logic 1. If this word is read from memory, output SA02 (sense amplifier output 2) will transfer a logic 1 to Write Amplifier 2. The output of Write Amplifier 2, $\overline{WL02}$, will send a logic 0 to the bit position 2 write gate of the appropriate register. When this data is written into the storage flip-flop, a logic 1 will be stored. The reader should refer back to figure 14-8.

14.6.2 WRITE AMPLIFIERS. The write amplifiers provide adequate current driving capabilities for all registers. Information from one register is routed through the write amplifiers and then distributed to other registers. It is in the write amplifiers that the sign bit is duplicated. The write amplifiers do not store information: they simply route information. The outputs of the S, SQ and BANK registers are not connected to the write amplifier inputs.

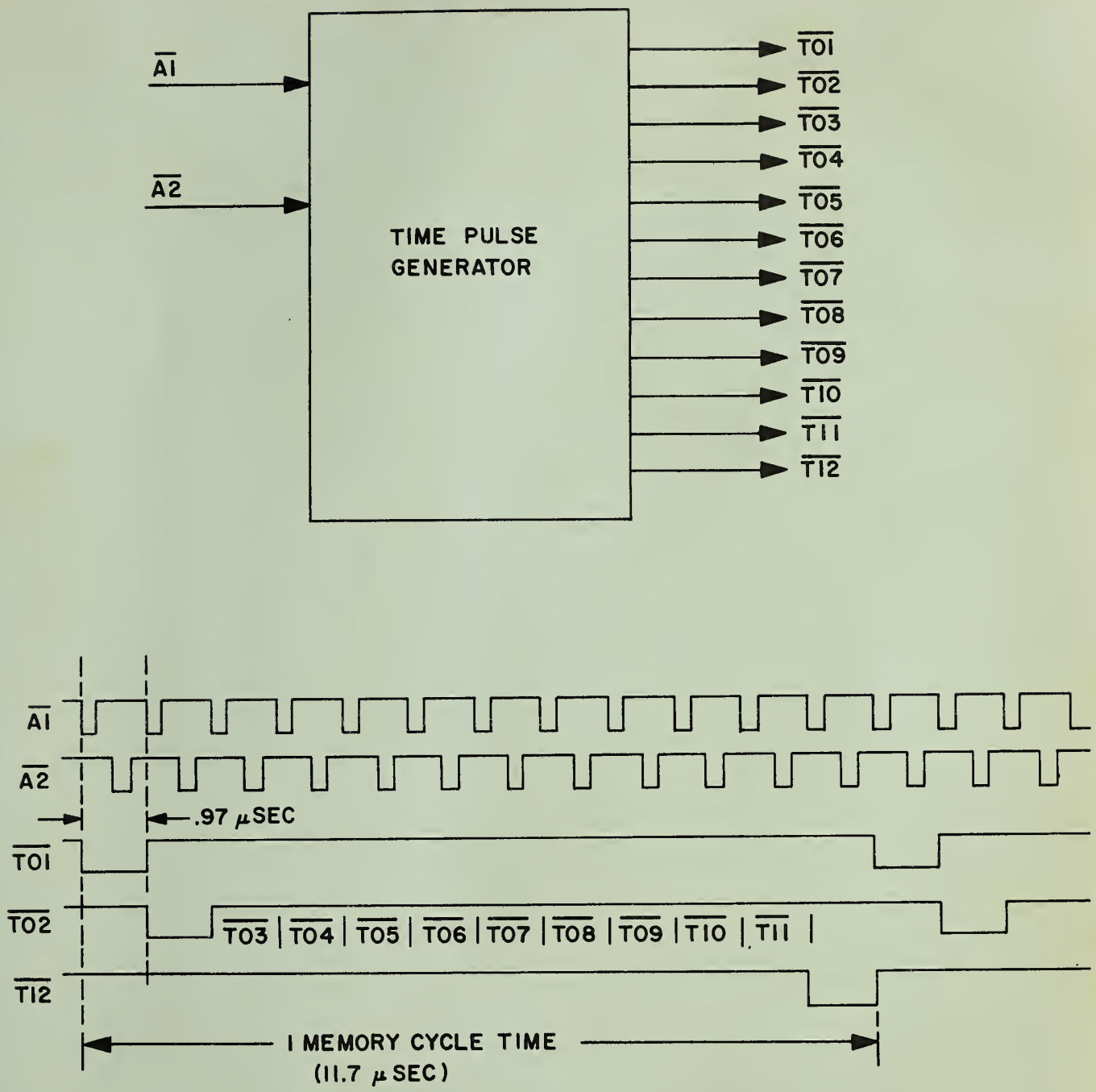


Figure 14-16. Time Pulse Generator and Associated Waveforms

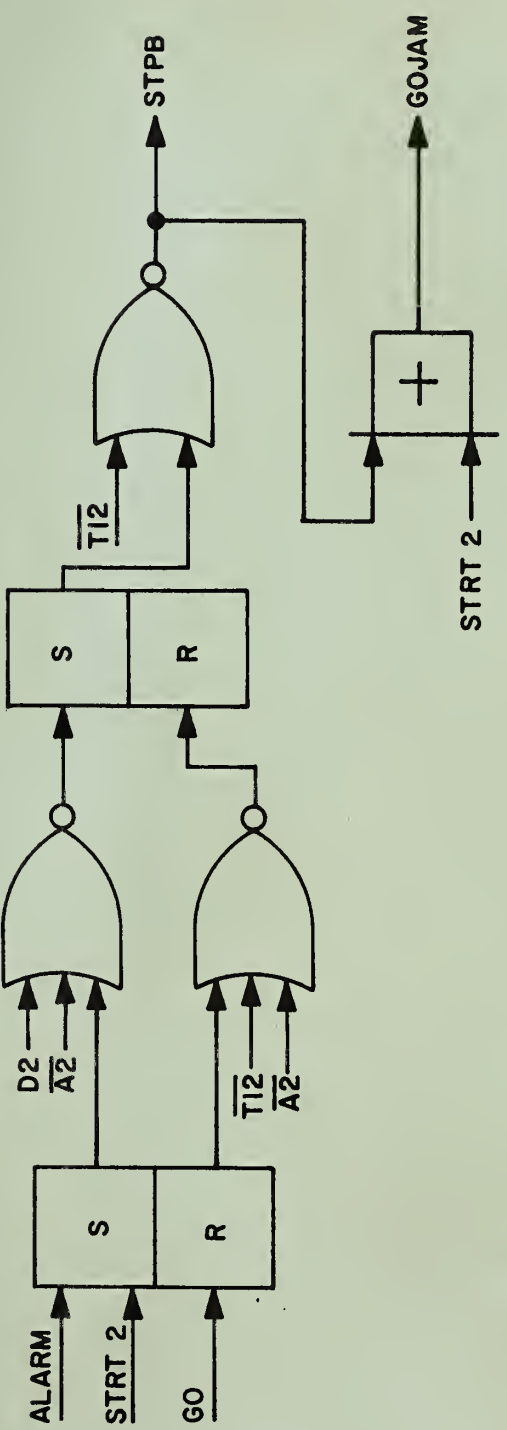


Figure 14-17. Start/Stop Logic

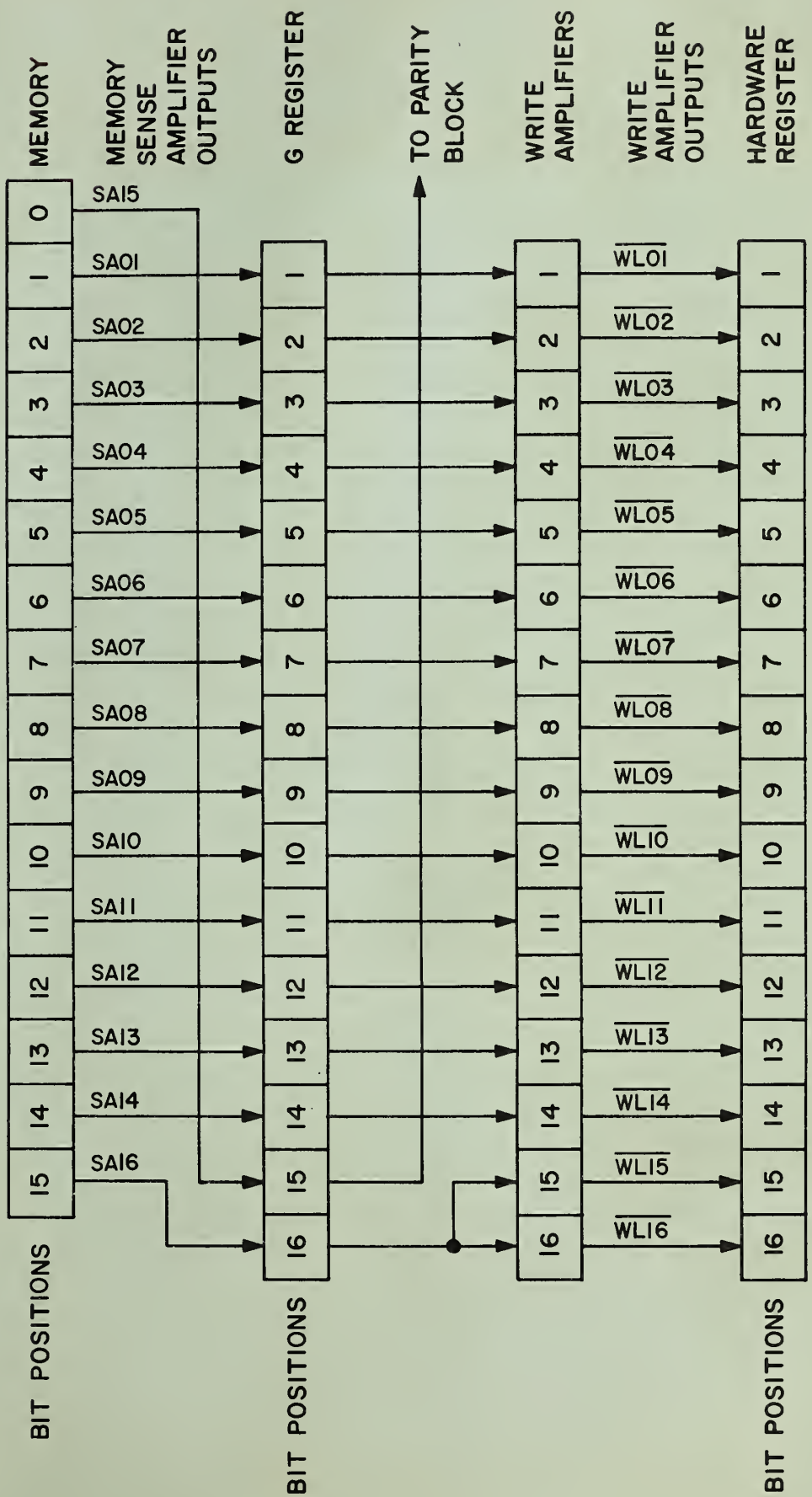


Figure 14-18. G Register Interface

14.6.3 S REGISTER AND BANK REGISTER. The S Register is the Address Register. It is 12 bits long and addresses erasable memory, fixed memory and the addressable hardware registers. The BANK register is used in conjunction with the S Register when fixed memory is addressed. The BANK register is five bits long and is an addressable register. Table 14-3 lists the addresses for memory and the various addressable register S.

The addresses in table 14-3 are determined in the following manner. If bits 11 and 12 of Register S are not both logic 1's, then the address is determined solely by the S Register as shown in figure 14-19. If bits 11 and 12 of Register S are both logic 1's, then the address is determined by the S Register and BANK Register as shown in figure 14-20. Note that bits 11 and 12 of the S Register must both be logic 0's if erasable memory or an addressable register is addressed.

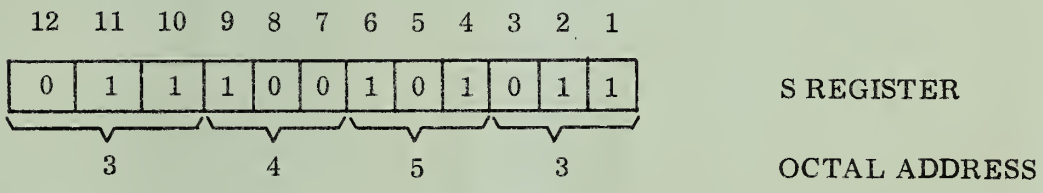


Figure 14-19. Address Determination Scheme #1

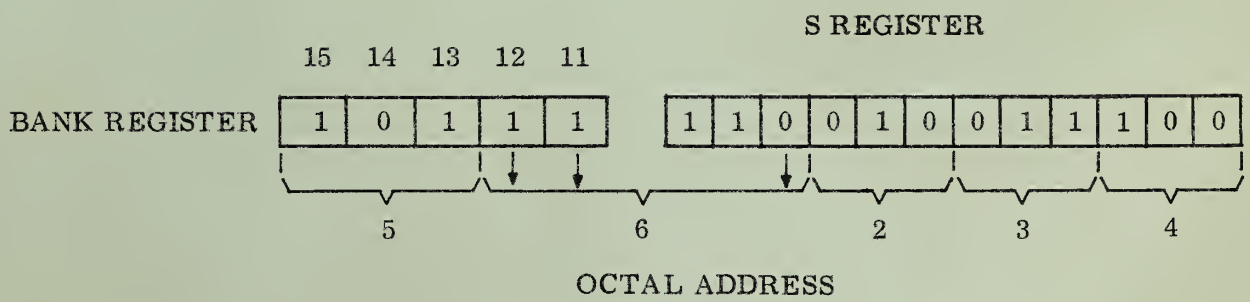


Figure 14-20. Address Determination Scheme #2

Table 14-3. Addressing

	Locations		Octal Address	Contents of BANK Register (1)					Contents of S Register (1)										
				15	14	13	12	11	12	11	10	9	8	7	6	5	4	3	2	1
Addressable Registers	A, Q, Z, LP		0000 - 0003	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0	x	x
	INPUT		0004 - 0007	x	x	x	x	x	0	0	0	0	0	0	0	0	0	1	x	x
	OUTPUT		0010 - 0014	x	x	x	x	x	0	0	0	0	0	0	0	0	1	x	x	x
	BANK		0015	x	x	x	x	x	0	0	0	0	0	0	0	0	1	1	0	1
Erasable	PROGRAM		0016 - 0017	x	x	x	x	x	0	0	0	0	0	0	0	0	1	1	1	x
	SPECIAL		0020 - 0027	x	x	x	x	x	0	0	0	0	0	0	0	1	0	x	x	x
	SPARES		0030 - 0033	x	x	x	x	x	0	0	0	0	0	0	0	1	1	0	x	x
	COUNTER		0034 - 0057	x	x	x	x	x	0	0	0	0	0	0	x	x	x	x	x	x
	GENERAL		0060 - 1777	x	x	x	x	x	0	0	x	x	x	x	x	x	x	x	x	x
Fixed	Fixed-Fixed	BANK 01	2000 - 3777	x	x	x	x	x	0	1	x	x	x	x	x	x	x	x	x	x
		BANK 02	4000 - 5777	x	x	x	x	x	1	0	x	x	x	x	x	x	x	x	x	x
	Fixed-Switchable	BANK 03	6000 - 7777	0	0	0	x	x	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 04	10000 - 11777	0	0	1	0	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 05	12000 - 13777	0	0	1	0	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 06	14000 - 15777	0	0	1	1	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 07	16000 - 17777	0	0	1	1	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 10	20000 - 21777	0	1	0	0	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 11	22000 - 23777	0	1	0	0	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 12	24000 - 25777	0	1	0	1	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 13	26000 - 27777	0	1	0	1	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 14	30000 - 31777	0	1	1	0	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 21	42000 - 43777	1	0	0	0	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 22	44000 - 45777	1	0	0	1	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 23	46000 - 47777	1	0	0	1	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 24	50000 - 51777	1	0	1	0	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 25	52000 - 53777	1	0	1	0	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 26	54000 - 55777	1	0	1	1	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 27	56000 - 57777	1	0	1	1	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 30	60000 - 61777	1	1	0	0	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 31	62000 - 63777	1	1	0	0	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 32	64000 - 65777	1	1	0	1	0	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 33	66000 - 67777	1	1	0	1	1	1	1	x	x	x	x	x	x	x	x	x	x
		BANK 34	70000 - 71777	1	1	1	0	0	1	1	x	x	x	x	x	x	x	x	x	x

(1) x means 0 or 1

14.6.4 SQ REGISTER. The SQ Register is a four bit register which contains the order code of the instruction to be executed. The bit positions are numbered 13 through 16, i.e., the SQ storage flip-flops receive their inputs from Write Amplifiers 13 through 16. The S and SQ Registers are sometimes thought of as a single 16 bit register.

14.6.5 Z REGISTER. The Z Register is a 16 bit addressable register. It is sometimes referred to as the "program counter". The Z Register contains the address of the next instruction to be performed. As each instruction is executed, the Z Register is incremented by +1 because instruction words are usually stored sequentially in memory.

14.6.6 A, LP AND Q REGISTERS. Register A is a 16 bit addressable register. It normally retains information between the execution of individual instructions. Register LP is a 16 bit addressable register. It is used only during the multiply and divide instructions. The Q Register is the "return address register". When the AGC transfers control to another program or subroutine, the content of the Z Register is stored in the Q Register. When the AGC returns to the original program, Register Q contains the address of the appropriate instruction. Register Q is an addressable 16 bit register.

14.6.7 B REGISTER. The B Register is a 16 bit register which is used as a storage or buffer register. When an instruction word is read from memory to the central processor, it is usually stored in Register B after passing through Register G. Bits 1 - 12 are then transferred to the S Register and bits 13 - 16 to the SQ Register. The B Register also provides a means for complementing data because its reset side can be interrogated. The reset side is called the C Register.

14.6.8 ADDER. The adder consists of the X, Y and U Registers. The X and Y Registers are the input registers. The U Register is the output register. In other words, the two numbers to be added are placed in the X and Y Registers. The sum of these numbers is found at the output of the U Register. Provisions are made to generate carries when necessary. Figure 14-3 showed the addition of positive and negative numbers; it also pointed out overflow and underflow conditions and end-around-carry. Figure 14-21 is a simplified block diagram of the adder. One number is gated into Register Y and the other into Register X. A maximum of 3 μ seconds later, their sum will appear as outputs SUM01 through SUM16. The CRY lines represent the carries that are generated during the addition of two bits and passed on to the next addition process. Note that the carry generated on the last computation is the end-around-carry and is routed to bit 1. Circuitry not shown in figure 14-21 has the capability of (1) adding +1 to a number by forcing an end-around-carry, (2) preventing an end-around-carry during certain operations and (3) inhibiting SUM16 and replacing it with SUM15 during angular addition. In general, SUM01 through SUM16 are routed to Write Amplifiers 1 through 16 respectively.

Figure 14-22 is a detailed view of the top block in figure 14-21, i.e., the logic circuitry associated with bit position 1 of the adder. Note that $\overline{\text{WL01}}$ is applied to both write gates. This does not mean that the same logic level will always be applied to the write gates of the X and Y Registers. The Y Register is loaded before the X Register; consequently, the logic level on $\overline{\text{WL01}}$ may change after it is written into Y. Signal CUG (clear U gate) is associated with $\overline{\text{WYG}}$ (write Y gate) but not with $\overline{\text{WXG}}$ (write X gate). In other words, the pulse CUG = logic 1 will only be developed in the middle of pulse $\overline{\text{WYG}}$ = logic 0.

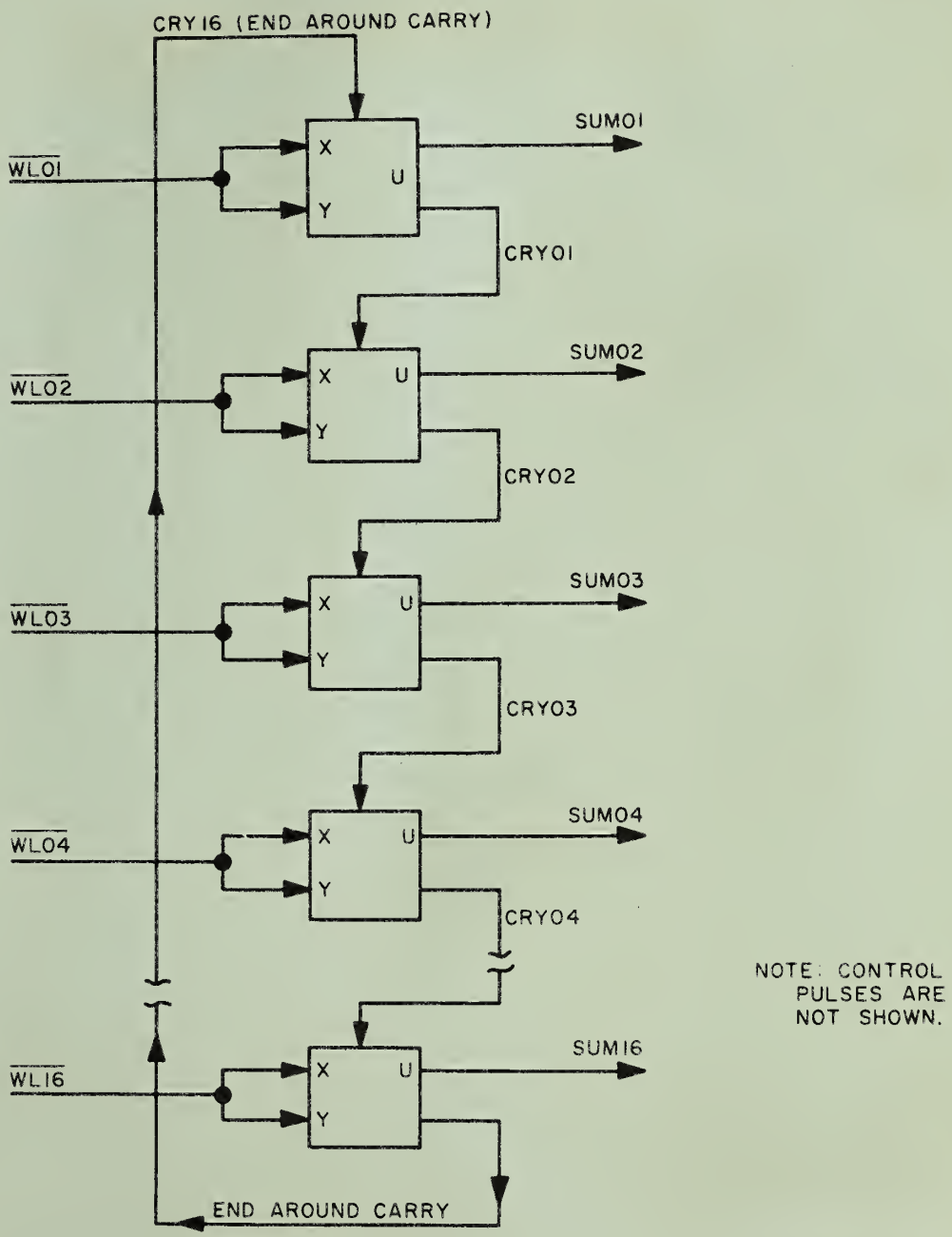


Figure 14-21. Adder Block Diagram

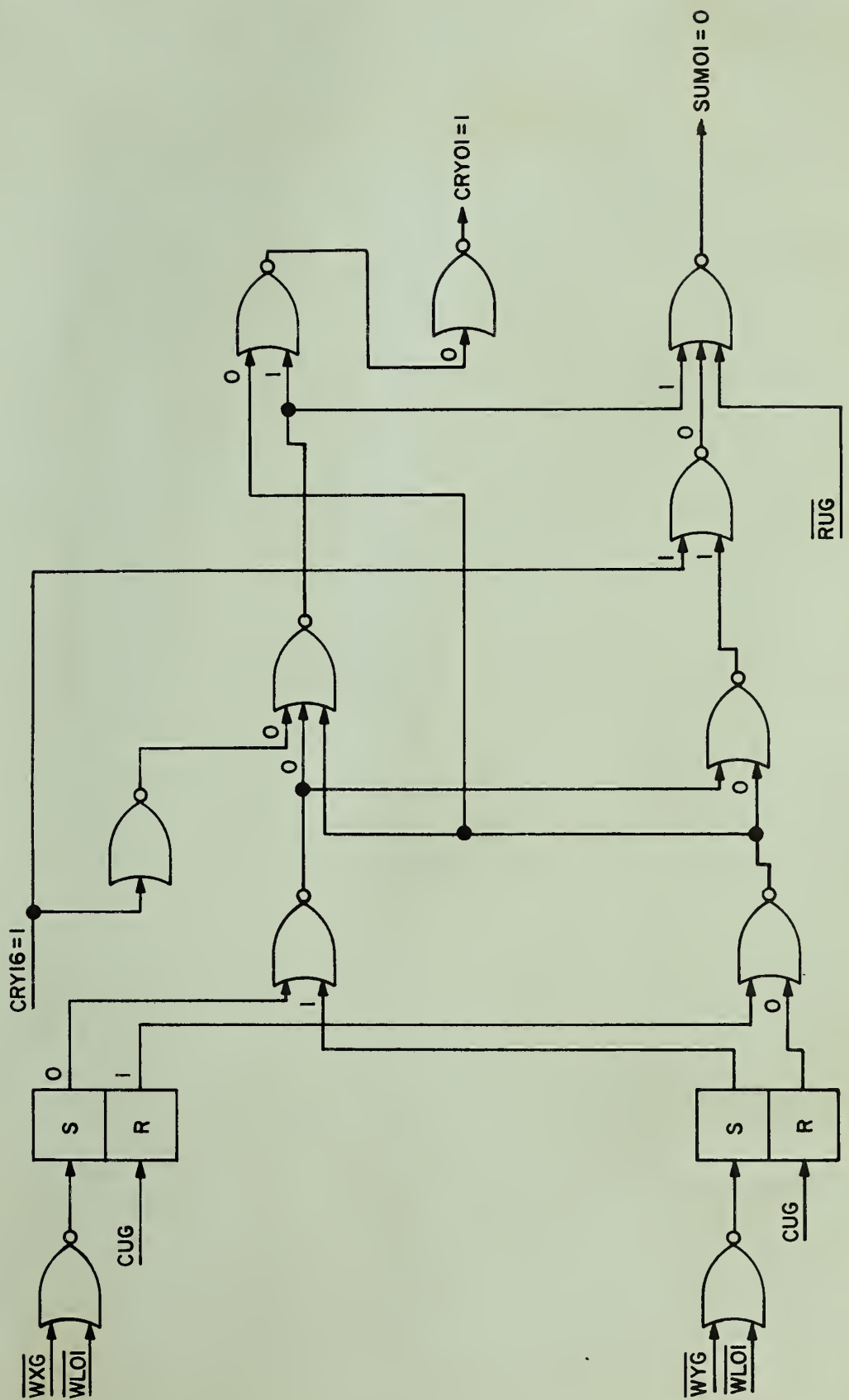


Figure 14-22. Adder (Bit Position 1)

Assume that CRY16 = 1, $\overline{WL01}$ (Y Register) = 0 and $\overline{WL01}$ (X Register) = 1. Remember, $\overline{WL01}$ carries the complement of the data read from memory or another hardware register; therefore, a logic 1 will be inserted into the Y Register and a logic 0 will be inserted into the X Register. The numbers (1 or 0) at the inputs and outputs of the logic gates shown in figure 14-22 are those logic level that would appear after (1) $\overline{WL01}$ = 0 has been written into the Y Register, (2) $\overline{WL01}$ = 1 has been written into the X Register and (3) CRY16 = 1 has been applied to the circuitry. The logic level associated with SUM01 is assumed to be the one present while $\overline{RUG}$ = 0, i.e., while the U read gate is being read.

14.6.9 PARITY BLOCK. The parity block provides a means of checking the computer memory and transfer circuits. It tests the parity of words arriving in the hardware registers from memory and generates a parity bit for words being written into erasable memory. Any time a word is read out of memory its parity must be tested. Every time a word is written into memory its parity must be generated. An alarm signal issued if the parity check fails. This signal is sent to the DSKY's where it lights the PARITY FAIL indicator on the nav panel DSKY and the COMP FAIL indicator on the main panel DSKY. The parity block is active during all basic instructions.

Figure 14-23 is a drawing of the parity block and bit position 15 of the G Register. Excluding control pulses, the parity block receives signals $\overline{WL16}$ and $\overline{WL14}$ through $\overline{WL01}$ from the write amplifiers, WL16 and WL14 through WL01 from inverters connected to the outputs of the write amplifiers and signal $\overline{PARBUS}$. Note that the parity block does not receive WL15 or $\overline{WL15}$.

When a word is read from memory into a hardware register, the parity bit is inserted into bit position 15 of the G register; consequently, when the G Register is being read, i.e., when $\overline{RGG}$ = 0, signal $\overline{PARBUS}$ is the complement of the parity bit. Signal $\overline{GPG}$ = 0 only when writing the parity bit into memory.

Assume that the G Register has been loaded by a word from memory and has the configuration shown in figure 14-24. Signals $\overline{RGG}$, $\overline{WPG}$ and CPG are timelined in figure 14-25 and will be used for the parity check which will take place during T1 - T4. Do not confuse T1 through T4 with $\overline{T01}$ through $\overline{T04}$. The pulses shown in figure 14-25 all take place during one action time. The reader should mark figure 14-23 during the following example to aid in his comprehension of the subject matter.

While $\overline{RGG}$ = 0, $\overline{PARBUS}$ = 1 and the WL and $\overline{WL}$ signals will have the configurations shown in figures 14-26 and 14-27. When CPG = 1, the flip-flops on sheet 1 of figure 14-23 will all be cleared, i.e., outputs A through F will go to a logic 0 and outputs $\overline{A}$ through $\overline{F}$ will go to a logic 1. When $\overline{WPG}$ = 0, the flip-flop outputs will be set in the following configuration: A = 0, B = 1, C = 1, D = 0, E = 1 and F = 0. The flip-flops will remain in this configuration until they are cleared again. If the incoming word, i.e., WL16 and WL14 through WL01, has an even number of logic 1's, outputs A through E will total an even number of logic 1's; if the incoming word has an odd number of logic 1's, outputs A through E will total an odd number of logic 1's. The reader should verify for himself why this is true and note that A through E, in this example, total an odd number of logic 1's.

Signals A, $\overline{A}$ through F, $\overline{F}$ are applied to the gates on sheet 2 of figure 14-23. If ODFBR = 1 and EVNF = 0, then there are an odd number of logic 1's in the word (excluding the parity bit); if ODFBR = 0 and EVNF = 1, then there are an even number of logic 1's in the word (excluding the parity bit). It is impossible for ODFBR and EVNF to both be logic 1's because either F or $\overline{F}$ must be a logic 1. If ODFBR and EVNF are both logic 0's, then there has been an error in the data transfer from memory. The reasoning is as follows.

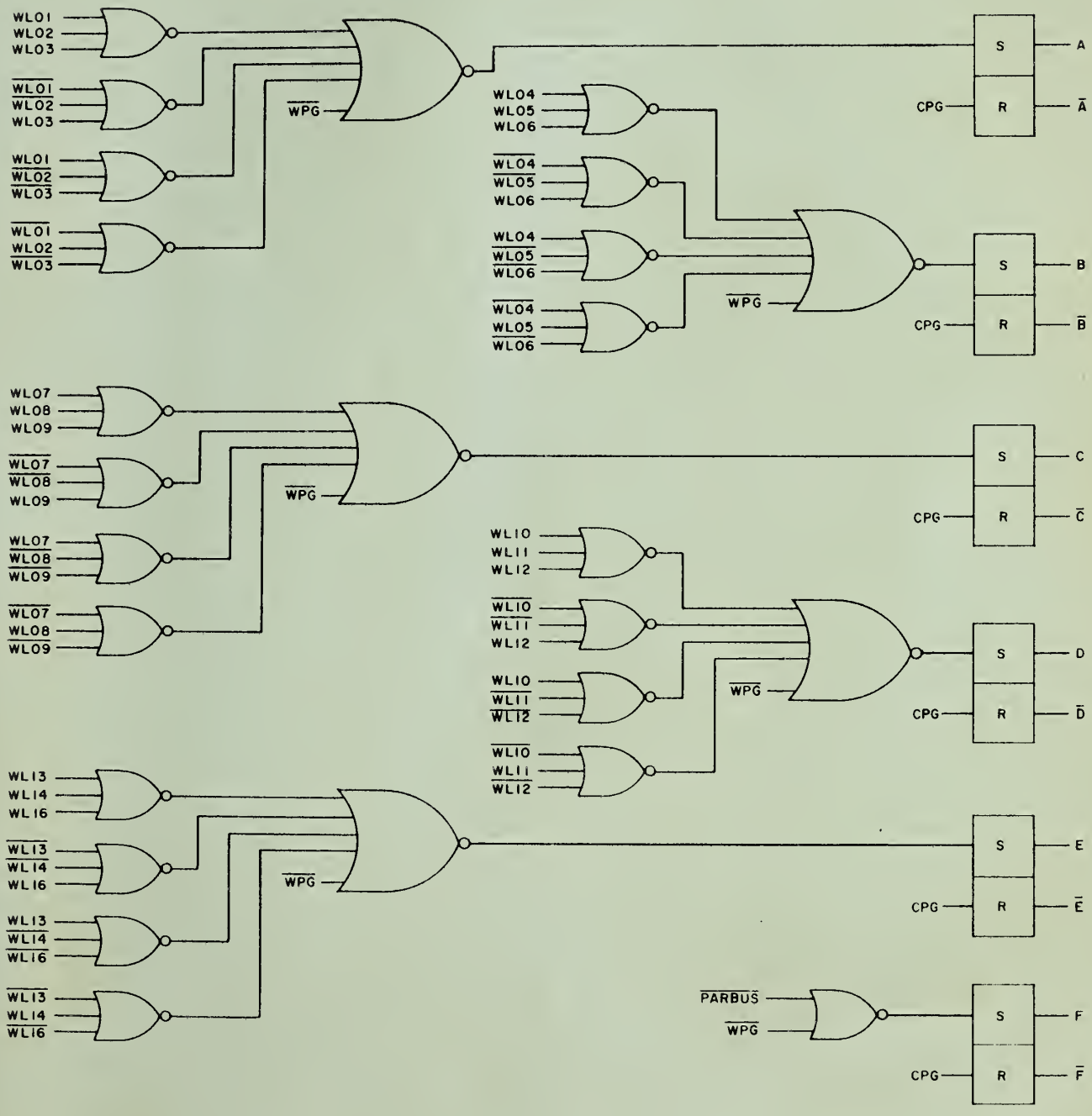


Figure 14-23. Parity Logic and G Register Interface (Sheet 1 of 2)

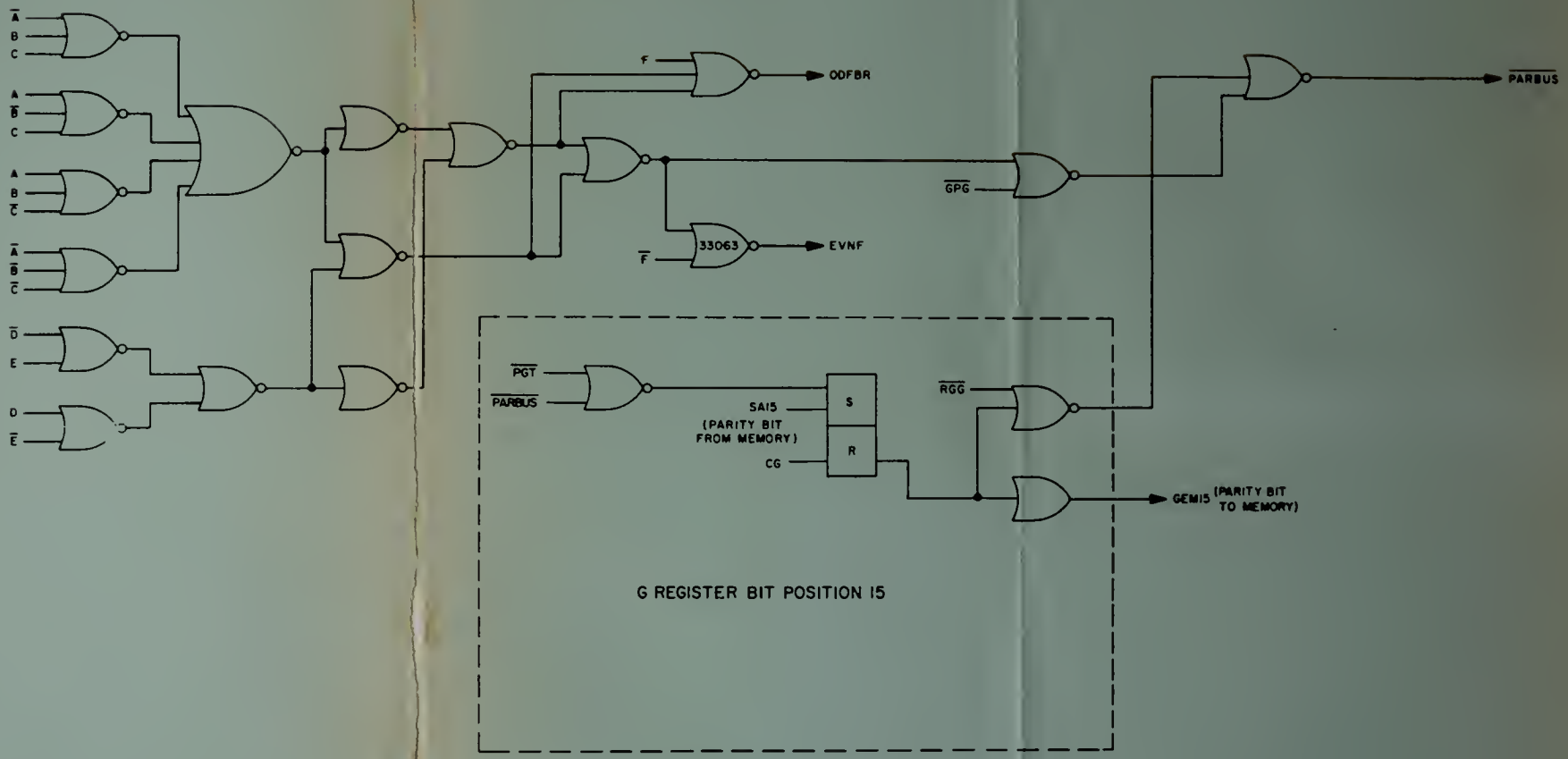


Figure 14-23. Parity Logic and G Register Interface (Sheet 2 of 2)

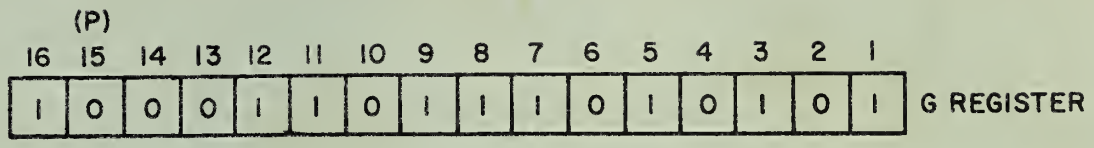


Figure 14-24. Sample G Register Configuration

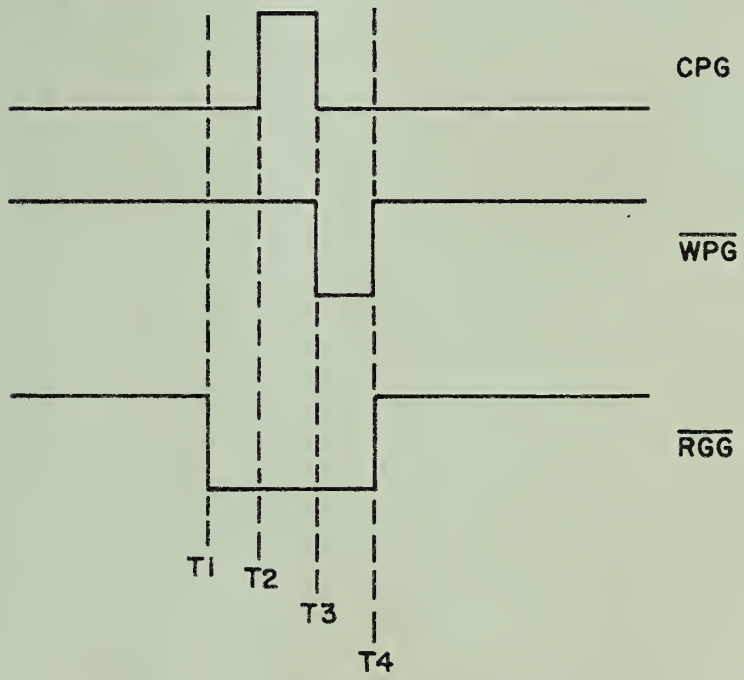


Figure 14-25. Parity Logic Signal Timeline

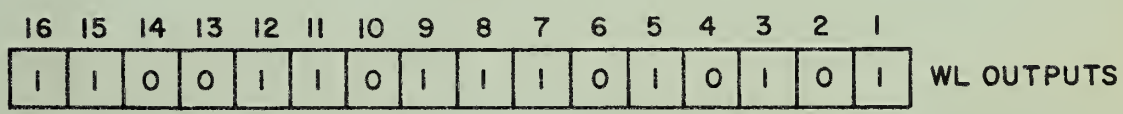


Figure 14-26. Parity Block Inputs #1

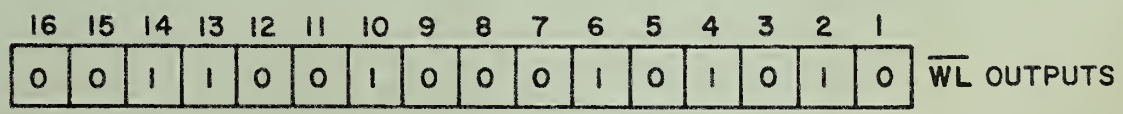


Figure 14-27. Parity Block Inputs #2

Suppose A, $\overline{A}$ through E, $\overline{E}$ have the same configuration as in the preceding paragraph but that F = 1 and $\overline{F}$ = 0. This would mean that A, $\overline{A}$ through E, $\overline{E}$ indicated an odd number of 1's in WL16 and WL14 through WL01 and that F, $\overline{F}$ indicated a parity bit = logic 1. This, of course, would mean that there was an even number of 1's in the word being checked for parity. Since words in memory contain an odd number of 1's, there has been an error in the data transfer from memory. If the reader has correctly manipulated the data given in the last two paragraphs of the previous page, he will find that ODFBR = 1 and EVNF = 0.

When a word is to be written into erasable memory, the parity logic generates a parity bit and writes this parity bit into position 15 of register G. This is accomplished by reading the word from the appropriate register (and placing it on the write lines) into the parity logic. The word is checked for an even or odd logic condition in a manner identical to that described previously, and a parity alarm occurs in case of incorrect parity. The parity bit is written into bit position 15 of register G by signal $\overline{PGT}$ which is generated coincidentally with $\overline{GPG}$. From bit position 15 of Register G, the parity bit is written into memory through the gate with output labeled GEM15.

14.6.10 BASIC DATA FLOW. Figure 14-28 is a block diagram of the central processor including an interface with other functional areas. When a word is gated out of memory, it is first stored in the Register G which serves as a temporary storage area. If the data came from E memory it is normally restored back into E memory after it is read into a register. The parity bit is removed from all words that come from memory. It is routed to the parity block where it is used to make the parity check. It is the interface between Register G and the write amps that cause a duplication of the sign bit to form the overflow/underflow bit. This bit is not written into the parity block or the IN/OUT registers. However, all other registers will receive this bit. There are 16 WL outputs from the write amps which can be gated into any of the central processor registers under control of the sequence generator. Words that are to be written into memory must have a parity bit generated for them in the parity block. This parity bit is sent directly to Register G where it will join the appropriate word that has been gated into Register G via the write amps. Words that are routed from the write amps to Register G do not contain the overflow/underflow bit. This bit is replaced by the newly generated parity bit. The entire word is then written into erasable memory.

14.7 MEMORY

The AGC has erasable and fixed memories. Erasable memory can be written into and read from; fixed memory can only be read from. Erasable memory stores intermediate results of computations, auxiliary program information and variable data suppled by external inputs from the G&N System and other systems in the spacecraft. Fixed memory stores programs, constants and tables. There is a total of 25,600 16-bit word storage locations in fixed and erasable memories. It should be noted that most of the memory capacity is of the fixed variety (24,576 locations). Both memories use magnetic cores as storage devices. However, the cores are used differently in each type of memory.

It is assumed that the reader is familiar with the basic magnetic properties of a ferrite core. A core is a static storage device having two stable states. It can be magnetized in one of two directions by passing sufficient current through wires which pierce the core. The direction of current determines the direction of magnetization. The core will retain its magnetization indefinitely until an opposing current switches the core in the opposite direction. A core is said to be switched if it changes state. Switching currents through the same core are algebraically additive. Wires which pierce a switched core will carry an induced pulse. These are called sense wires.

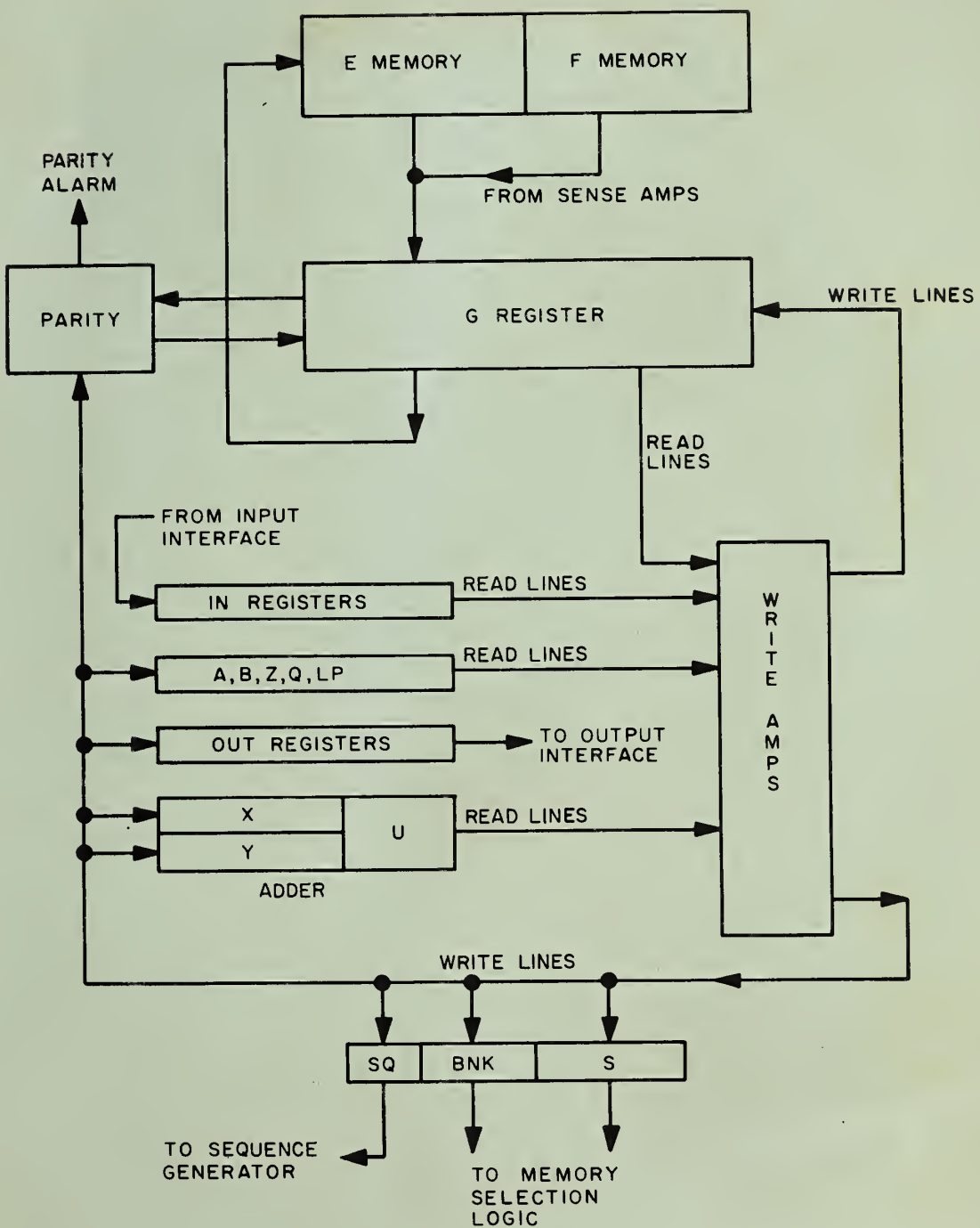


Figure 14-28. Central Processor Block Diagram

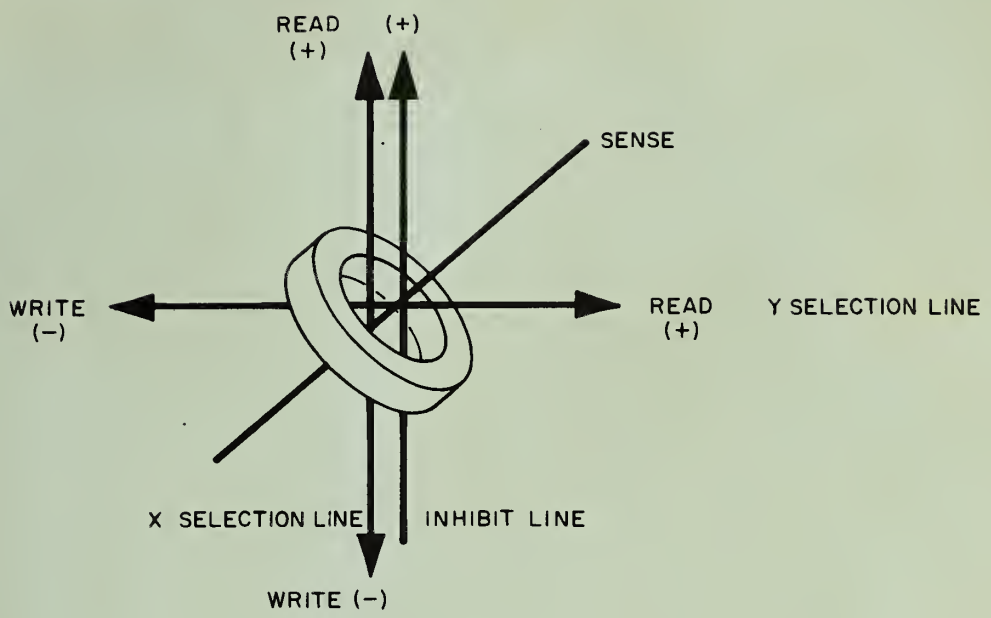
14.7.1 ERASABLE MEMORY. Erasable memory is a coincident-current, ferrite core type, random access memory. It has a capacity of 1,024 words but only 1008 locations are used. Octal addresses 0000_8 through 0015_8 are used to address hardware registers. Addresses 0016_8 and 0017_8 are used as a programmer's convenience (table 14-3). Read-out of erasable memory is destructive; therefore, information required for later used must be restored. One magnetic core is provided for each bit of information; therefore, there are more than 16,000 cores in erasable memory. Only one word is selected for writing into or reading from erasable memory at one time. Selection is controlled by the S register through the address decoder.

14.7.1.1 Core Application. Each core is erasable memory is threaded by four wires: X selection, Y selection, sense and inhibit (figure 14-29). A core is said to be in the "1" state, i.e., the core is storing a logic 1, if it is switched by simultaneous X and Y selection currents of $+ 1/2I_X$ and $+ 1/2I_Y$ respectively (figure 14-29). A core is said to be in the "0" state, i.e., the core is storing a logic 0, if it is switched by simultaneous X and Y selection currents of $-1/2I_X$ and $-1/2I_Y$ respectively. Note that both the X and Y switching currents must be present to switch a core. The necessary switching current = $\pm I$; therefore, the X or Y selection lines can individually only supply half the necessary switching current. To read a core, an attempt is made to switch the core to the 0 state by passing coincident current through the X and Y selection lines in the read direction. If the core is in the 1 state when it is switched, a pulse will be induced on the sense line. If the core is already in the 0 state, there will be no pulse induced on the sense line. Note that if a logic 1 had been stored in the core, this information would be lost since the core is now in the 0 state.

To write a logic 1 into the core, $-1/2I_X$ and $-1/2I_Y$ are passed through the X and Y selection wires. Note that these "write" currents are opposite in direction to the "read" currents. Therefore, an attempt is made to switch the core to the 1 state. The two currents add and cause switching to take place unless it is desired to write a zero into the core. In this case, the inhibit line will carry $+ 1/2I_X$ which will cancel the $-1/2I_X$; consequently, the total switching current = $-1/2I$ which is not enough to switch the core. Therefore, the core remains in the 0 state. Before any core is ever written into, it is first cleared. This amounts to reading a core before writing into it.

14.7.1.2 Core Array. The erasable memory core array consists of (1) 16,384 cores, (2) 32 X selection lines, (3) 32 Y selection lines, (4) 16 inhibit lines and 16 sense lines. The cores are arranged in a cube, 32 x 32 x 16 (figure 14-30). This cube consists of 32 X planes, 32 Y planes and 16 bit planes. The intersection of an X and a Y plane defines a word location. Associated with each (X, Y) plane is one and only one (X, Y) selection line. This line threads each and every core in that plane. Associated with each bit plane is one and only one inhibit line. This line threads each and every core in that plane. Also associated with each bit plane is one and only one sense line which threads each and every core in that plane. The bit plane cores are threaded diagonally by the sense lines and vertically by the inhibit lines (figure 14-31). The inhibit lines are used when data is written into erasable memory; the sense lines are used when data is read from erasable memory.

Since one sense line threads all the cores in a given bit plane, current will be induced in the line if the state of any core in the given plane is changed. Similarly, current through an inhibit line prevents every core in the plane associated with it from changing to the 1 state during writing.



FUNCTION	X	Y	INHIBIT
WRITE ONE	$-\frac{1}{2} I_X$	$-\frac{1}{2} I_Y$	0
WRITE ZERO	$-\frac{1}{2} I_X$	$-\frac{1}{2} I_Y$	$+\frac{1}{2} I_X$
READ (CLEAR)	$+\frac{1}{2} I_X$	$+\frac{1}{2} I_Y$	0

Figure 14-29. Erasable Memory Core Threading

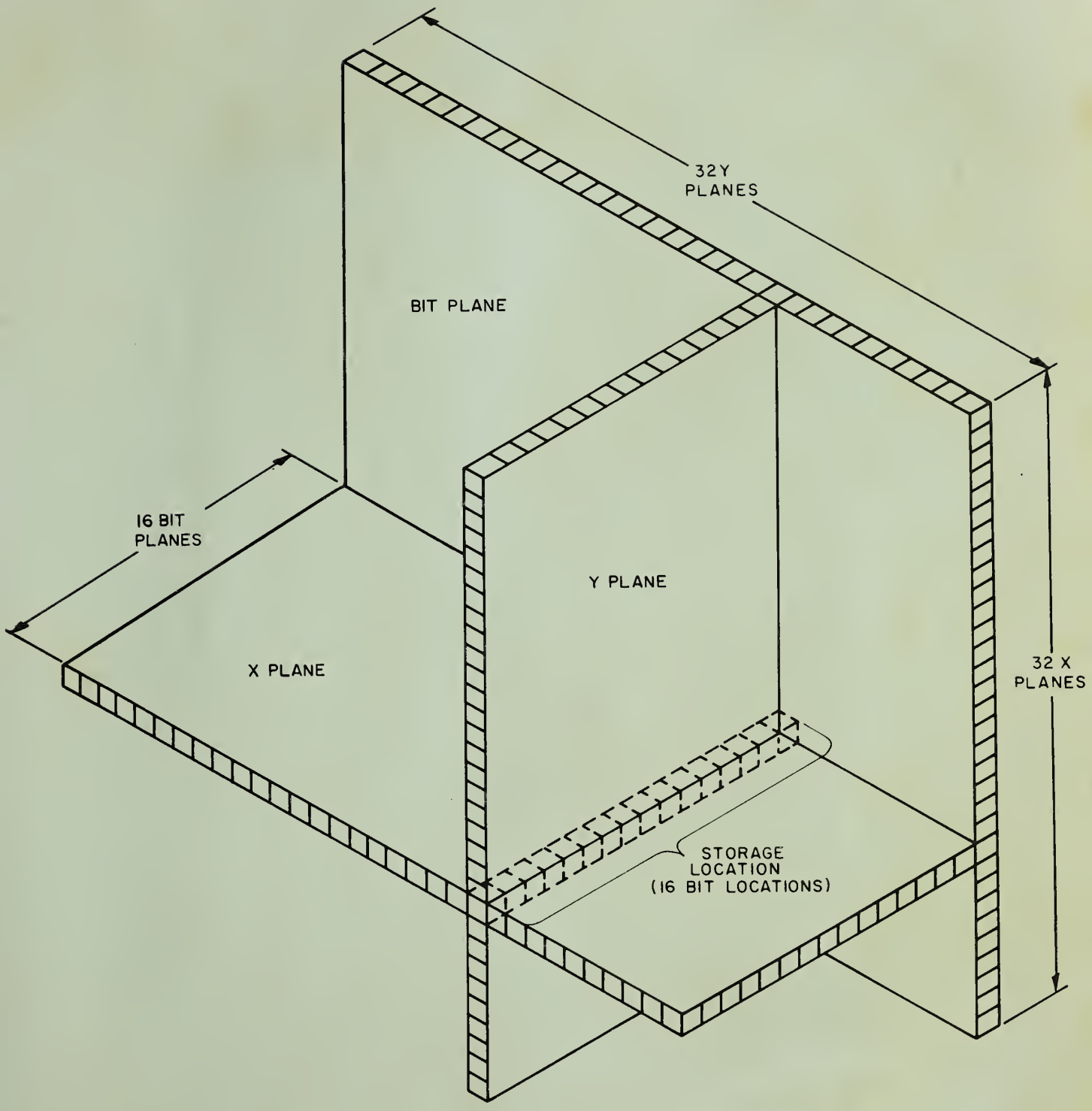


Figure 14-30. Erasable Memory Core Array

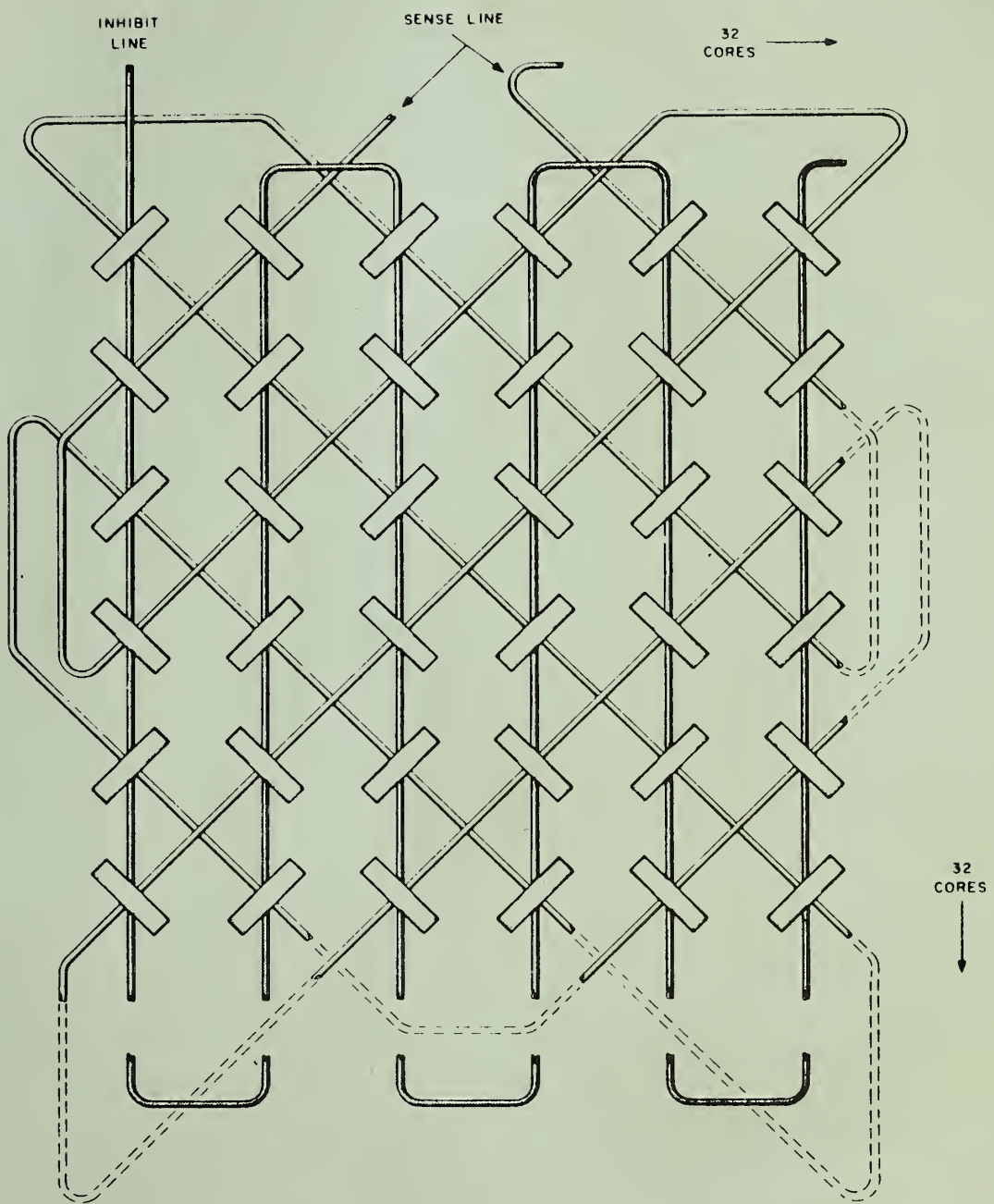


Figure 14-31. Bit Plane Threading

Each X plane is threaded by one X selection line and 32 Y selection lines. Each Y plane is threaded by one Y selection line and 32 X selection lines. To read a word from erasable memory, switching currents $+1/2I_X$ and $+1/2I_Y$ are applied to the proper X and Y selection lines. These lines thread a total of 1024 cores but only 16 of the cores receive both $+1/2I_X$ and $+1/2I_Y$. In other words, only 16 cores receive a current large enough to switch them, i.e., +I. The cores in a "1" state will switch and pulses will be induced on the appropriate sense lines. The cores in a "0" state will not switch and pulses will not be induced on the sense lines associated with these cores. The information read out of erasable memory will be sent to the G Register and then to other areas of the AGC. Note that the 16 cores are now all in the 0 state.

Suppose it is desired to retain the information just read out of erasable memory. Since this information has been destroyed, it must be written back into erasable memory. The G Register still contains the data read out of memory. To write the information back into memory, currents $-1/2I_X$ and $-1/2I_Y$ are applied to the core array. These currents travel on the same X and Y selection lines as described in the previous paragraph. Note that these currents will switch all the 16 defined cores to a "1" state. To prevent those cores that should store a 0 from switching to a 1 state, $+1/2I_X$ is applied to the proper inhibit lines. Therefore, only those cores that receive a total switching current of -I will switch to a 1 state. The other cores will remain in the 0 state.

14.7.1.3 Addressing Erasable Memory. Figure 14-32 is a general block diagram of erasable memory with its associated circuitry. The first 12 bits of an instruction word constitute the address part of the instruction. These are loaded into the S Register and applied to the address decoder. The first 10 bits will uniquely define the location of all 1024 words in erasable memory. If bits 11 and 12 are not both 0, fixed memory is being addressed. The address decoder generates the XB, XT, YB, and YT signals. Table 14-4 lists the inputs and outputs of the address decoder. For instance, if the S Register contained 000000111101 in bits 12 through 1 respectively, the address decoder would produce logic 1 signals YT0, YB1, XT3 and XB5. Signals YT0 and YB1 would be used to choose a Y selection line. Signals XT3 and XB5 would be used to choose an X selection line.

Figure 14-33 is a detailed breakdown of the X selection steering. There are eight separate core switches in the X Bottom Selection Steering Switches Block. These switches are activated by signals XB0 through XB7. The X Top Selection Steering Switches block contains four such switches which are controlled by signals XT0 through XT3. The steering diodes are necessary to facilitate the passage of current in either direction for reading or writing. Figure 14-34 illustrates in detail the operation of the selection switches in the choice of a plane of cores.

Assume that the incoming S Register bits (address) are 0000111101 in bits 10 through 1 respectively. Figure 14-34 shows only the two core switches effected by the X control pulses. The core switches are not a part of the core array. They are, however, magnetic cores with storage properties. Each core has 4 coil windings wound as indicated by the polarity dots. The cores act as small transformers as well as storage devices. The XT3 and XB5 pulses will be generated simultaneously. This causes transistors Q2 and Q4 to be momentarily biased on since their core windings are wired the same as the control pulses. Thus, current will flow in the read direction (from B+ to ground) through one of 32 X selection wires. In addition, the cores are switched in a direction opposing the arrows shown in figure 14-34. The cores essentially remember the location which is being read so that the information can be rewritten back into the same location. The information would otherwise be destroyed. To write requires

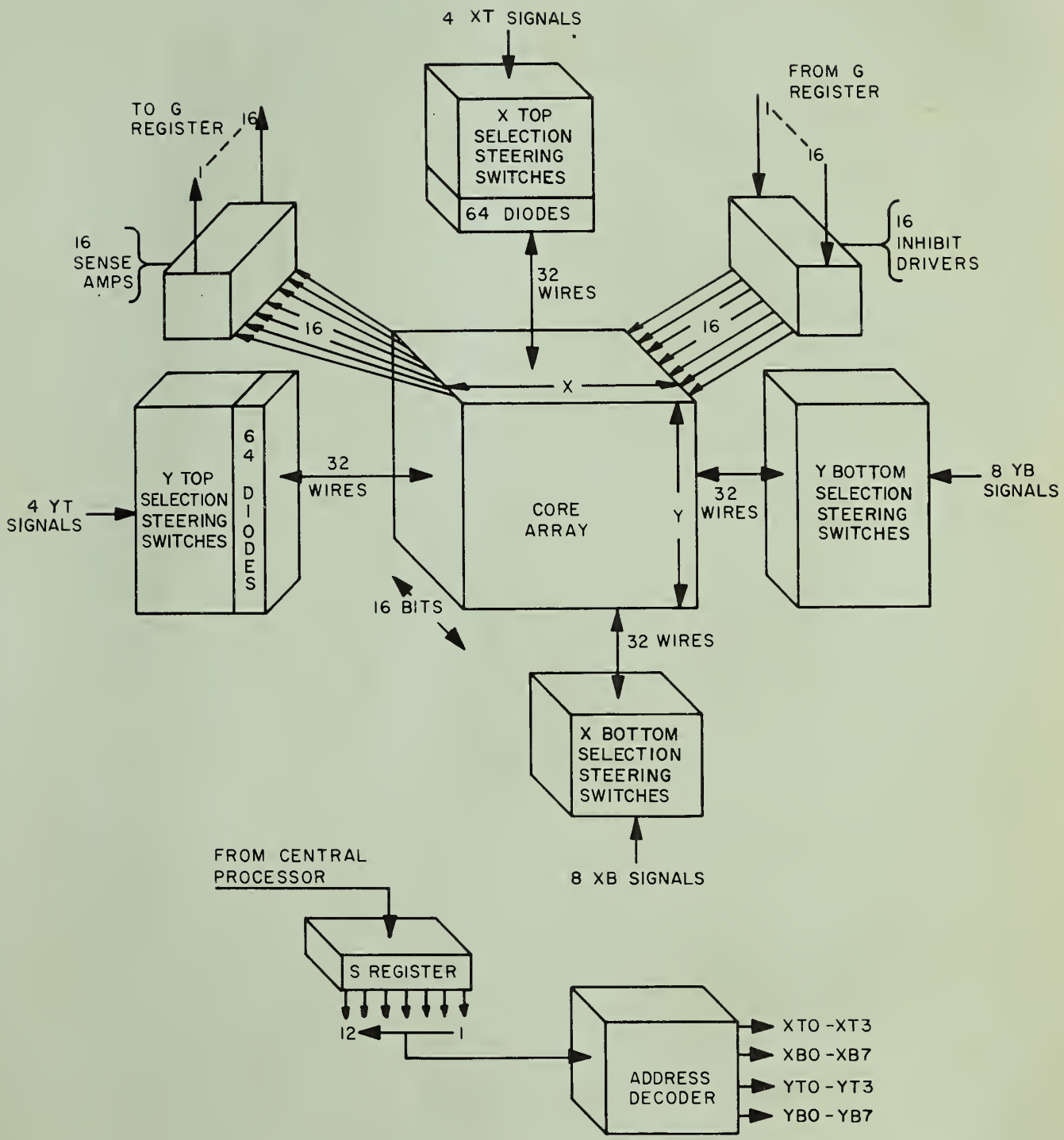


Figure 14-32. Erasable Memory Block Diagram

Table 14-4. Address Decoder Outputs

Signal	Bit		Signal	Bit			Signal	Bit		Signal	Bit		
	10	9		8	7	6		5	4		3	2	1
YT0	0	0	YB0	0	0	0	XT0	0	0	XB0	0	0	0
YT1	0	1	YB1	0	0	1	XT1	0	1	XB1	0	0	1
YT2	1	0	YB2	0	1	0	XT2	1	0	XB2	0	1	0
YT3	1	1	YB3	0	1	1	XT3	1	1	XB3	0	1	1
			YB4	1	0	0				XB4	1	0	0
			YB5	1	0	1				XB5	1	0	1
			YB6	1	1	0				XB6	1	1	0
			YB7	1	1	1				XB7	1	1	1

Contents of the notated bits are the contents of the S Register. Bits 11 and 12 are assumed to be 0. The YT, YB XT and XB signals are outputs of the address decoder and are a logic 1 when the S Register contents are as shown above.

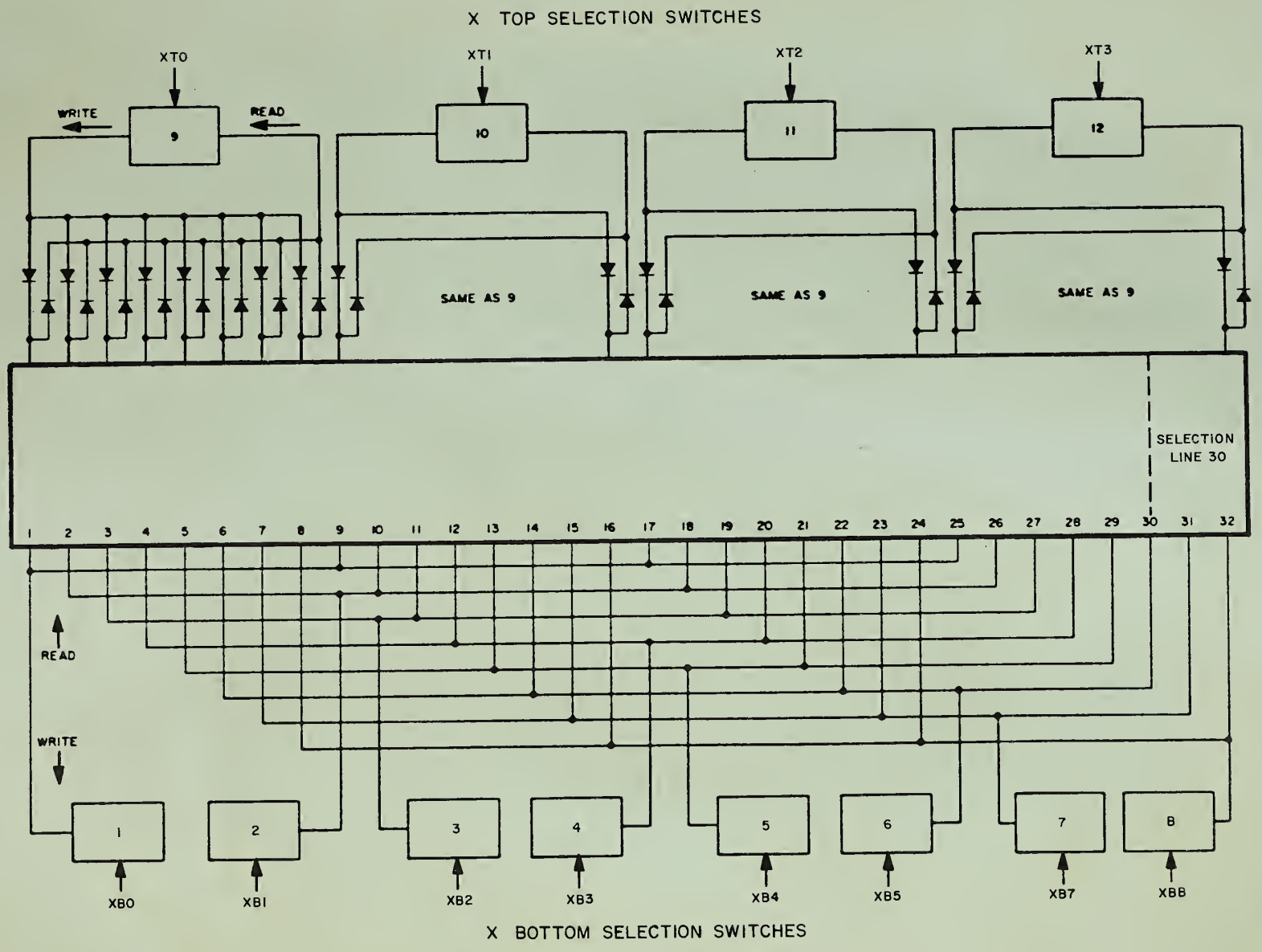


Figure 14-33. "X" Selection Steering

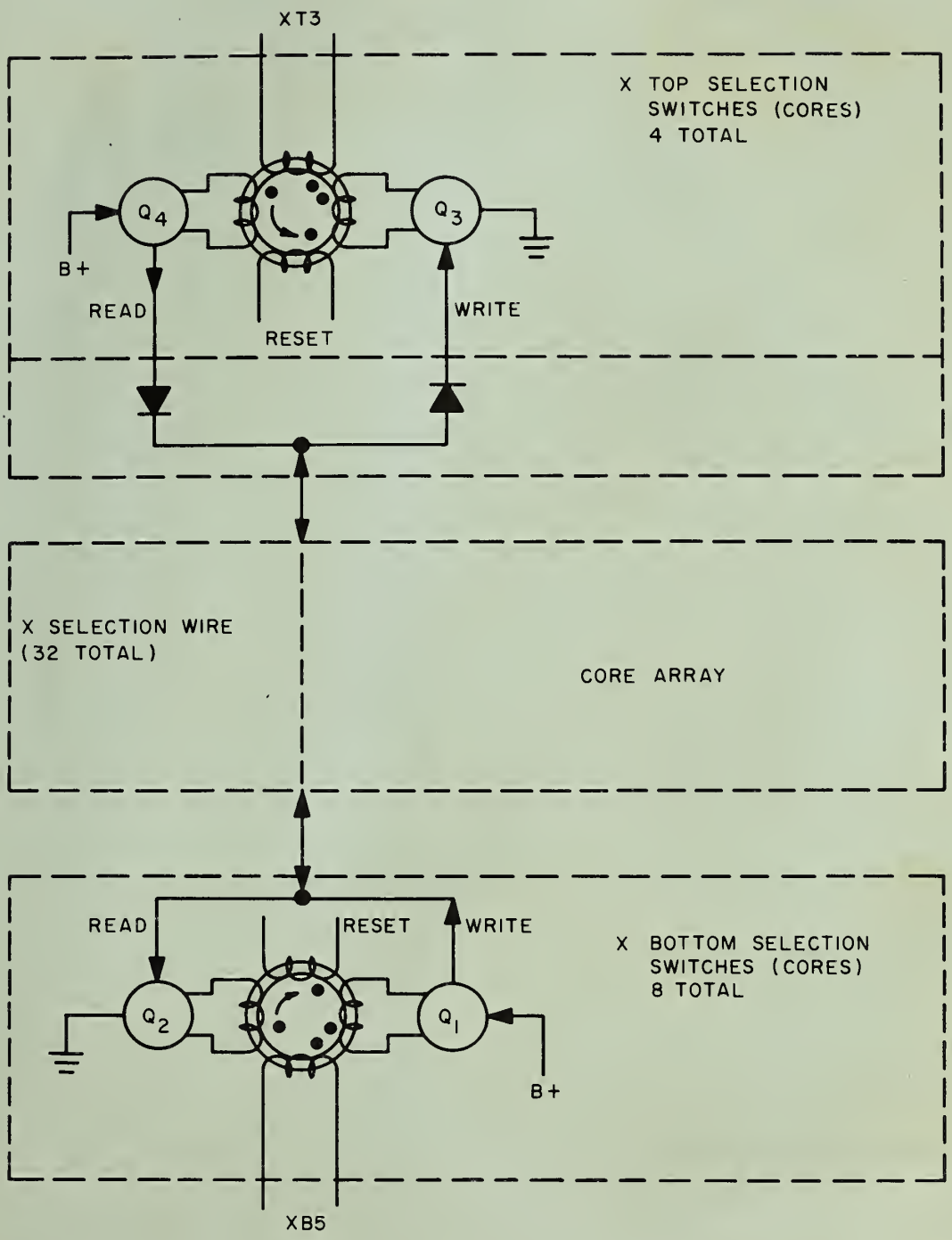


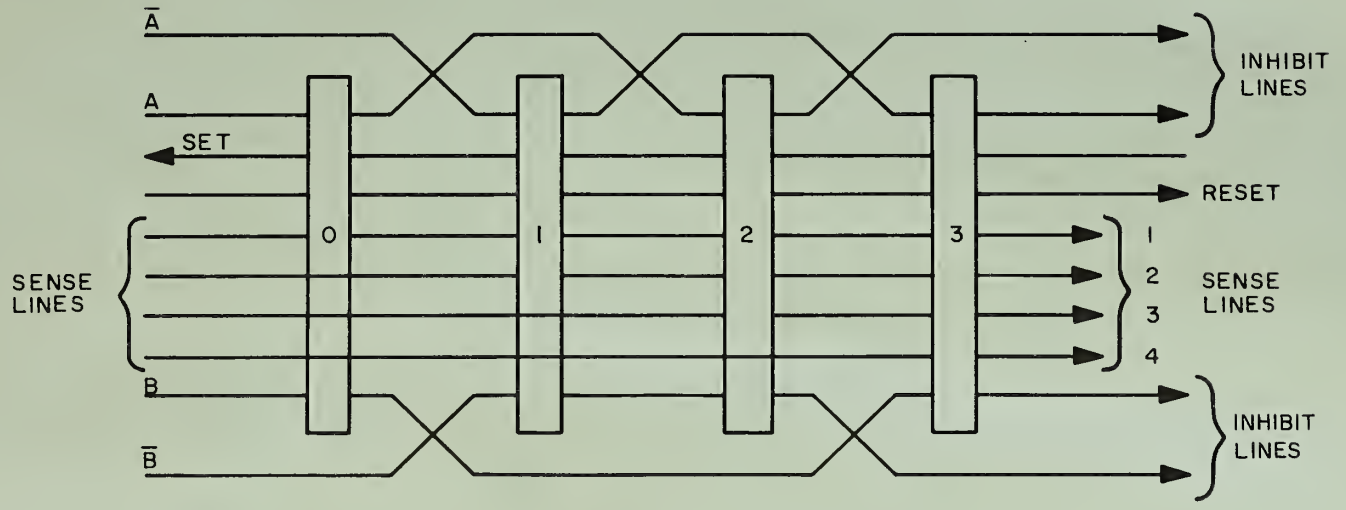
Figure 14-34. Selection of "X" Plane

that current be passed in the opposite direction in the same selection wires. The RESET pulse will be routed to all core switches in the selection switch blocks. Only those switches just previously switched will be in a position to switch back to their original state. This will bias Q1 and Q3 on, allowing conduction of current in the write direction from B+ to ground. Note that the diodes simply steer the current by acting as blocking diodes. The Y selection circuitry is identical to that discussed above. It is the selection of both an X and a Y wire that causes the selection of a 16-bit word. It should be mentioned that regardless of whether it is desired to read out or write into erasable memory, the selection procedure and operation of the core switches is the same. If it is desired to simply write a new word into a location, readout will occur clearing the locations to all zeros. The information read out can be loaded into the G Register where it will control the inhibit wires at the time the RESET pulse is issued. All bits in the selected word will switch to a 1 except those which have inhibiting current running through them. Figure 14-32 shows the inhibit drivers receiving inputs from the G Register to control the 16 inhibit words. Also shown are the sense amps which receive and amplify pulses which are induced onto the sense wires during readout. These amplifier pulses are applied to the G Register where they are stored as logic ONES. There are 16 sense amps, one for each bit in the selected word.

14.7.2 FIXED MEMORY. Fixed memory is a core-rope type with a capacity of 24,576 words. Readout of information from fixed memory is non-destructive. Fixed memory cannot be written into. Information stored in fixed memory is determined by the wiring configuration through the cores and, hence, cannot be changed in any way be electrical means. A rewiring of the fixed memory sticks would be necessary to change any program, table or constant which is stored in fixed memory. The word "rope" arises from the physical picture of the cores with many wires strung through them or around them. Each core in fixed memory will be associated with eight 16 bit words rather than 1 bit as in erasable memory. Since each core is associated with 8 words, there are 3072 cores in fixed memory. The contents of registers S and BANK select locations in fixed memory for readout.

14.7.2.1 Core Application. In the rope core memory, information is permanently stored as a result of the wiring configuration. The direction of magnetization of the core in defining a logic 1 or logic 0 is not applicable. Rather, sense wires routed through the hole of the core will define a logic 1 while a sense line routed around the core will define a logic 0.

Figure 14-35 illustrates the use of the magnetic core in the rope core memory. This hypothetical model consists of 4 cores (edge views) numbered CORE 0 through CORE 3. Each core will store one 4 bit word, numbered WORD 0 through WORD 3. The bit configuration of each word is determined by whether the particular sense wires are routed through the hole or around the hole. The associated table in figure 14-35 shows the bit configuration that would be produced on the sense wires if the associated core was switched. Only one core would be switched at any one time. The problem is one of selecting the desired core to be switched. A two-bit address could be used to uniquely define any one of 4 cores. The A and B inhibit lines (along with their complements) represent the bit configuration of the two-bit address. These wires are routed in and out of the four cores in order to select only one core.



	INHIBIT LINES				SENSE LINES				
	A	Ā	B	B̄	4	3	2	1	
CORE 0	X		X		0	0	0	1	WORD 0
CORE 1		X		X	0	0	1	1	WORD 1
CORE 2	X			X	0	1	1	1	WORD 2
CORE 3		X	X		1	1	1	1	WORD 3

X INDICATES LINE INHIBITS CORE FROM SWITCHING

Figure 14-35. Hypothetical Rope Core

Assume that it is desired to read WORD 2 from memory. In figure 14-35, the direction of the arrows indicate the direction of current flow. Lines that are broken at the core pierce the core. Lines that are continuous at the core are routed around the core. Before reading a core, a current, I, is passed through the RESET line switching all cores into one state of magnetism. Currents are then passed through the SET line, $\overline{A}$ line, and the B line simultaneously in the direction shown. The current, I, in the SET line attempts to switch all cores back to the original state. However, the inhibit wires $\overline{A}$ and B carry current 1/2I in the opposite direction in order to oppose the SET current and cancel its effects. All cores except one will receive inhibiting current. Note that CORE 2 is not pierced by the $\overline{A}$ or B inhibit line. Therefore, CORE 2 changes state. This changing state produces a changing flux field which induces an electrical pulse in all sense lines which pierce the hole. Thus, sense lines 1, 2 and 3 will carry a momentary pulse while sense line 4 carries no pulse. The pulses represent logic ones while the lack of pulses represents a logic zero. The table included in figure 14-35 shows how the inhibit lines are wired to inhibit certain cores from switching. Note that if current is assumed to flow in A it cannot flow in $\overline{A}$. The same idea applies to B and $\overline{B}$. Additional cores could be added to this model by increasing the number of inhibit lines.

In reality, each core of erasable memory is threaded or bypassed by 128 sense lines and 14 inhibit lines. When a core is switched, only 16 of the sense lines are active. These 16 lines carry one word of information.

14.7.2.2 Fixed Memory Layout. Fixed memory consists of three core ropes - R, S and T (figure 14-36). Each core rope contains 1024 cores and is divided into two rope modules. Rope S, for instance, consists of rope modules B21 and B22. Each rope module consists of 512 cores, 4 set lines and 8 strands. Rope module B29, for example, contains set lines A, B, $\overline{C}$, D and strands 04, 05, 06, 07, 28, 29, 30 and 31. A strand is a set of 16 sense lines. Note that the set lines are associated with all the rope modules. In fact, Plane A contains all and only those cores threaded by set line A. Plane B contains all and only those cores threaded by set line B, etc. Only one set line is active when a word is being read from fixed memory. In other words, if set line A is carrying a set current, set lines B, C and D will not be active.

The 512 cores in a rope module can be divided into four groups of 128 cores. One such 128 core group is defined by Plane A in rope module B24. Another such 128 core group is defined by Plane C in rope module B22. Each core in such a group is associated with 128 sense lines and one set line. For example, strands 12-15 and 36-39 are associated with each core in the group defined by Plane C in rope module B22. Since each strand consists of 16 sense lines, there is a total of 128 sense lines associated with each of these cores.

There is a total of 48 strands in fixed memory. Note that any given strand, e.g., strand 30 in rope module B29, is associated with each and every core in its rope module. In other words, each and every strand is associated with a total of 512 cores.

Fixed memory is divided into 24 banks and each bank stores 1024 words. It is important to note that each strand is associated with two and only two banks, and each bank is associated with four strands. For instance, strand 02 is associated with banks 04 and 01, and bank 04 is associated with strands 00-03. Note that each bank is associated with 256 cores.

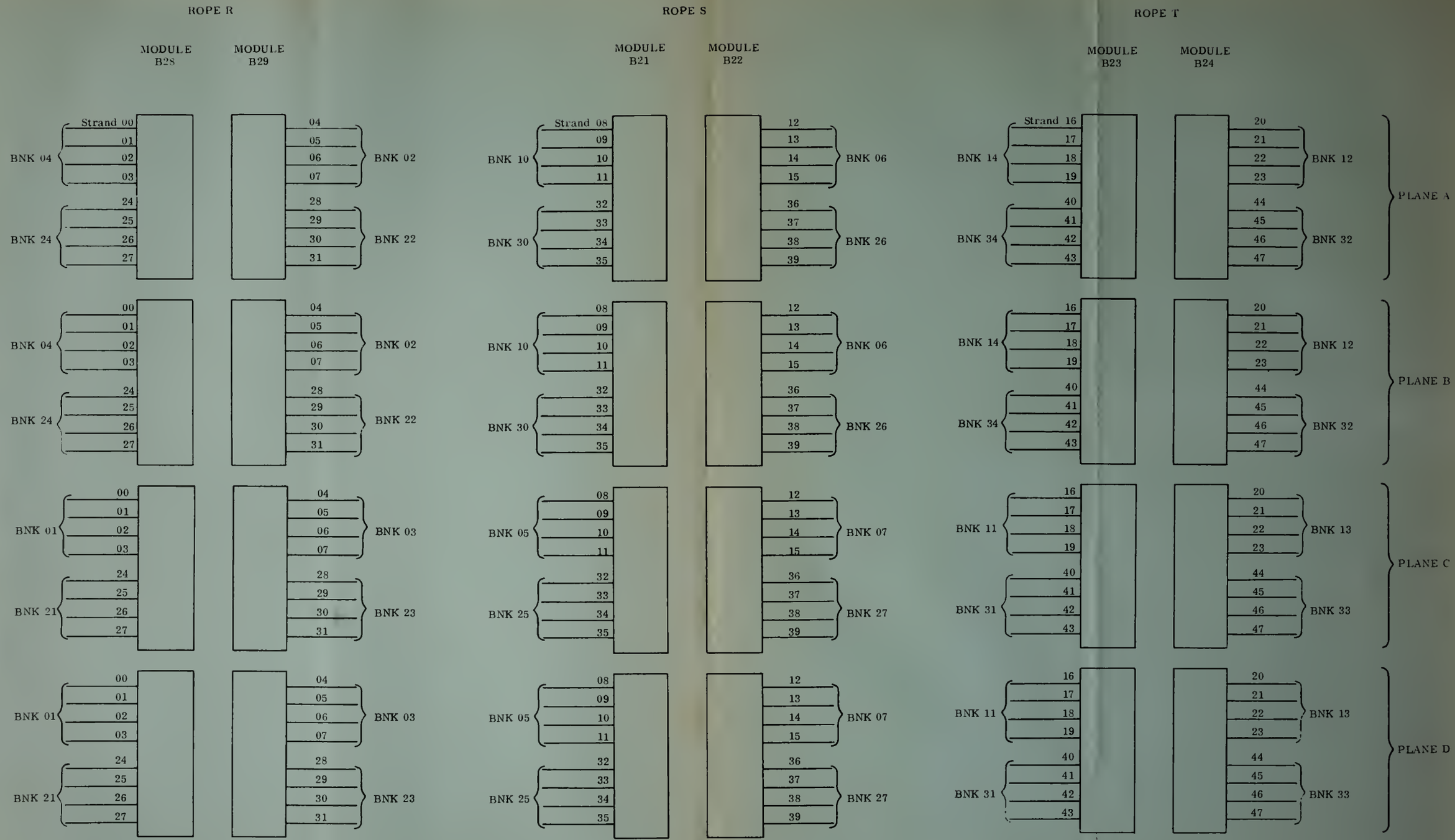


Figure 14-36. AGC Fixed Memory Layout

Assume that one and only one core in fixed memory is switched. Since there are eight strands associated with each core, there are eight possible 16 bit words that could be simultaneously read out. Obviously, this is not a desirable condition. Therefore, it is desirable to select one core to be switched and one of the eight strands associated with that core to be read.

14.7.2.3 Addressing Fixed Memory. The first 10 bits of the S Register were sufficient to define all 1024 erasable memory locations. However, the 12 bits of the S Register are not sufficient to define all the locations in fixed memory. Therefore, the BANK register is used to provide the additional bits necessary to uniquely define a location in fixed memory, i.e., the BANK register is used to extend the addressing capability of the S Register when fixed memory is addressed. Fixed memory is addressed when bits 11 and 12 of the S Register are not both zero. The first two banks in fixed memory are called fixed-fixed (FF) memory. The other 22 banks comprise the fixed-switchable (FS) memory. The distinction arises from the selection techniques employed. Fixed-fixed memory can be addressed using the S Register only. When bits 11 and 12 are 01 or 10, FF memory is being addressed. When FS memory is addressed, bits 11 and 12 of the S Register must always be logic ones. Thus, bits 11 and 12 of the S Register will determine whether erasable memory, FF or FS memory is being addressed. To address FS memory, the programmer must load the BANK register with the bits corresponding to the desired bank. This is done by addressing the BANK Register using 0015_8. In addition, the programmer must insure that bits 11 and 12 of the S Register are both ones. The following description describes the selection of a fixed memory location. The reader should provide himself with additional examples in order to obtain the proper feel for this material. In obtaining this feel, the reader will probably understand why fixed memory is often referred to by less accurate, but seemingly more appropriate, terms.

Assume that the BANK register contains 1, 0, 0, 1, 0 in bits 15 through 11, respectively. Assume also that the S Register contains 1, 1, 1, 0, 1 in bits 12 through 8, respectively. Therefore, IL09A = 0, IL10 = 1 and RPG4 = 1 (table 14-5). The other RPG signals are a logic 0. Table 14-5 is simply an input/output listing. It can be thought of as a box with the BANK register's contents and bits 11 and 12 of the S Register as inputs. The outputs would be signals IL09A, IL10A and RPG1 through RPG6.

Figure 14-37 is the set line selection logic. This group of gates determines which of the four set lines will be selected. In other words, these gates determine the plane in which the switched core will be located. Choosing one of the four possible set lines immediately eliminates 3/4 of fixed memory's storage. SET B = 1 because IL09A = 0 and ST08 (bit 8 of Register S) = 1 (figure 14-37). Note that signals SET A, SET C and SET D are logic 0's. Note also that all banks in fixed memory have been eliminated except banks 04, 24, 02, 22, 10, 30, 06, 26, 14, 34, 12 and 32 (figure 14-36).

Since RPG4 = 1 and all the other RPG signals = 0, all banks except 24 and 22 can be eliminated from consideration (figure 14-38). Note, in this figure, that the only AND gates which can possibly have a logic 1 output are those to which RPG4 = 1 is applied. Therefore, the only strands which can possibly be enabled are strands 24 through 31. Since Planes A, C and D have been eliminated, the only banks associated with these strands in Plane B are banks 22 and 24 (figure 14-36).

Table 14-5. Fixed Memory Selection Signals

Bank Register					S Reg		IL09A	IL10A	Rope Control Signal	Bank
15	14	13	12	11	12	11				
x	x	x	x	x	0	1	1	0	RPG1	01
x	x	x	x	x	1	0	0	1		02
0	0	0	x	x	1	1	1	1		03
0	0	1	0	0	1	1	0	0		04
0	0	1	0	1	1	1	1	0	RPG2	05
0	0	1	1	0	1	1	0	1		06
0	0	1	1	1	1	1	1	1		07
0	1	0	0	0	1	1	0	0		10
0	1	0	0	1	1	1	1	0	RPG3	11
0	1	0	1	0	1	1	0	1		12
0	1	0	1	1	1	1	1	1		13
0	1	1	0	0	1	1	0	0		14
1	0	0	0	1	1	1	1	0	RPG4	21
1	0	0	1	0	1	1	0	1		22
1	0	0	1	1	1	1	1	1		23
1	0	1	0	0	1	1	0	0		24
1	0	1	0	1	1	1	1	0	RPG5	25
1	0	1	1	0	1	1	0	1		26
1	0	1	1	1	1	1	1	1		27
1	1	0	0	0	1	1	0	0		30
1	1	0	0	1	1	1	1	0	RPG6	31
1	1	0	1	0	1	1	0	1		32
1	1	0	1	1	1	1	1	1		33
1	1	1	0	0	1	1	0	0		34

x means a 1 or 0

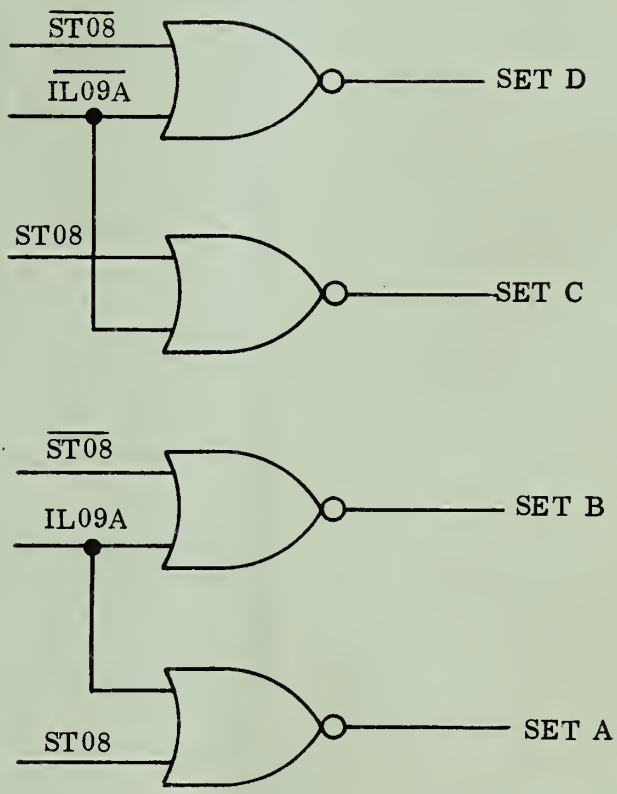


Figure 14-37. Set Line Selection Logic

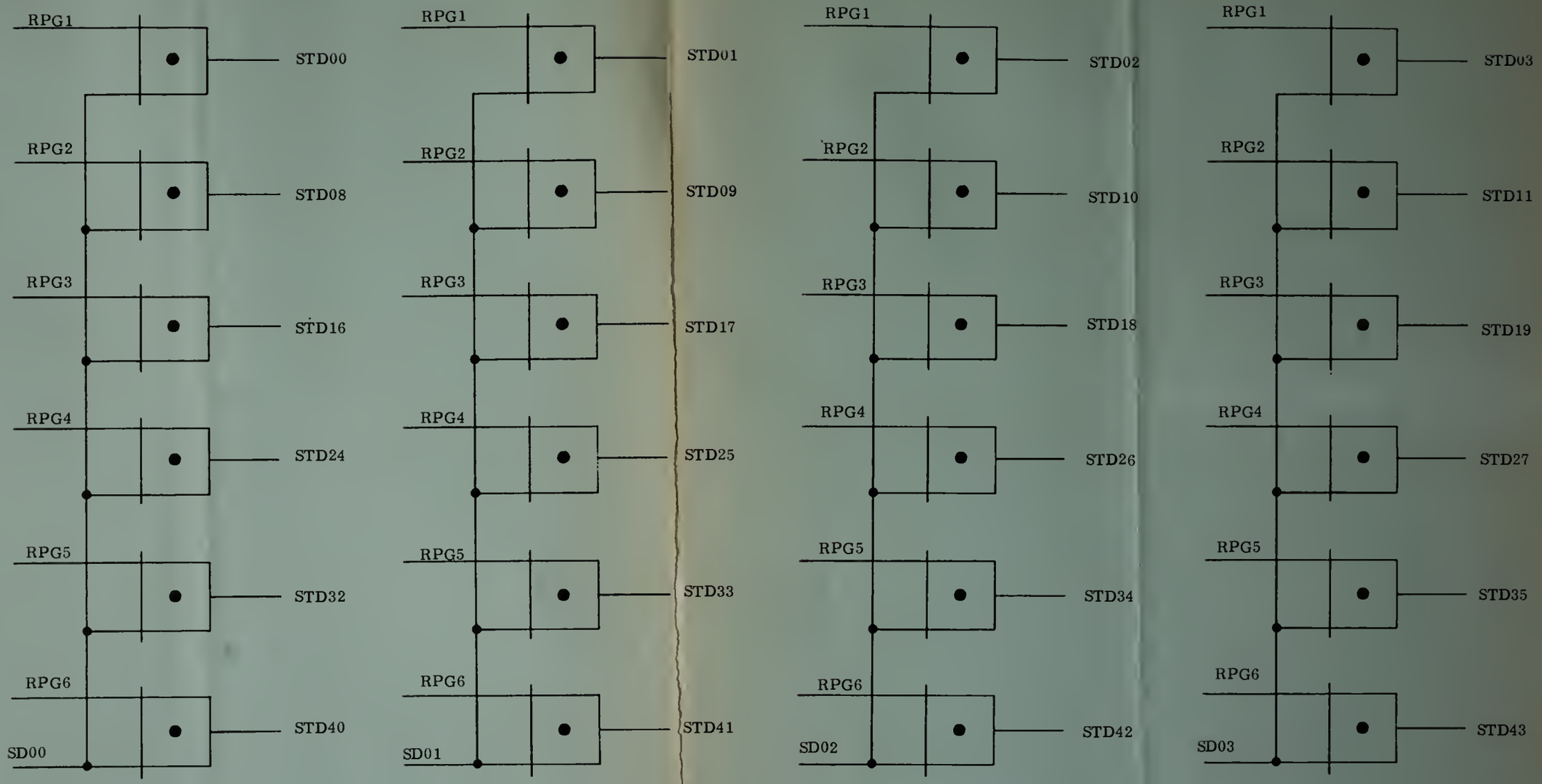


Figure 14-38. Strand Line Selection Logic (Sheet 1 of 2)

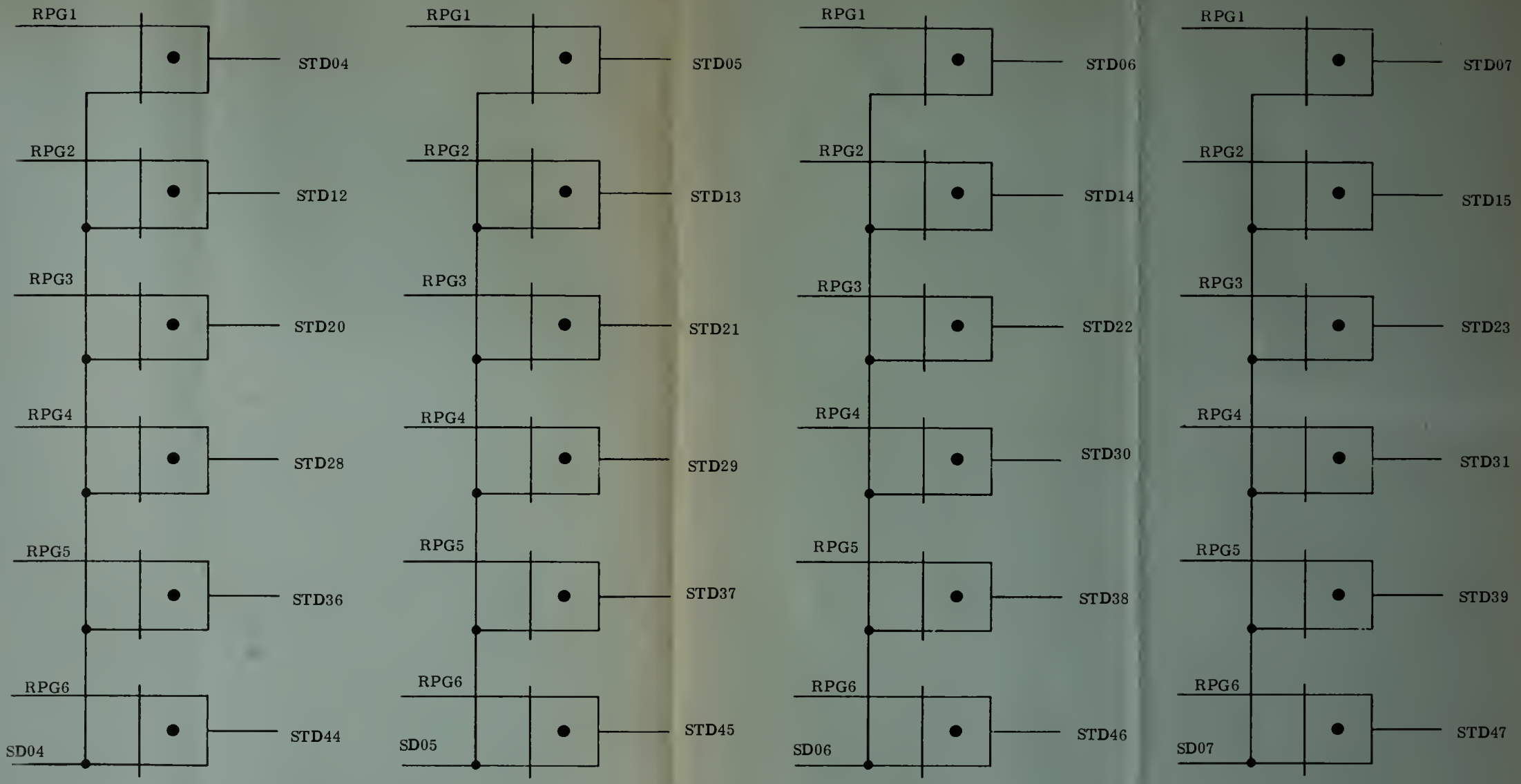


Figure 14-38. Strand Line Selection Logic (Sheet 2 of 2)

It is now necessary to select one strand. Note that the selection of one strand will also eliminate one of the two remaining banks. Associated with each group of six strands is a strand gate. For example, in figure 14-38, strands 01, 09, 17, 25, 33 and 41 are associated with strand gate 01. When strand gate 01 is enabled, signal SD01 = 1. Figure 14-39 is the strand gate selection logic. Since IL10A = 1 and bits 10 and 9 of Register S are 1 and 0 respectively, strand gate 06 is enabled and SD06 = 1. Since SD06 = 1 and RPG4 = 1, strand 30 is enabled, i.e., STD 30 = 1 (figure 14-38). Strand 30 is associated with all 128 cores in Plane B of rope module B29. If one of these cores is switched while the other 127 are inhibited, the configuration of the 16 sense lines in strand 30 with respect to the switched core will determine the information read from fixed memory. It has been previously stated that there are 14 inhibit lines associated with each core in fixed memory. Seven of these lines, however, are simply complements of the other seven. Therefore, seven independent bits of information will suffice in inhibiting 127 of 128 cores because $2^7 = 128$. Bits 1 through 7 of the S Register supply the 7 independent bits of information which inhibit 127 of the 128 cores associated with strand 30.

Figure 14-40 is a gross block diagram of the selection circuitry discussed in preceding paragraphs. The reader should check this drawing against figures 14-37 through 14-39.

A few general remarks on fixed memory will be made before the topic is considered completed. Note, in figure 14-41, the relationship between the BANK Register's content and the bank selected in fixed memory (table 14-5).

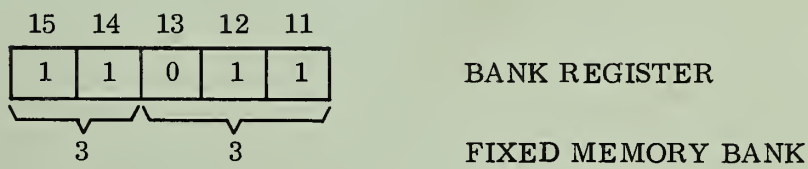


Figure 14-41. BANK Register and Fixed Memory Bank Relationship

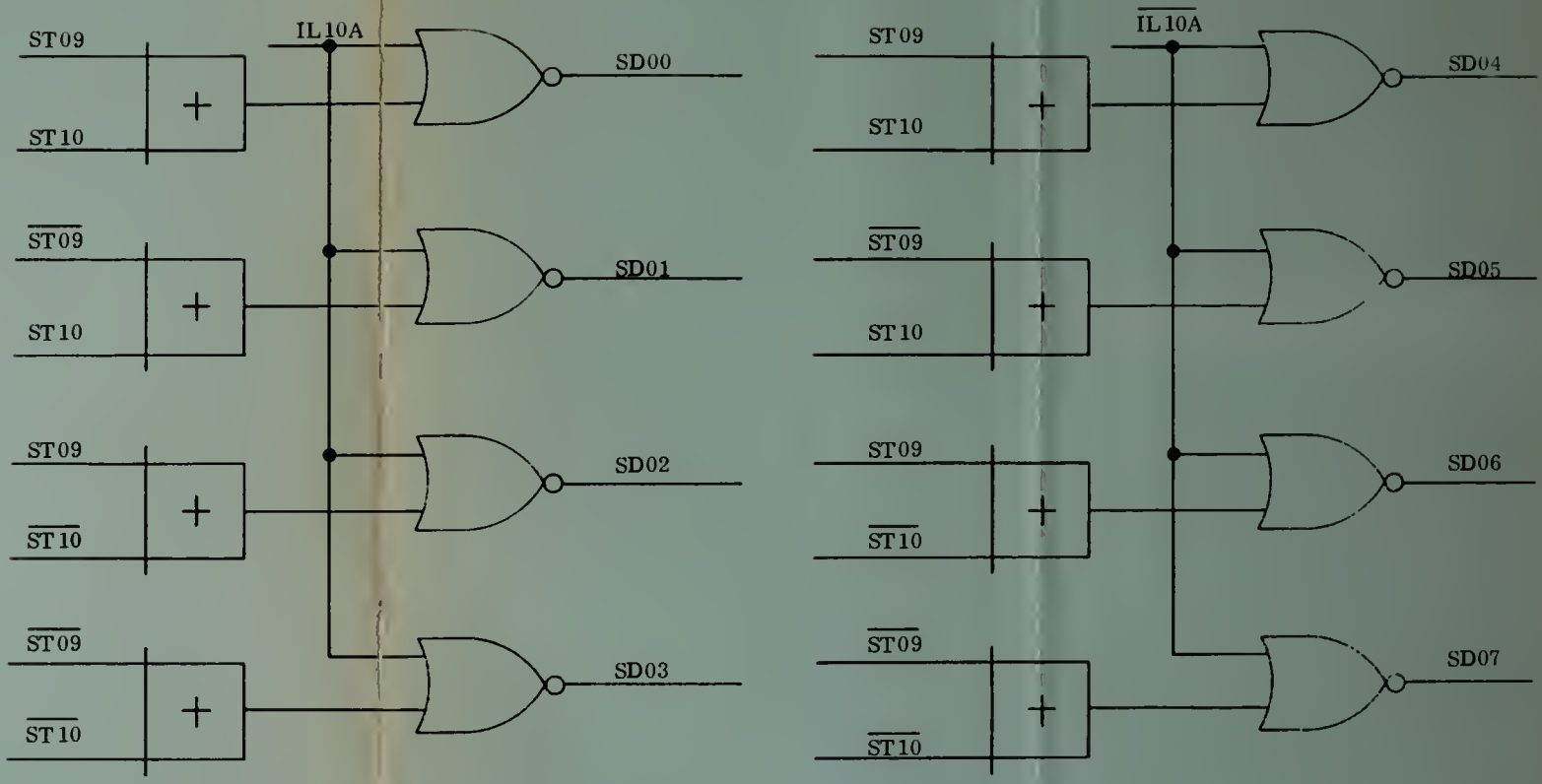


Figure 14-39. Strand Gate Selection Logic

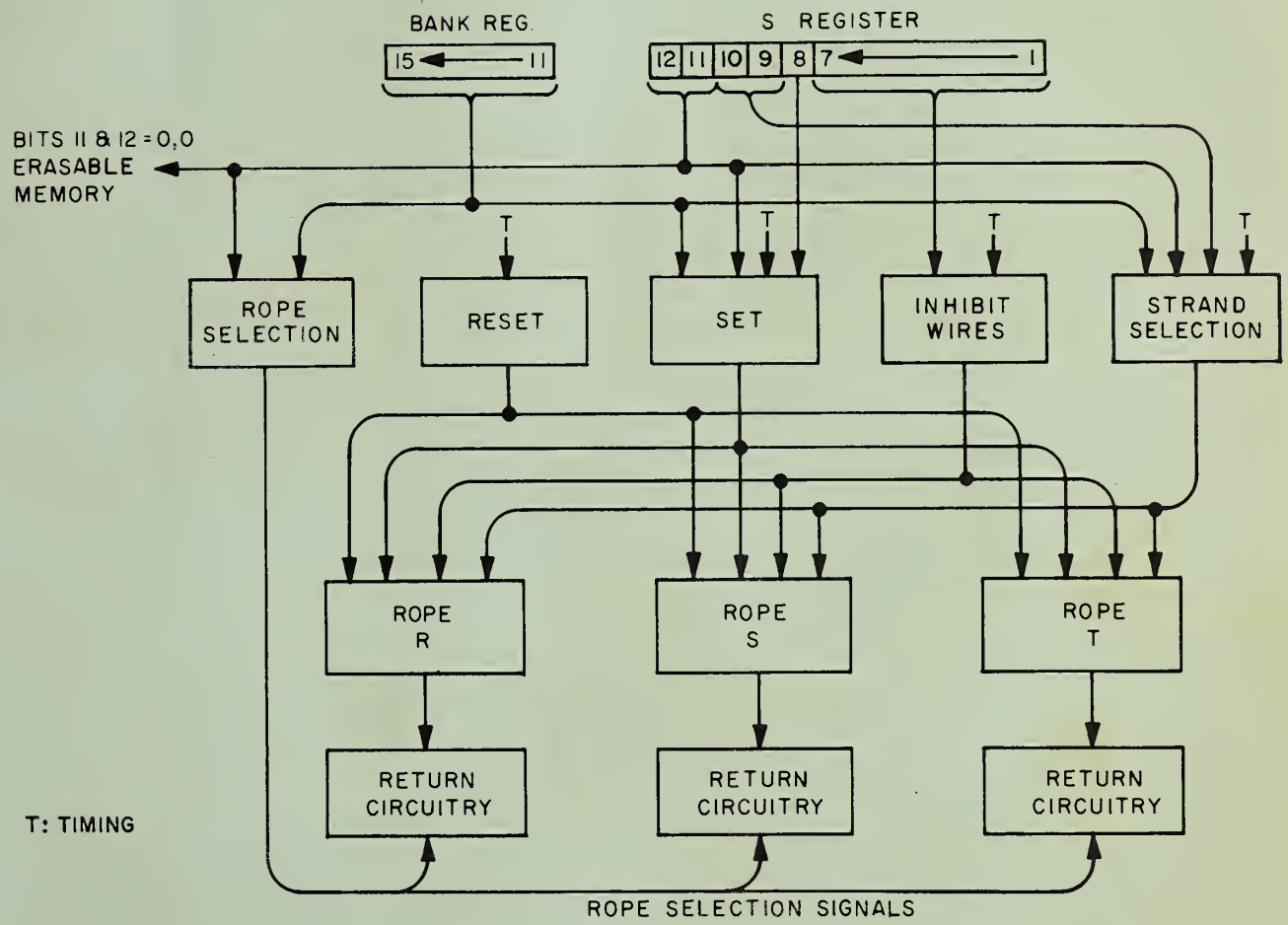


Figure 14-40. Fixed Memory Organization and Selection

Assume bits 11 and 12 of Register S to be logic 1's and the configuration of the BANK Register to be that of figure 14-41. According to table 14-5, the register configuration stated in the preceding sentence will uniquely define bank 33 in fixed memory. Bank 33 (figure 14-36) is defined by planes C and D and strands 44 through 47. Since IL09A = 1 (table 14-5), either SET D or SET C will be a logic 1 (figure 14-37). The logic level of ST08 is not known and, consequently, both plane D and plane C must be considered. Since IL10A = 1, any one of the strand gates from 04 to 07 could be enabled (figure 14-39). Since RPG6 = 1 and SD04 through SD07 are all equally likely to be a logic 1, signals STD 44 through STD 47 are equally likely to be a logic 1 (figure 14-38). Therefore, bank 33 has been uniquely defined.

14.8 SEQUENCE GENERATOR

The function of the sequence generator is to direct the execution of machine instructions. The sequence generator combines basic timing pulses defining action times with the order code to produce a set of sequential "control pulses". These pulses control the sequencing of data within the computer as they carry out the instruction defined by the order code. "Forced" instructions are involuntary instructions that are normally requested by external stimuli. There are no order codes associated with these instructions. Control pulses to execute these instructions, however, are generated in a similar manner.

14.8.1 INSTRUCTIONS.

Instructions are directions given to the AGC to perform certain specific operations. Together with addresses, they constitute the building blocks of a program. Programs are sequential lists of instruction words which usually contain instructions and addresses. There are several types of instructions used in the AGC. They may be categorized as follows:

MACHINE (21)

- REGULAR (11)
  - BASIC (8)
  - EXTRA CODE (3)
- INVOLUNTARY (6)
- MISCELLANEOUS (4)

INTERPRETIVE (71)

There are two general categories of instructions: machine and interpretive. Machine instructions can be interpreted and executed directly by using the sequence generator to control computer operation. Interpretive instructions are a programmer's convenience and must be interpreted under program control, converted to machine instructions and then executed as machine instructions. The following paragraphs will discuss the three types of machine instructions separately.

14.8.1.1 Regular Instructions. Regular instructions are those defined by order codes. The order code is always programed within the instruction word along with an associated address which is represented by the letter K. The 8 basic instructions can be directly interpreted. The 3 extra code instructions require an indexing of the basic instructions for their generation. Table 14-6 lists the basic instructions along with their mnemonic codes, octal codes and associated purpose. The address, K, represents either a memory location or an addressable central processor register. c(K) represents the contents of K, i.e., the data located in K. The letters L, L + 1, L + 2, etc., are used to designate the addresses of successive instruction words stored in memory. c(L), c(L + 1), etc., indicate the contents of locations L, L + 1, L + 2, i.e., the instructions located in L, L + 1 and L + 2.

14.8.1.1.1 Instruction TC K (Order Code 0). Instruction TC K transfers control to the instruction stored at location K. Instruction TC K does not disturb the accumulator content or the content of location K. The basic instruction address that is skipped by instruction TC K is stored in Register Q and returned to by instruction TC Q. This instruction gives the computer the capability of jumping from program to program. This is called an unconditional jump.

14.8.1.1.2 Instruction CCS K (Order Code 1). The count, compare and skip instruction provides the computer with a conditional jump capability. That is, the AGC will alter its normal sequential reading of instructions on the basis of the sign and magnitude of the data in location K. In addition, the absolute value of K will be decremented by one. There are four possibilities:

a. The instruction at location L + 1 is executed next if the data at location K is greater than plus zero. Instruction CCS K then writes the content of location K into the accumulator and decrements the accumulator content by one.

b. If the data at location K is equal to plus zero, the instruction at location L + 2 is executed next. Instruction CCS K then clears the accumulator and sets the accumulator to plus zero.

c. If the data at location K is less than minus zero, the instruction at location L + 3 is executed next. Instruction CCS K then reads the complement of the content of location K into the accumulator and decrements the accumulator by one.

d. If the data at location K is equal to minus zero, the instruction at location L + 4 is executed next. Instruction CCS K then clears the accumulator and sets the accumulator content to plus zero.

The contents of K are not disturbed during this process.

14.8.1.1.3 Instruction NDX K (Order Code 2). The index instruction adds c(K) to the contents of the next instruction address, L + 1. The result is the next instruction. This process is called indexing or modifying an instruction.

14.8.1.1.4 Instruction XCH K (Order Code 3). The exchange instruction exchanges the accumulator content with c(K). Location K may be in erasable memory or fixed memory. If the address is in fixed memory, the instruction amounts to a clear and add instruction. No operation occurs and the instruction at L + 1 is executed next if K is the address of the accumulator. Results are therefore similar to instruction TC K + 1. However, XCH K may be preferred because the content of Register Q is preserved.

Table 14-6. Regular Instructions

Mnemonic	Octal Code	Name	Purpose
BASIC INSTRUCTIONS			
TC K	0	Transfer control	Transfers control to instruction at K
CCS K	1	Count, compare and skip	Branches to one of four instructions specified by c(K)
NDX K	2	Index	Modifies next instruction
XCH K	3	Exchange	Exchanges accumulator content with c(K)
CS K	14	Clear and subtract	Enters the complement of the content of K into the accumulator.
TS K	15	Transfer to storage	Transfers accumulator content to K
AD K	16	Add	Adds C(K) to accumulator content
MSK K	17	Mask	AND's accumulator content with c(K)
EXTRA CODE INSTRUCTIONS			
MP K	11	Multiply	Multiplies accumulator content by c(K)
DV K	12	Divide	Divides accumulator content by c(K)
SU K	13	Subtract	Subtracts c(K) from accumulator content

14.8.1.1.5 Instruction CS K (Order Code 14). Instruction clear and subtract K clears the accumulator and reads the complement of c(K) directly into the accumulator. Instruction CS K does not disturb the content of location K. If K is the address of the accumulator, the content of the accumulator is complemented.

14.8.1.1.6 Instruction TS K (Order Code 15). Instruction TS K, transfer to storage, transfers the content of A to K directly if no overflow or underflow occurs and the content of A is not disturbed. The content of A, less the overflow or underflow bit, is transferred to K. If overflow or underflow occurs, the overflow counter (OVCTR) is respectively incremented or decremented. This causes the AGC to execute the instruction at L + 2 next.

14.8.1.1.7 Instruction AD K (Order Code 16). Instruction add K reads the content of location K into the accumulator if the accumulator is initially clear. If the accumulator contains a number, instruction AD K adds the content of location K to the accumulator content. The result is placed in the accumulator. Instruction AD K does not disturb the content of location K If K is the accumulator address, the accumulator content is doubled. In case of overflow or underflow, the OVCTR counter is respectively incremented or decremented.

14.8.1.1.8 Instruction MSK K (Order Code 17). Instruction MASK K logically AND's the accumulator content with the content of K. The result is placed in the accumulator. The c(K) is not disturbed during this process.

14.8.1.1.9 Instruction MP K (Order Code 11). Instruction MP K is an extra code instruction which is generated by using the NDX instruction. Once generated, the instruction multiplies c(A) by c(K). The result is a 28-bit product in the register A and register LP. Register LP contains the low order bits (14 through 1). Instruction MP K does not disturb the content of location K. The accumulator content is squared by this instruction if K is the address of the accumulator.

14.8.1.1.10 Instruction DV K (Order Code 12). Instruction DV K, divide K, is an extra code instruction formed by indexing. c(A) is divided by c(K). The result is a 14-bit quotient in the accumulator. The binary point is set between bits 15 and 14 of the accumulator content. Any remainder is a whole number with the binary point to the right of bit 1. Instruction DV K does not disturb the content of location K.

14.8.1.1.11 Instruction SU K (Order Code 13). Instruction SU K, subtract K, is the third extra code instruction formed by indexing. The SU K instruction subtracts c(K) from c(A). The result is placed in the accumulator. Instruction SU K does not disturb the content of location K. If the accumulator is initially clear, instruction SU K copies the complement of the location K content into the accumulator. If K is the address of the accumulator, the result in the accumulator is minus zero. In case of overflow or underflow, the OVCTR counter is respectively incremented or decremented.

14.8.1.2 Involuntary Instructions. Involuntary instructions (table 14-7) consist of program priority control and counter priority instructions. These instructions do not have associated order codes. They are generated by the priority control and sequence generator circuitry in response to external inputs.

14.8.1.3 Miscellaneous Instructions. Miscellaneous instructions (table 14-8) consist of start instructions and display and load instructions associated with the CTS (Computer Test Set).

Table 14-7. Involuntary Instructions

Mnemonic	Name	Purpose
PRIORITY INSTRUCTION		
RUPT	Interrupt	Interrupts current program
RSM	Resume	Resumes interrupted program
COUNTER INSTRUCTION		
PINC	Plus increment	Increments content of addressed counter
MINC	Minus increment	Decrements content of addressed counter
SHINC	Shift	Shifts content of addressed counter one place to left
SHANC	Shift and add one	Shifts content of addressed counter one place to left and adds one

Table 14-8. Miscellaneous Instructions

Mnemonic	Name	Purpose
START INSTRUCTIONS		
GO	Go	Starts computer
TCSA	Start at specified address	Executes program at specified address
DISPLAY AND LOAD INSTRUCTIONS		
OINC	Display	Displays content of addressed location
LINC	Load	Loads addressed location

14.8.2 SEQUENCE GENERATOR OPERATIONS. The three categories of machine instructions are each handled differently in the sequence generator. They will be discussed separately. A machine instruction consists of one or more subinstructions. It takes 1 MCT to execute one subinstruction. A subinstruction is a part of the main instruction. For example, the CCS instruction is made up of two subinstructions, CCS0 and CCS1. Thus, it takes approximately 24 μ sec to execute the CCS instruction. Most of the basic instructions consist of either one or two subinstructions. A special subinstruction, STD2 (standard 2), is used to obtain the next instruction in the program and to update the program counter (Z register). This subinstruction is performed immediately after most subinstructions. It is not a part of the machine instructions listed in tables 14-6, 14-7 or 14-8. Each subinstruction is further divided into 12 action times. The execution of any subinstruction is caused by a set of control pulses generated at each action time. A control pulse is a 1 μ sec pulse occurring at a specific action time. Examples of control pulses are $\overline{\text{WXG}}$, $\overline{\text{RUG}}$, etc. By generating these control pulses at specific times, the AGC is able to control and direct the sequencing of data throughout its functional areas.

The sequence generator produces these control pulses upon receipt of an order code or signals from priority control indicating an involuntary instruction is to be performed. The basic timing pulses $\overline{\text{T01}}$ through $\overline{\text{T12}}$ are combined with these instruction requests. The result is the production of control pulses which define specific actions that are to be performed at specific action times in order to execute the subinstruction.

Another important function of the sequence generator involves the mechanization of branching functions or logic choices. The capacity of the AGC to alter its sequence of execution of events on the basis of previous knowledge is sometimes called a conditional jump. Testing for overflow or underflow and for sign are functions performed in this circuitry.

14.8.2.1 Regular Instruction Execution. Reference figure 14-42 during the following discussion. The control pulse, NISQ (next instruction sequence), is generated during a STD2 subinstruction. This signal indicates that the old instruction has been completed and a new one is requested. The SQ service block then clears the SQ register and issues a $\overline{\text{RB}}$ and a $\overline{\text{WSQ}}$ pulse. Bits 13, 14, 15 and 16 contain the order code at this time. This order code is read into the SQ register via the order code transfer gate. The transfer gate simply transfers during normal operation. The order code defines one of eleven regular instructions to be performed. The subinstruction code generator also produces a two-bit subinstruction code. This two-bit code will further define the subinstruction within the regular instruction. Table 14-9 lists all machine subinstructions along with their associated order codes and subinstruction codes. Notice that the CCS0 subinstruction is differentiated from the CCS1 subinstruction by the 00 and the 01 subinstruction code respectively. The subinstruction code is controlled by control pulses ST1 and ST2 which are internal control pulses. After the completion of CCS0, the ST1 control pulse would be routed internally from the crosspoint matrix back to the subinstruction code generator where and 01 would be produced and applied, along with the unchanged order code, to the instruction decoder. It is the function of the instruction decoder to logically develop subinstruction commands by combining order code and subinstruction code information. There is a subinstruction command for every subinstruction. These commands are routed to the crosspoint matrix where they are combined with timing pulses $\overline{\text{T01}}$ and $\overline{\text{T12}}$ to produce control pulses.

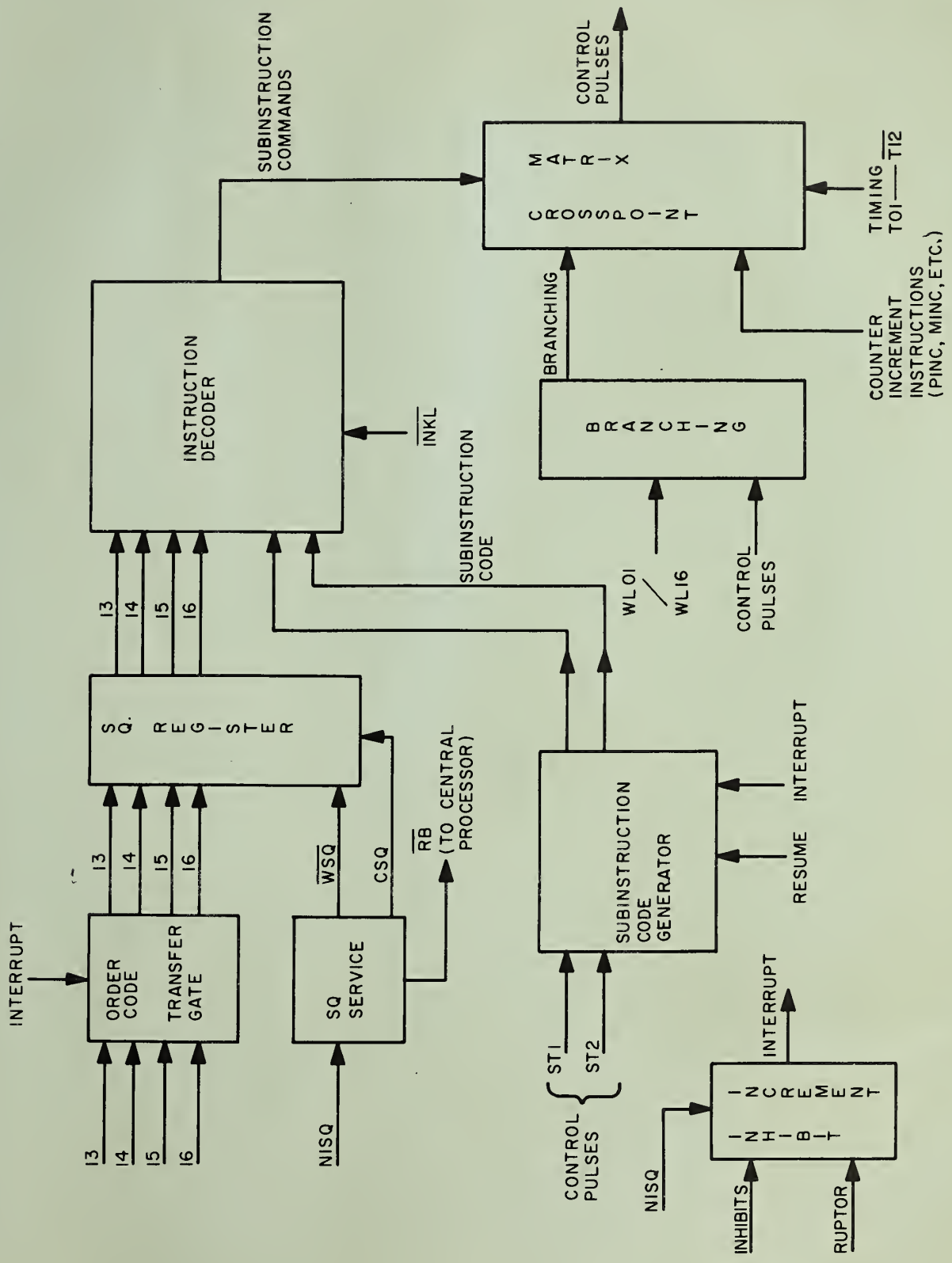


Figure 14-42. Sequence Generator Flow Diagram

Table 14-9. Sequence Generator Codes

Subinstruction Initials	Order Code				Subinstruction Code	
	16	15	14	13	MSD	LSD
STD2	X	X	X	X	1	0
TC0	0	0	0	0	0	0
XCH0	0	0	1	1	0	0
CS0	1	1	0	0	0	0
TS0	1	1	0	1	0	0
MSK0	1	1	1	1	0	0
AD0	1	1	1	0	0	0
NDX0	0	0	1	0	0	0
NDX1	0	0	1	0	0	1
CCS0	0	0	0	1	0	0
CCS1	0	0	0	1	0	1
SU0	1	0	1	1	0	0
MP0	1	0	0	1	0	0
MP1	1	0	0	1	0	1
MP3	1	0	0	1	1	1
DV0	1	0	1	0	0	0
DV1	1	0	1	0	0	1
RUPT1	0	0	1	1	0	1
RUPT3	0	0	1	1	1	1
RSM	0	0	1	0	1	1
PINC	X	X	X	X	X	X
MINC	X	X	X	X	X	X
SHINC	X	X	X	X	X	X
SHANC	X	X	X	X	X	X
GO	0	0	0	0	0	1
TCSA	0	0	0	0	1	1
OINC	X	X	X	X	X	X
LINC	X	X	X	X	X	X

X Indicates 0 or 1

Figure 14-43 is a hypothetical crosspoint matrix showing control pulses produced for only three subinstructions with only three action times envolved, T01 through T03. Remember, a subinstruction really takes 12 action times to be performed.

A chart included in figure 14-43 defines the specific control pulses issued at specific times for specific subinstructions. Gates 1, 2 and 3 consist of AND and OR circuits which will logically produce control pulses necessary to execute subinstructions ADO, DVO and TC. Since a given control pulse might be generated at different times but routed to the same place, OR circuits are necessary to combine like signals.

Assuming the ADO subinstruction command has been produced by the instruction decoder, the chart on figure 14-43 shows the following: at T01, control pulses $\overline{\text{RBG}}$ and $\overline{\text{WSG}}$ are generated; therefore, the content of register B is written into register S. At T02, control pulses $\overline{\text{RAG}}$ and $\overline{\text{WYG}}$ are generated; therefore, the content of register A is written into register Y. At time T03, the G register is cleared. The above mentioned control pulses cause the ADO subinstruction to be executed. In reality, the AGC uses many subinstructions and a wide variety of control pulses. Some of these pulses are used frequently and some are highly specialized and only used during a single subinstruction.

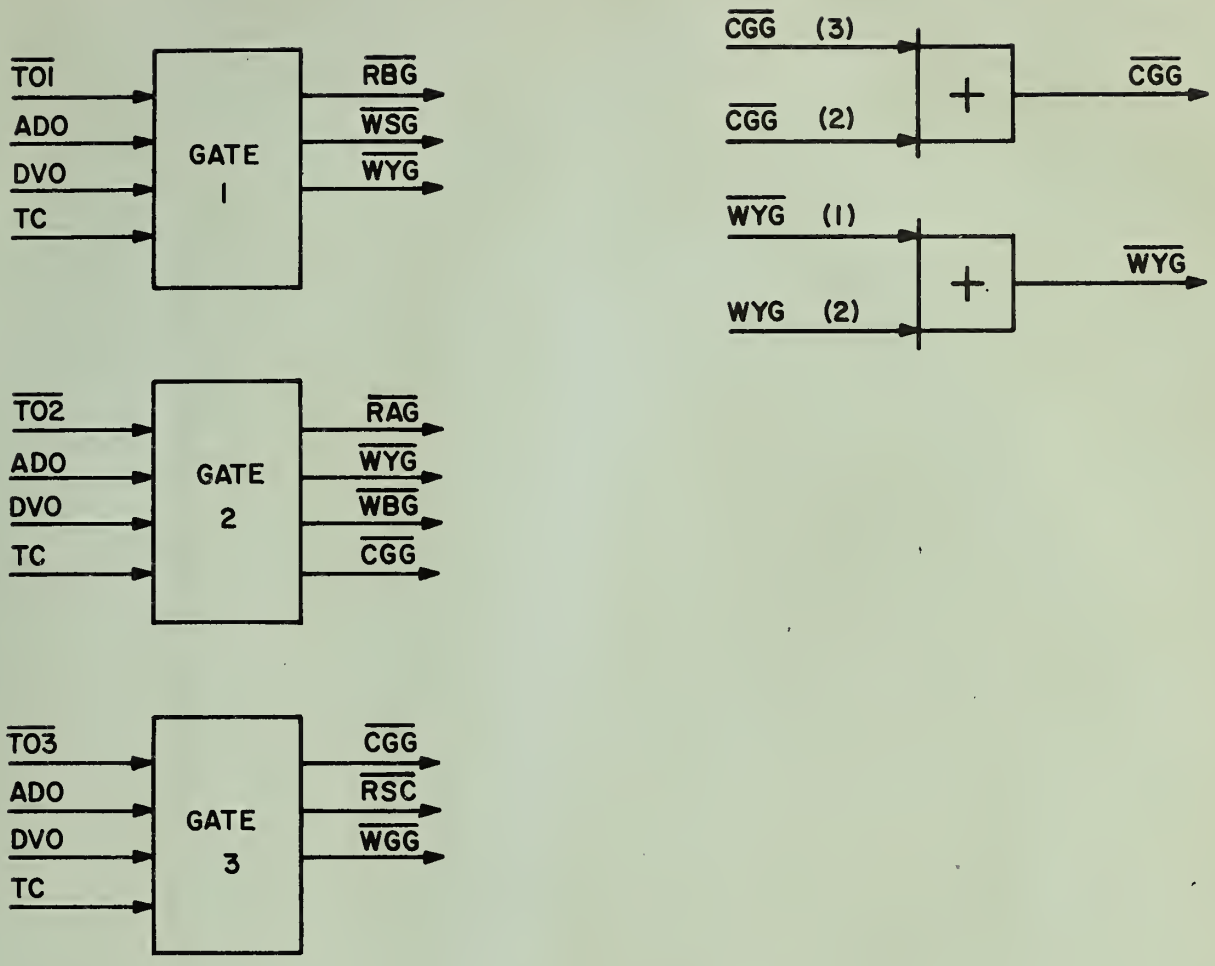
14.8.2.2 Involuntary Instruction Execution. There are two types of involuntary instructions: program priority instruction and counter instructions. They will be considered separately. The execution of these instructions is directed by the sequence generator in response to one of five interrupts or incrementing signal inputs. The instructions (except RSM) are not programmed. They are forced or hardware generated while normal operation of the sequence generator is inhibited.

14.8.2.2.1 Program Priority. The instruction RUPT will be executed when one of 5 interrupts occur. The sequence generator is notified of this occurrence via the inhibit interrupt block. The inhibit interrupts block is used to prevent an interruption of the AGC during a critical operation. Figure 14-44 indicates the conditions causing an inhibition of the interrupts. There are basically 3 causes:

a. Overflow-Underflow Detection. Underflow or overflow detection will occur in the branching block. It is necessary to store this excess in an erasable memory location to preserve the results of some central processor manipulation. This would take only one MCT after which the inhibit would be released and recognition of a possible interrupt would occur.

b. Programmed Inhibit. The programmer can purposely inhibit interrupts by programming an address of 0017_8. He may release this inhibit by programming 0016_8. These addresses are reserved exclusively for this purpose. The programmer therefore can prevent the possibility of the program being interrupted during some critical transfer routine.

c. Interrupt in Progress. It is impossible to interrupt an interrupting program until that program is completed. The completion of this program will be implemented with the instruction RSM (Resume) which must be programmed.



CONTROL PULSE CHART

SUB-INST	TOI	TO2	TO3
ADO	$\overline{RBG}$ $\overline{WSG}$	$\overline{RAG}$ $\overline{WYG}$	$\overline{CGG}$
DVO	$\overline{RBG}$ $\overline{WSG}$	$\overline{RAG}$ $\overline{WBG}$ $\overline{CGG}$	$\overline{RSC}$ $\overline{WGG}$
TC	$\overline{RBG}$ $\overline{WSG}$ $\overline{WYG}$		$\overline{CGG}$

Figure 14-43. Hypothetical Crosspoint Matrix

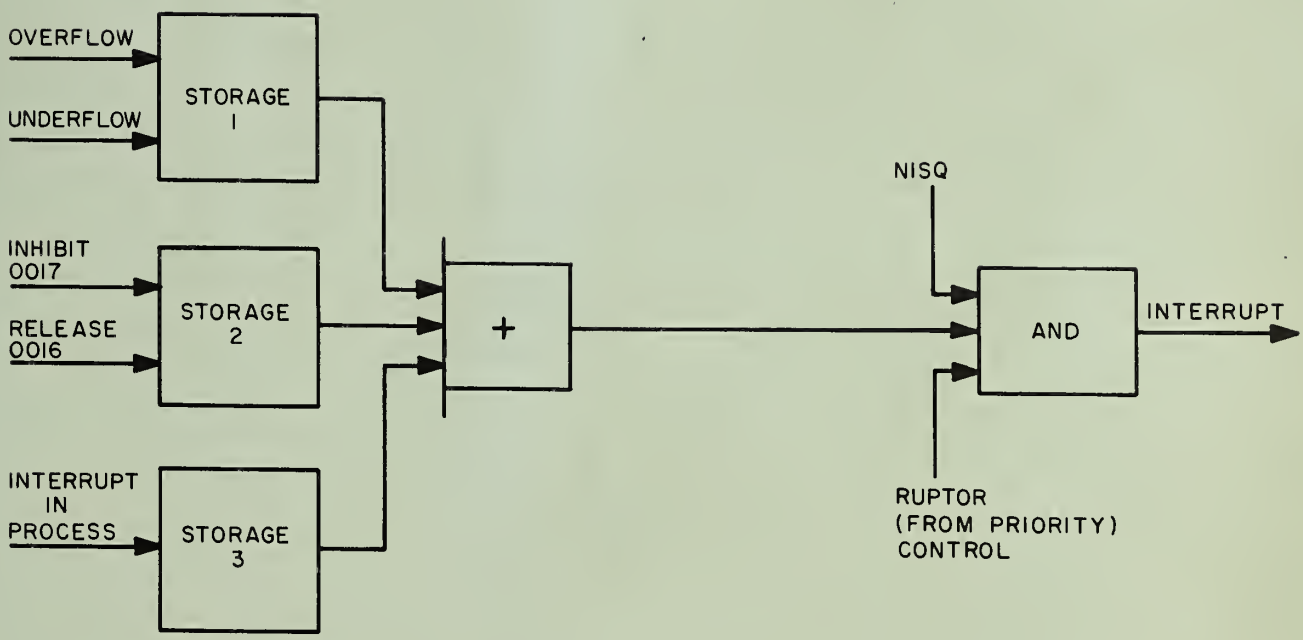


Figure 14-44. Inhibit Interrupt

An interrupt would be mechanized as follows: A RUPTOR signal from the priority control block would cause an INTERRUPT if there are not inhibits and if the previous entire instruction has been completed as indicated by the presence of the NISQ control pulse. The interrupt signal would force the generation of a specific order code and subinstruction code. These codes would then be transferred into the instruction decoder where the RUPT 1 subinstruction command is produced. Table 14-9 shows that the order code for the RUPT instruction is 0011. It requires 2 subinstructions to facilitate the transfer of the AGC into the specific interrupting program (KEYRUPT, ERRUPT, UPRUPT, etc.). An RSM instruction is required to terminate the interrupt. As pointed out, this is a programmed instruction whose order code is the same as the NDX order code. However, the subinstruction code will be different.

14.8.2.2.2 Counter Instructions. Counter instructions are executed by direct inputs from the priority block indicating an incrementing pulse has been received. These signals PINC, MINC, SHINC and SHANC will force the crosspoint matrix to produce directly the appropriate sets of control pulses. The priority control block also produces $\overline{\text{INKL}}$ which occurs any time a counter increment is requested. This signal completely inhibits the generation of subinstruction commands. The counter instructions may be executed at the end of any memory cycle time and cannot be inhibited as the interrupts can be. Table 14-9 shows that the order codes and subinstruction codes of the counter instructions are not significant any may be either 0 or 1. It takes only one MCT to update a counter.

14.8.2.3 Miscellaneous Instruction Execution. The OINC and LINC instructions are executed as counter instructions. The GO and TCSA instructions are executed in a manner similar to a program interrupt.

14.8.2.4 Branching. This block has the function of implementing the logic choices of the AGC. It is here that the computer will alter its future course on the basis of the results of a computation or logical process. For example, the comparing portion of the CCS instruction will be carried out here. The detection of underflow and overflow will be effected here also. Detection of the sign of a word is carried out here as part of the execution of several instructions. Figure 14-45 shows a breakout of the branching block. All branching requires control pulses for initiation. Shown is the test for sign with bit 16 incoming to be scrutinized if the appropriate control pulse is present. Test minus zero is a test for all 1's present in a particular word. These two tests are important parts of the CCS instruction execution. The underflow and overflow test blocks respond to a 10 or 01 on bits 16 and 15 respectively. The detection of underflow or overflow could cause an inhibit of interrupts while incrementing or decrementing the OVCTR (overflow counter) or it could cause the computer to branch into a different program. All of the test gates are routed to the branch flip-flops where two signals are produced and applied to the crosspoint matrix. Here, new sets of control pulses will be produced causing a new sequence of events to take place. The actual events that take place depend upon the subinstruction that is being executed at the time of testing or detection.

14.8.2.5 Instruction Flow. Figures 14-46 and 14-47 are flow charts of the TC0 and STD2 subinstructions. These figures detail information transfer in the AGC relative to action times.

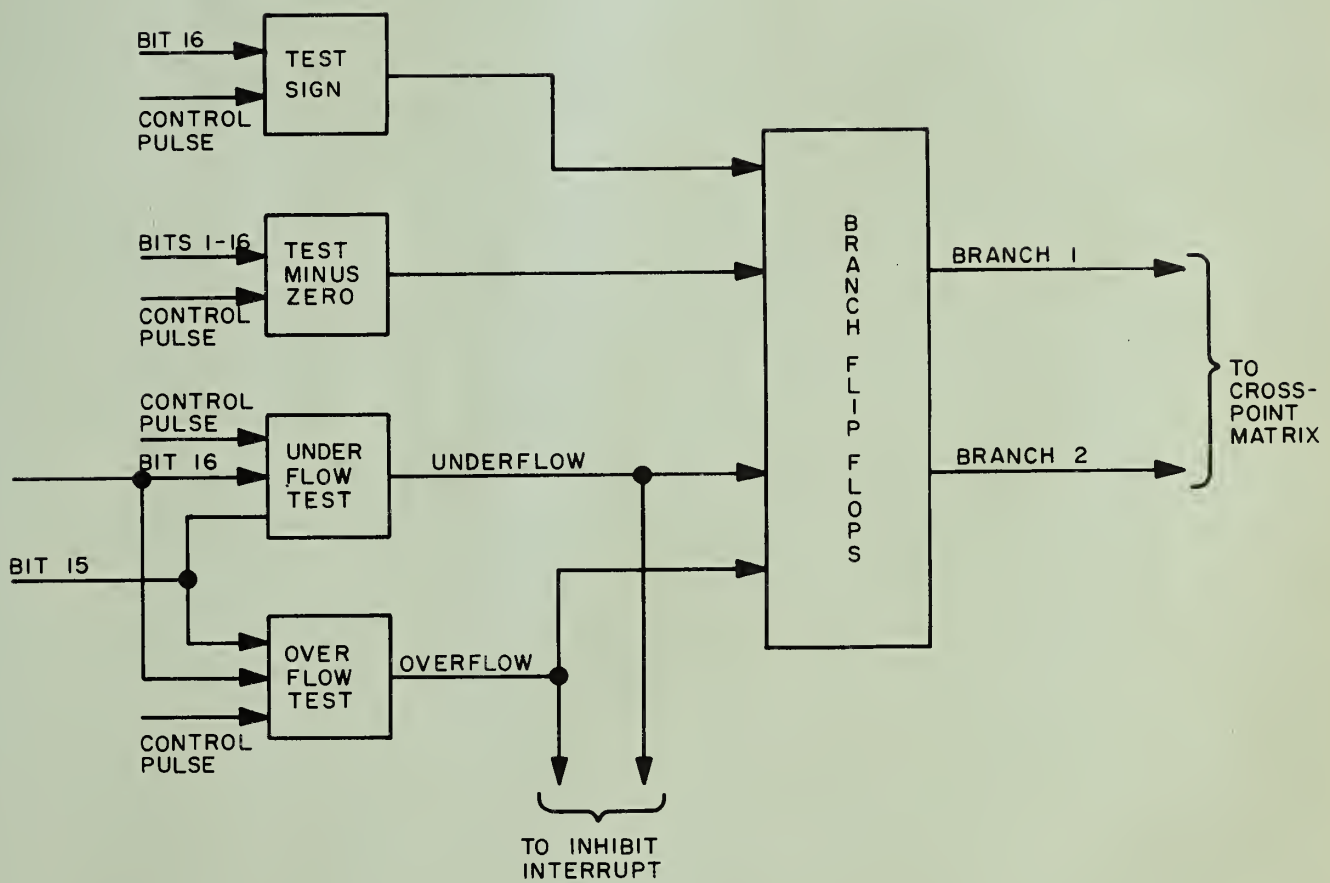


Figure 14-45. Branching

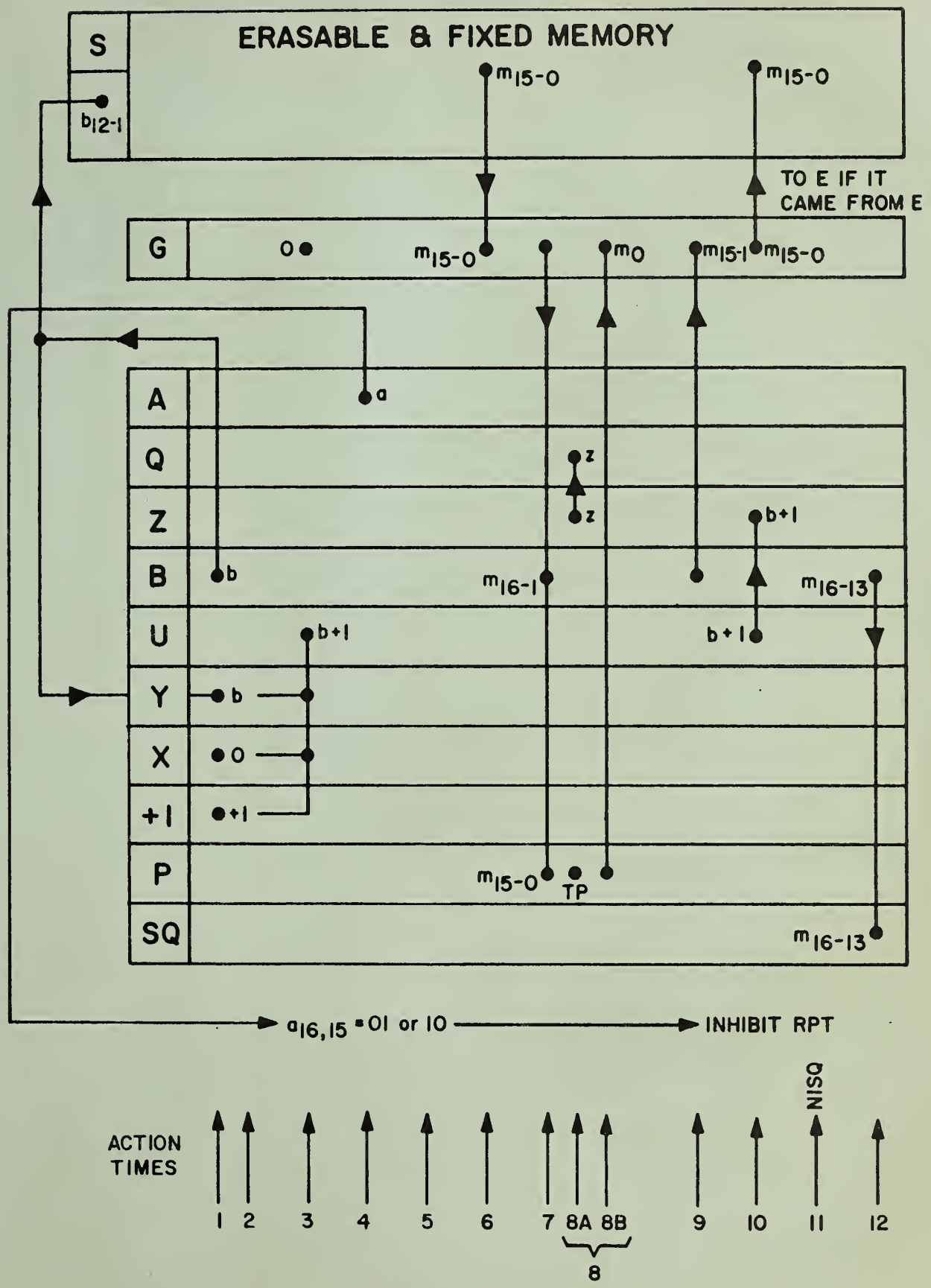


Figure 14-46. TC0

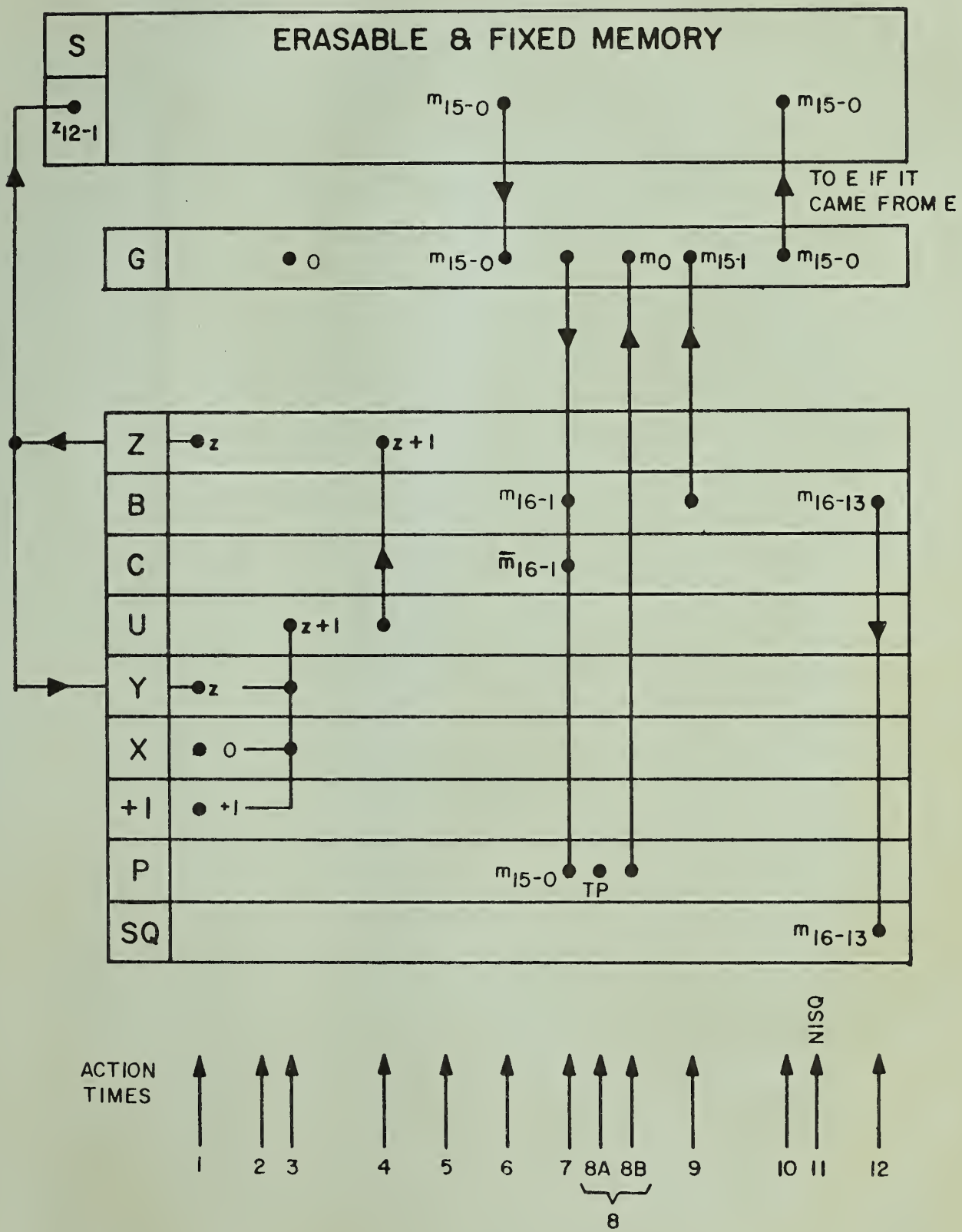


Figure 14-47. STD2

14.9 PRIORITY CONTROL

Priority control consists of counter priority control and interrupt priority control. The purpose of counter priority control is to update the counters in erasable memory. Counter priority control is also used during test functions to implement the display and load instruction requests provided by the computer test set. The purpose of program interrupt priority control is to transfer AGC control to one of six interrupt transfer subroutines stored in fixed memory.

14.9.1 COUNTER PRIORITY CONTROL. A counter is updated when counter priority control receives an incremental pulse for the given counter. Only one counter can be updated at a time. However, counter priority control may receive incremental pulses simultaneously for several counters. When incremental pulses for more than one counter are present, the counters are updated in a preassigned order. Counter priority control is designed to differentiate between incremental pulses pertaining to increment, decrement, shift, and shift-and-add-one counter instructions (involuntary instructions). When an incremental pulse is received, counter priority control produces the address of the counter to be updated and commands the sequence generator to execute the proper counter instructions.

During a test function, the computer test set produces display and load instruction requests. When a display or load instruction request is received, the counter priority control commands the sequence generator to execute the display or load instruction. The display instruction is used to read the contents of fixed and erasable memory. The load instruction is used to enter data into erasable memory.

Counter interrupts are listed in table 14-10. They provide the AGC with incremental or digital data. This data consists of changes in velocity, changes in time, changes in gimbal and optical unit angular positions and drive pulses developed by the AGC and Uplink Telemetry inputs. At the present time, according to the hardware configuration, 20 input counters are implemented in erasable memory through the counter interrupt priority control circuitry.

According to the present program, only 16 of the 20 counters are now in use. About half of these counters provide for parameters generated internal to the AGC. The other counters provide for input parameters generated external to the AGC. Any one of these parameters can occur at any time and two or more of the parameters can occur simultaneously. Because of this, the counter priority control circuitry (1) provides a priority assignment for the inputs so that a logical processing order is established when one or more inputs require simultaneous processing and (2) stores all inputs until the AGC is ready to process them.

In addition to these two functions, the counter priority control circuitry develops (3) the address of the memory counter associated with the particular input being processed and (4) control signals which are sent to the sequence generator so that the proper processing is performed. The control signals are PINC, MINC, SHINC, SHANC and an inhibit signal $\overline{\text{INKL}}$. $\overline{\text{INKL}}$ inhibits the generation of control pulses defined by the order code held in the SQ register while the control pulses for the counter instructions are generated.

Table 14-10. Counter Interrupts

Priority	Memory Register	Name	Sources	Use
1	0034	OV CTR	AGC	Overflow-underflow counter
2	0036	TIME 2	Time 1 overflow, AGC	Most significant time word
3	0035	TIME 1	100 CPS, AGC	Least significant time word
4	0037	TIME 3	100 CPS, AGC	Time counter for program initiation
5	0040	TIME 4	100 CPS, AGC	Time counter for input/output program
6	0041	UPLINK	Communications system	Data input to AGC from ground
7	0042	OUT CTR 1	AGC output circuits	Pulse counter for pulsing IRIG's or inertial CDU's
8	0043	OUT CTR 2	AGC output circuits	Pulse counter for pulsing optical CDU's
9	0044	PIPA X	ISS PIPA X	Counts ΔV pulses from X PIPA
10	0045	PIPA Y	ISS PIPA Y	Counts ΔV pulses from Y PIPA
11	0046	PIPA Z	ISS PIPA Z	Counts ΔV pulses from Z PIPA
12	0047	ICDU X	Inertial CDU X	Counts $\Delta\theta$ pulses from outer gimbal CDU
13	0050	ICDU Y	Inertial CDU Y	Counts $\Delta\theta$ pulses from inner gimbal CDU
14	0051	ICDU Z	Inertial CDU Z	Counts $\Delta\theta$ pulses from middle gimbal CDU
15	0052	OCDU X	Optical CDU X	Counts $\Delta\theta$ pulses from optics shaft CDU
16	0053	OCDU Y	Optical CDU Y	Counts $\Delta\theta$ pulses from optics trunnion CDU
17	0054	NOT IN USE AT THIS TIME		
18	0055			
19	0056			
20	0057			

Note: The lower the priority number, the higher the priority.

Figure 14-48 is a block diagram of the counter interrupt priority control circuitry. In this diagram, the inputs are divided into three groups. Group 1 inputs cause a PINC instruction. Group 2 inputs cause a PINC or MINC instruction. Group 3 inputs cause a SHINC or SHANC instruction. All of the counter interrupt parameters of these groups input to a circuitry block called the priority chain. Included in this block are flip-flops for the storage of the input pulses and the circuitry which establishes the various input priorities. When a higher priority flip-flop is set, indicating that processing is required for a particular input, the outputs from all lower priority flip-flops which may be set are inhibited. This allows the request for a particular counter instruction and the address of the appropriate memory counter to be generated. The address generated during the processing of a counter interrupt is also used to reset the appropriate flip-flop in the priority chain.

Another signal, $\overline{\text{CTROR}}$ (COUNTER OR), is developed which results in the signal $\overline{\text{INKL}}$. $\overline{\text{INKL}}$ is also developed by the request for an OINC or LINC instruction. These two instructions are results of inputs from the Computer Test Set and enable the loading or display of a specified memory register.

The overall flow of information which occurs during the processing of a counter interrupt input is shown in figure 14-49. In this diagram, it is assumed that a PIPA X input is being processed which could be either a + or - pulse and result in either a PINC or MINC instruction. These instructions require one MCT to execute. Execution can be initiated at the end of any MCT. Circuitry is utilized which does not contain useful information from the program controlled processing in program at the time the execution of the counter interrupt instruction was initiated.

When a + or - PIPA X pulse occurs, it is set into the appropriate flip-flop in the counter priority control circuits. Assuming that this is the highest priority counter interrupt input that requires servicing at the end of the MCT during which it occurred, the appropriate instruction signal, PINC or MINC, the signal $\overline{\text{INKL}}$ and the six bit address (0044 for X PIPA) are generated. During the next MCT, the sequence generator develops the control pulses for the PINC or MINC instruction. These instructions cause the six bit address referencing the proper counter in erasable memory to be set into the S register through the write amplifiers. Still under control of the PINC or MINC control pulses, the content of the specified counter is read from the erasable memory using the address contained in the S register. The content of the counter is set into the adder circuitry of the AGC where a binary 1 is added to or subtracted from it. When this updating process is complete, the updated content of the counter is stored back into the specified memory counter using the address held in the S register. Having read, updated and written the content of the specified counter back into the memory, the address held in the S register is used to reset the flip-flop in the counter priority control circuitry which requested the servicing. This completes the servicing of the PIPA X input which required one MCT or 12 μ sec to perform.

All of the counter interrupt inputs are processed in essentially the same manner as the PIPA X input. Later in this section of the study guide, the use of some of the other counter interrupt inputs and parameters will be presented. They are used in implementing other functions involving the AGC's interface functions.

14.9.2 INTERRUPT PRIORITY CONTROL. Program interrupts cause the suspension of the processing of a particular program and cause a particular routine to be executed. The execution of the routine (one of six) depends upon which input to the program interrupt priority control circuitry requires servicing.

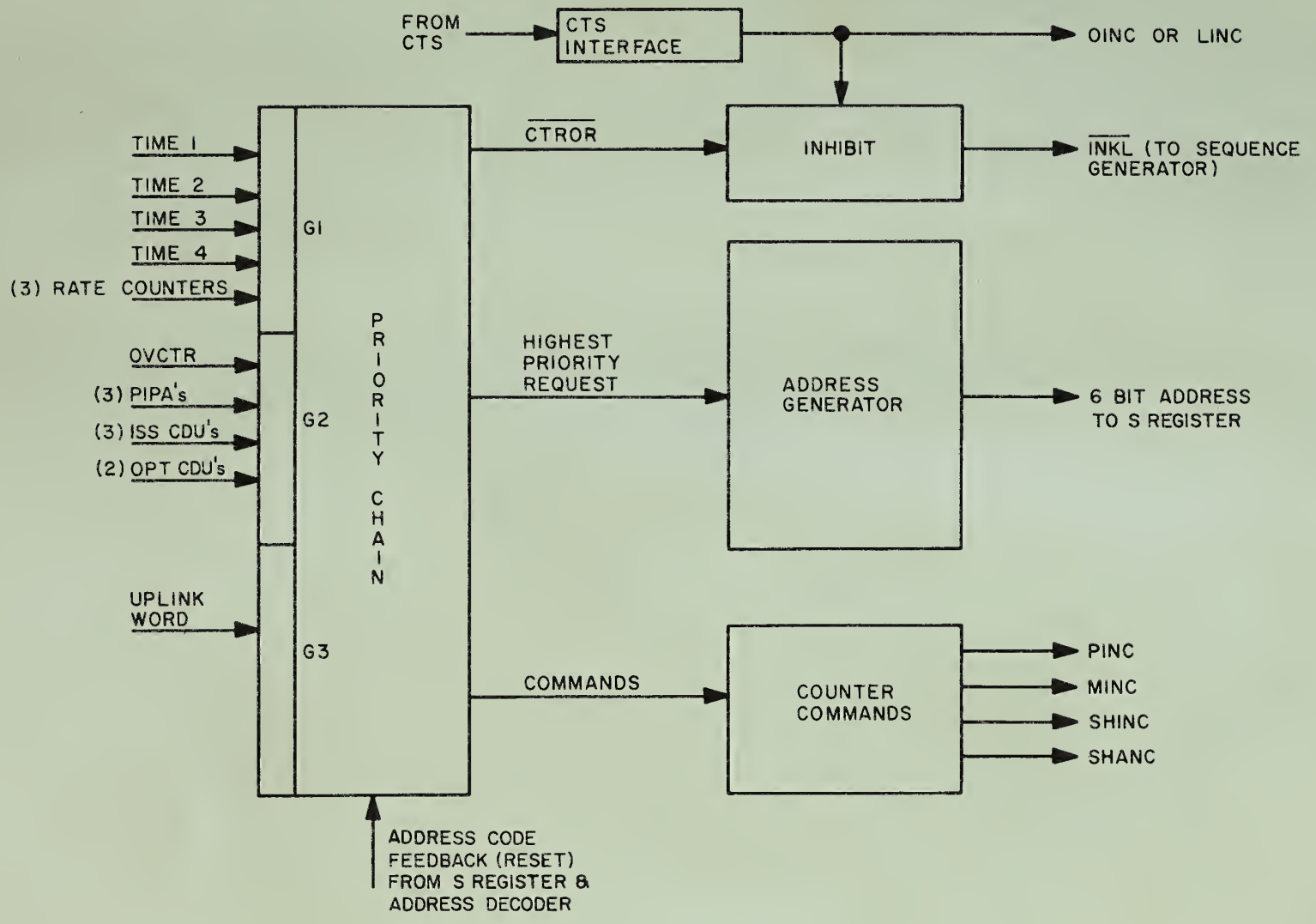


Figure 14-48. Counter Priority Control

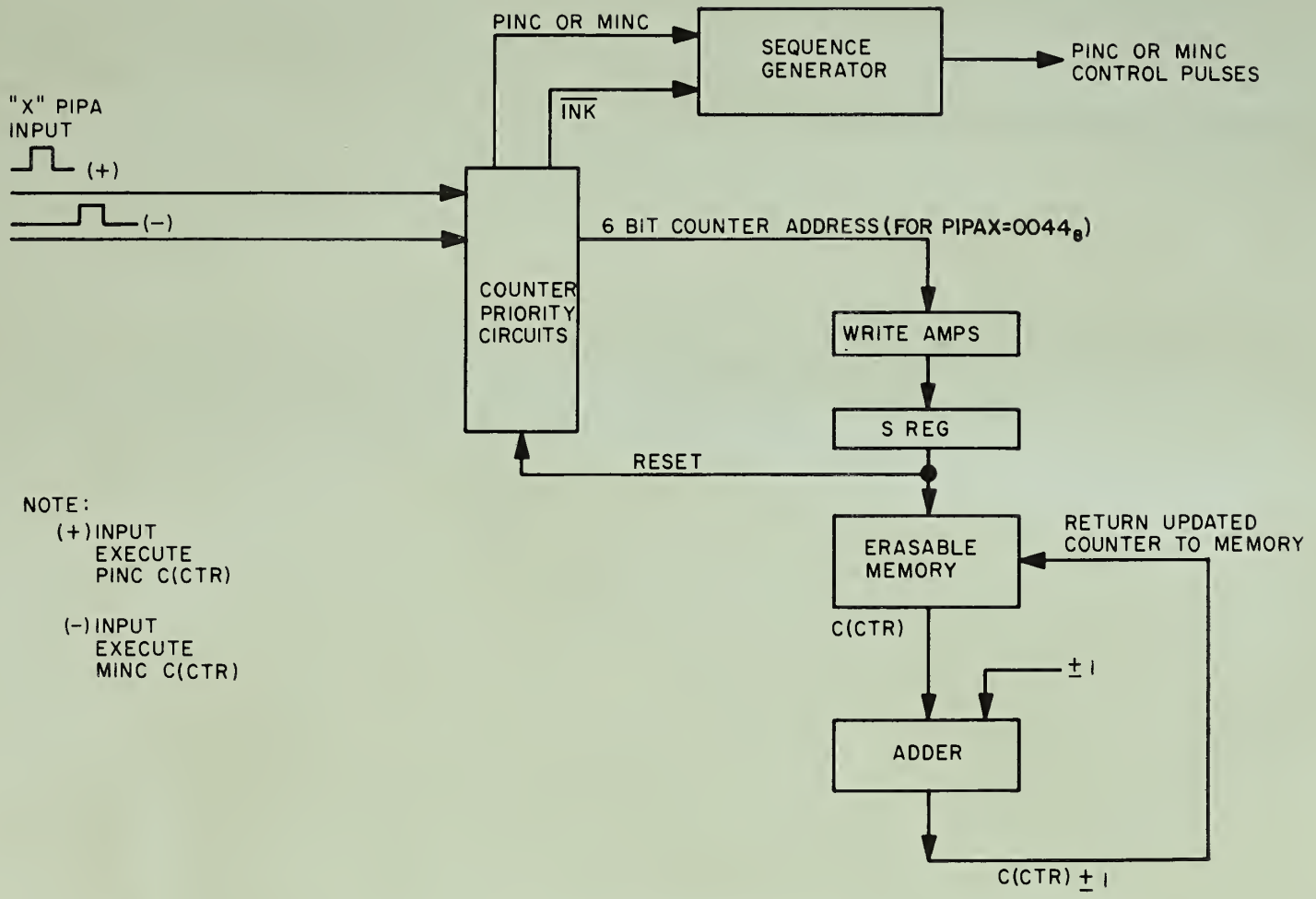


Figure 14-49. Counter Input Interface Flow Diagram

The signals used to request the execution of the T3RUPT, T4RUPT, UPRUPT and DNRUPT routines are of a short duration $\approx 1\,\mu$ sec. However, the requests for the KEYRUPT (resulting from a keyboard input, MARK or MARK REJECT) and the request for RUPT 2 are of longer duration. If these long duration signals were used directly to request the processing of an interrupt routine, the request for the routine would still be present when the routine had been processed. This would cause the routine to be processed again. This is not a desirable condition; consequently, "trap" circuits are used to condition these inputs. The trap circuitry enables only one $1\,\mu$ sec pulse to be developed per input request. A reset signal is required to reset the trap circuitry before another request pulse can be developed. In the case of the keyboard or MARK trap, the releasing of the keyboard key or MARK or MARK REJECT key generates the required reset signals. The reset signal for the RUPT 2 trap is provided by bit position of the OUT 1 register.

Table 14-11 lists the program interrupts, their priorities and their use. Figure 14-50 is a block diagram of the program interrup priority control. In this figure, the request signals for the program interrupts are routed to request flip-flops. The outputs of the flip-flops are interconnected in a manner such that if a higher priority request is present, the outputs of all lower priority request flip-flops are inhibited. Whenever the request for the execution of an interrupt routine is honored, the starting address of the routine is generated and a signal RUPTOR is routed to the sequence generator. The honoring of an interrupt request is enabled at the end of the last MCT of an instruction.

When the request for a program interrupt is honored, signal RUPTOR forces the order code for the RUPT instruction into the SQ register causing this instruction to be executed. This instruction enables the contents of the Z and B registers to be stored in the erasable memory and, using the generated address, forces control to the starting point of the appropriate interrupt routine. At the beginning of the interrupt routines, the contents of the A and Q registers are stored in the erasable memory. By storing the contents of the B, Z, A and Q registers, the next instruction, the next-next instruction's address, the data being operated on and the return address of the interrupted program are stored. These quantities are restored in the central processor registers prior to returning control back to the interrupted program when the execution of the interrupt routine is completed.

14.9.2.1 T3RUPT Routine. The T3RUPT routine is initiated by the overflow of the TIME 3 counter. This counter, which is incremented every 10 ms through counter interrupt action, is used to time the initiation of a processing function. The counter is set to overflow minus the time delay required. When the desired time has elapsed, the TIME 3 counter will overflow and initiate the execution of the T3RUPT routine. The T3RUPT routine then routes control to the specified processing function to be performed at this time. When completed, control is returned to the T3RUPT routine which returns control to the interrupted program. The T3RUPT routine is the highest priority program interrupt.

14.9.2.2 RUPT 2. RUPT 2 is a spare program interrupt at the present time. It will be incorporated to provide the processing for sequencing signals generated by the Saturn guidance system and spacecraft systems. The signals which will be handled by this interrupt are:

a. Guidance Release

b. Saturn Ullage

c. S-4B Separate

d. CM/SM Separate.

Table 14-11. Program Interrupts

Priority	Start Address	Name	Source	Use
1	2000	T3RUPT	Overflow of time 3 counter	Time schedule programs to be processed
2	2004	RUPT 2	SIVB instrumentation unit inputs of Saturn ullage, guidance release, & SIVB separate, and mission sequencer input of CM/SM separate	Initiation of processing required by these sequencing inputs (not included in Sunrise 69).
3	2010	T4RUPT	Overflow of time 4 counter	Time schedule an input/ output control program
4	2014	KEYRUPT	DSKY keyboard or MARK or MARK REJECT push-button	Process keyboard input from DSKY or record necessary data for mark
5	2020	UPRUPT	Whenever a complete word is parallelized in the uplink counter	Process the coded information injected into the AGC via the uplink input
6	2024	DNRUPT	Telemetry end pulse from telemetry programmer of the communications and instrumentation system	Loads an AGC word to be sent via downlink during next transmission time

Note: The lower the priority number, the higher the priority.

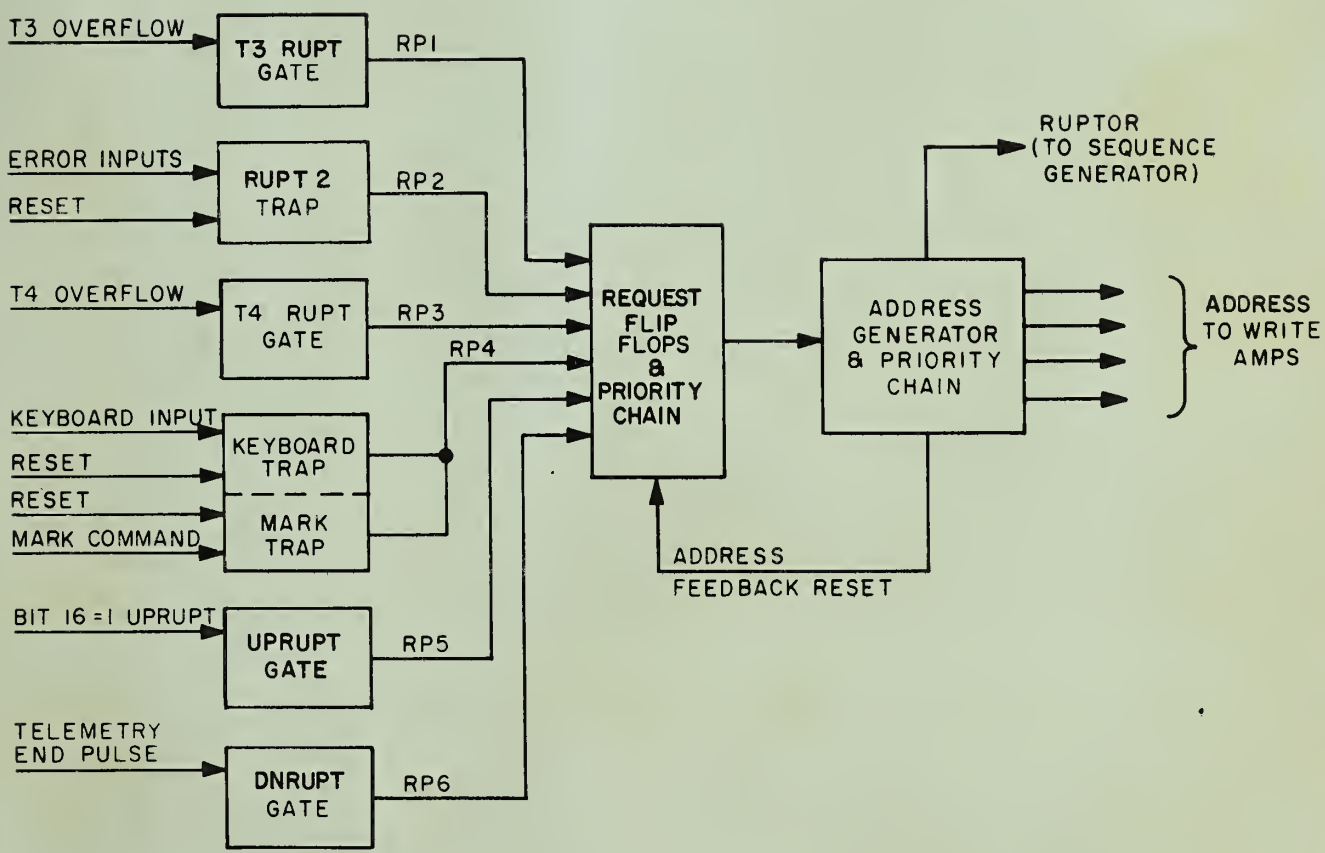


Figure 14-50. Program Interrupt Priority Control

14.9.2.3 T4RUPT Routine. The execution of the T4RUPT routine is initiated whenever the TIME 4 counter overflows. Normally, the TIME 4 counter is set to overflow in 60 ms. The time counter is incremented every 10 ms through counter interrupt action.

The T4RUPT routine provides the following interface functions:

a. Positioning of the stable member by driving the ISS CDU's

b. Positioning of the optical unit by driving the OSS CDU's

c. Sampling and verifying the ISS and OSS modes

d. Driving the relays of the DSKY's to provide for information display, ISS and OSS mode commands and condition indications

e. Processing of the PIPA, IMU and CDU fail inputs to the AGC

f. Performing checks on the downlink telemetry word rate

14.9.2.4 KEYRUPT Routine. The KEYRUPT routine is initiated whenever a key of the DSKY keyboards, the MARK pushbutton or the MARK REJECT pushbutton is depressed. The KEYRUPT routine provides for accepting the key code input and initiating the processing of the key code if the execution of the routine was initiated as a result of a keyboard input. If the execution is initiated as a result of a MARK or MARK REJECT, the MARK data (time, gimbal angles and optical angles) are recorded or rejected.

14.9.2.5 UPRUPT Routine. The UPRUPT routine is initiated whenever a binary 1 is shifted into bit 16 of the uplink counter through counter interrupt action. The uplink provides a serial to parallel conversion of information sent to the AGC over this data link. The information sent uplink is in the form of keycodes and the UPRUPT routine performs essentially the same function as the KEYRUPT for keyboard inputs. The UPRUPT routine accepts the uplink word, checks the validity of the transmission and initiates the processing of the keycode input.

14.9.2.6 DNRUPT Routine. The DNRUPT routine is initiated by the TELEND sync pulse from the downlink telemetry programmer. This pulse occurs either 10 or 50 times per second and therefore, the DNRUPT routine is executed at these rates. The DNRUPT routine selects the appropriate AGC word to be transmitted downlink and loads it into the OUT 4 register. From this register the information is gated in a serial manner for transmission to the ground station.

14.10 INPUT-OUTPUT

In addition to the counter interrupt and the program interrupts previously discussed, the AGC has a number of other inputs derived from its interfacing hardware. These inputs are a result of the functioning of the hardware or an action by the operator of the spacecraft. The counter interrupts in most cases enable the AGC to process inputs representative of data parameters such as changes in velocity. The program interrupt inputs to the AGC are used to initiate processing of functions which must be processed a relatively short time after a particular function is present. The other inputs to the AGC, in general, enable the AGC to be cognizant of "conditions" which exist in its environment. These inputs are routed to, and are available to the AGC's programs through the AGC's input registers.

Input registers IN 0, IN 2 and IN 3 are connected to the input interface circuits and loaded directly without program control. Their function is to store discrete signals from the G&N and other spacecraft systems. These signals include system alarms, moding signals, keyboard inputs, etc. Register IN 1 is used in conjunction with scaler B to accumulate real time during standby operation. Output registers OUT 0, OUT 1 and OUT 2 are connected to the output interface circuits and can be loaded by addressing under program control. OUT 0 is used for output displays sent to the DSKY. OUT 4 is connected to the telemetry (downlink) circuits and is controlled to perform at parallel-to-serial conversion.

The outputs of the AGC fall in one of the following categories: (1) data, (2) control, (3) condition indications. Some of these outputs are controllable through the AGC's program while others are present as a function of the AGC circuitry. All of the outputs which are controlled by the AGC's programs are developed through the AGC's output registers.

14.10.1 THE AGC'S INPUT REGISTERS. The AGC, at the present time, utilizes four input registers. The inputs to these registers enable the AGC, through its programs, to remain cognizant of conditions which exist in its environment. These inputs are derived from the three subsystems of the G&N System, the Stabilization and Control System, the mission sequencer, and the SIV-B instrumentation unit.

14.10.1.1 IN 0 Register. The utilization of the digit positions of the IN 0 Register is shown in figure 14-51. Of the possible 15 usable digits of this register, digit positions 14, 10, 9 and 8 are spares at this time. The usuage of the remaining digit positions is as follows:

Bit 15 - MARK - A binary 1 is placed in this digit position whenever the MARK or MARK REJECT pushbuttons are depressed. This indication is used by the KEYBRUPT routine to determine if the interrupt was caused by a MARK - MARK REJECT or by an input from a DSKY keyboard. Definition between a MARK and a MARK REJECT is accomplished by inspecting bit 12 of IN 3 Register, ZERO OPTICS. If this bit is a binary 1, the KEYRUPT routine was initiated by the MARK REJECT pushbutton. If bit 12 of IN 3 is a binary 0, the interrupt was caused by the MARK pushbutton.

Bits 13, 12 and 11 - G&N ENTRY MODE, G&N ΔV MODE and G&N ATTITUDE CONTROL MODE. These three inputs originate in the Stabilization Control System's mode control circuitry. They enable the G&N System to initiate these three modes as indicated by the SCS mode control panel.

Bit 7 - INHIBIT UPSYNC - A binary 1 is inserted into this bit position if the UPLINK telemetry bit rate exceeds 1600 bits per second. When this occurs, processing of the inputs from the Communications and Instrumentation System to the AGC carrying UPLINK information are not processed because too much computer time could be spent in processing this data. The bit rate detecting circuitry is part of the AGC.

Bit 6 - BLOCK UPLINK - A binary 1 is inserted into this bit position if the UPTL switch of the Main Panel DSKY is in the "BLOCK" position. This inhibits the processing of the inputs to the AGC from the Communications and Instrumentation System carrying UPLINK data.

BIT	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
IN "0" REGISTER		MARK	S.P. N.C.	G/N ENTRY MODE	G/N ΔV MODE	G/N ATT. CONT. MODE	S.P. N.C.	S.P. N.C.	S.P. N.C.	INHIBIT UPSYNC.	BLOCK UPLINK	KEY CODE 5	KEY CODE 4	KEY CODE 3	KEY CODE 2	KEY CODE 1

Figure 14-51. IN 0 Register Bit Assignments

Bit 5, 4, 3, 2 and 1 - This five bit code is formed by the depression of a key on one of the DSKY's. Whenever any of the keys on the DSKY's are depressed (except for the TEST ALARM key) a unique five bit code unique for the particular key is inserted into these bit positions. The AGC's KEYRUPT routine, also developed whenever a key is depressed, reads the code from the IN 0 Register and initiates the processing of the keycode input.

14.10.1.2 IN 1 Register. Whenever the AGC is placed in the STANDBY mode of operation, the only portion of the AGC which is operating is the timing circuitry. Therefore, the AGC cannot maintain its real time reference through its normal means by using the TIME 1 and TIME 2 counters. To enable the AGC to maintain its real time reference, even though it cannot use these time counters, the output of Scaler B of the AGC's timing circuitry forms the IN 1 Register. The output of the IN 1 Register is then used as a real time reference capable of counting up to approximately 23.3 hours in increments of 1.28 seconds (figure 14-5).

Two routines are required to enable the maintenance of the AGC's real time reference. One routine reads and stores the configuration of the IN 1 Register and the contents of the TIME 1 and TIME 2 counters prior to placing the AGC in the STANDBY mode. The other routine reads the configuration of the IN 1 register immediately after the AGC is put in the ON mode after leaving the STANDBY mode. It then uses this value of time and the value of time from IN 1 Register stored prior to entering the STANDBY mode to calculate the time the AGC was in the STANDBY mode. It then adds the time the AGC was in STANDBY to the stored contents of TIME 1 and TIME 2 counters after which the TIME 1 and TIME 2 counters are set to the updated time words as calculated above. In this manner, the AGC can maintain a real time reference to within approximately one second of time with the AGC in the STANDBY mode up to 23.3 hours. Note; the SUNRISE 69 program does not contain these required routines. They will be included in future programs.

14.10.1.3 IN 2 Register. The utilization of the digit positions of IN 2 Register of the AGC are as follows (figure 14-52).

Bit 15 - PARITY FAIL - This input is derived from the AGC's parity checking circuitry. Whenever a word is transferred from the AGC's memory and the parity is not odd, a binary 1 is inserted into this digit position.

Bits 14 and 13 - G&N MONITOR MODE and SCS ΔV MODE - These inputs originate in the SCS mode control circuitry and indicate to the AGC which program it should be processing.

Bits 12, 11 and 10 - IMU FAIL, PIPA FAIL and CDU FAIL - These three inputs, generated in the Inertial Subsystem of the G&N System, indicate that a failure has been detected in the stabilization loops, PIPA loops or the CDU loops.

Bit 9 - SM/CM Separation - This input is generated in the mission sequencer and indicates when the SERVICE MODULE and COMMAND MODULE have separated.

Bits 8, 7, 6 and 5 - SIV-B SEPARATION, SATURN ULLAGE, GUIDANCE RELEASE and LIFT OFF - These inputs are generated in the SIV-B Instrumentation Unit. They indicate to the AGC that the described actions have occurred or have been commanded to occur.

BIT	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
IN "2" REGISTER		PARITY FAIL	G/N MOD. MODE	SCS ΔV MODE	IMU FAIL	PIPA FAIL	CDU FAIL	CM/SM SEP.	SIVB SEP.	SATURN ULL.	GUID. REL.	LIFT OFF	← FINE TIME →			
													200PPS	400PPS	800PPS	1600PPS

Figure 14-52. IN 2 Register Bit Assignments

Bits 4, 3, 2 and 1 - 200 pps, 400 pps, 800 pps and 1600 pps - These inputs are generated by Scaler A. The four inputs of 200, 400, 800 and 1600 pulses per second form an extension of the TIME 1 and TIME 2 counters. By using these four digit bits, a granularity of the AGC's real time reference of 0.625 m-sec. is obtained. This four section of IN 2 Register is called FINE TIME and is used by programs which require a time reference with this granularity.

14.10.1.4 IN 3 Register. The IN 3 Register is used to inform the AGC programs of the Inertial and Optical Subsystem modes. At the present time, digit positions 13, 9 and 8 are spares. The remaining digit positions are used as follows (figure 14-53).

Bit 15 - OR of C1 - C33 - This input is the logical OR of the C relays contained in the DSKY's. If any one or more of the C relays are in the set state, a 1 is present in this digit position.

Bit 14 - COMPUTER CONTROL OPT - This input is a binary 1 whenever the optics function switch is in COMPUTER position. When this switch is in the COMPUTER position, the AGC is capable of positioning the optics and commanding optical modes.

Bit 12 - ZERO OPTICS - This input, when it is a binary 1, indicates that the optical unit is zeroing. When this digit position and bit 15 of the IN 0 Register are both binary 1's, the MARK REJECT pushbutton has been depressed.

Bit 11 - STAR PRESENCE - This input indicates that the star tracker has the optical unit locked on a star when it is a binary 1.

Bit 10 - TRACKER ON - A binary 1 present in this digit position indicates that the star tracker power switch is in the ON position.

Bit 7 - K5 ENTRY - This input will be a binary 1 any time the K5 relay of the Inertial Subsystem is in the set state. It indicates to the AGC that the ISS is in the ENTRY mode.

Bit 6 - TRANSFER SWITCH - The input to this digit position is a binary 1 whenever the Transfer Switch is in the COMPUTER position. This enables the AGC to control the moding and positioning of the Inertial Subsystem and the positioning of the stable member.

Bit 5 - K12 - This input will be a binary 1 whenever Relay K12 of the ISS is in the set state. It indicates that the ISS is in the ATTITUDE CONTROL mode.

Bit 4 - K4 - This input will be a binary 1 whenever Relay K4 of the ISS is in the set state. It indicates the ISS is in the FINE ALIGN mode. It is also a binary 1 when the ZERO ENCODER mode is used.

Bit 3 - K3 - This input will be a binary 1 whenever Relay K3 of the ISS is in the set state. It indicates that the ISS is in the MANUAL CDU mode.

Bit 2 - K2 - This input will be a binary 1 whenever Relay K2 of the ISS is in the set state. It indicates that the ISS is in the COARSE ALIGN mode.

Bit 1 -K1 - This input will be a binary 1 whenever Relay K1 of the ISS is in the set state. This indicates to the AGC that the ISS is in the ZERO ENCODER MODE.

BIT	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
IN "3" REGISTER		OR OF C1 - C33	COMP. CONTR. OPT.	S.P. N.C.	ZERO OPT.	STAR PRES.	TRKR. ON	S.P. N.C.	S.P. N.C.	K5 ENTRY	TRN. SW	K12 ATT. CONTR.	K4 FINE ALIGN	K3 MANUAL CDU	K2 COARSE ALIGN	K1 ZERO ENCODER

Figure 14-53. IN 3 Register Bit Assignments

14.10.2 THE AGC'S OUTPUT REGISTERS. The AGC, at the present time, utilizes four registers to develop its program controlled outputs. Through these registers, the AGC is capable of displaying information/requests to the astronaut, controlling the modes of operation of the ISS and OSS, and performing various functions associated with other spacecraft systems.

14.10.2.1 OUT 0 Register. The OUT 0 Register is used to transmit information to the NAVIGATION and MAIN PANEL DSKY's (figure 14-54). The information transmitted to the DSKY's is used to set up the display portion of the DSKY's, to control the moding of the ISS and OSS, to control condition indicators and to develop signals to the SCS.

Digit positions 15 through 12 are used to form a four bit code. Depending on the configuration of the code, one of 14 banks of relays will be selected in the DSKY's. Each bank contains 11 bistable relays which are used to perform the functions mentioned above. Therefore, the four bit code formed by digits 15 through 12 selects or enables 11 relays in each of the DSKY's.

The remaining digits of OUT 0 Register, digits 11 through 1, control the set and reset states of the 11 relays selected by the four digit code. Each of the 11 digit positions in the OUT 0 Register controls one of the 11 selected relays. The AGC words used to control these relays in the DSKY's through the OUT 0 Register are called RELAY WORDS.

Whenever the AGC desires to set or reset a relay or a group of relays in the DSKY's, it places the appropriate configuration of binary digits into the OUT 0 register. After 20 m-sec., the register is reset to zero. This allows enough time for the relays to establish one of their two states, but keeps the power consumption and heat build-up to a minimum.

The 154 relays contained in each DSKY and controlled by the OUT 0 Register are divided into two groups. One group from each DSKY consists of 121 relays and controls the information displayed on the DSKY's PROGRAM, NOUN VERB, R1, R2 and R3 display panels. The UPLINK ACTIVITY indicator panel and the flashing of the VERB and NOUN display panels are also controlled by relays in this group. The relays in this group are called "R" relays.

The other group of relays consists of 33 relays in each DSKY. These relays (1) control the moding of the ISS and OSS G&N System condition indicators and (2) control signals for use in other S/C systems. These relays are referred to as "C" relays.

14.10.2.2 OUT 1 Register. The usage of the digit positions of the OUT 1 Register is shown in figure 14-55. Digit positions 15, 14, 12, 11, 8 and 6 are spares at the present time. The remaining digit positions are utilized as follows.

Bit 13 - ENGINE ON - This digit position is used to control the Service Module Engine. Whenever a binary 1 is placed in this digit position, a 3200 pps 3 μ sec. pulse width signal is developed which causes the engine to fire. A binary 0 in this digit position produces a signal which turns the engine off.

BIT	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
OUT "0" REGISTER		RELAY WORD 4	RELAY WORD 3	RELAY WORD 2	RELAY WORD 1	RELAY BIT 11	RELAY BIT 10	RELAY BIT 9	RELAY BIT 8	RELAY BIT 7	RELAY BIT 6	RELAY BIT 5	RELAY BIT 4	RELAY BIT 3	RELAY BIT 2	RELAY BIT 1

USED TO SELECT 1 OF 14 RELAY MODULES IN DSKY.

USED TO SET OR RESET THE 11 RELAYS WITHIN THE SELECTED RELAY MODULE IN DSKY.

Figure 14-54. OUT 0 Register Bit Assignments

BIT	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
OUT "1" REGISTER		S.P. N.C.	S.P. N.C.	ENG. ON	S.P. N.C.	S.P. N.C.	BLOCK END PULSE	ID WORD	S.P. N.C.	RUPT 2 TRAP RESET	S.P. N.C.	CHECK FAIL	TEL. ALARM	KEY RELEASE	COMP. ACT.	PROG. ALARM

Figure 14-55. OUT 1 Register Bit Assignments

Bit 10 - BLOCK END PULSE - This digit position, when it contains a binary 1, inhibits the TELEMETRY END PULSE from the Communications and Instrumentation System. This inhibits the AGC from loading a new computer word for downlink telemetry transmission. The digit position is set to a binary 1 whenever the downlink telemetry word rate from the AGC exceeds 50 words/sec. This is done so that the AGC does not utilize too much time loading AGC words for downlink transmission.

Bit 9 - ID WORD - This digit position is used in conjunction with AGC words which are transmitted via downlink telemetry. It is used to define what type of AGC word is being transmitted.

Bit 7 - RUPT 2 TRAP RESET - This digit position is used to reset the trap circuitry associated with RUPT 2 or the ERROR RUPT program interrupt.

Bit 5 - CHECK FAIL - This digit position is used to indicate to the astronaut or the operator of a ground based keyboard that he has made an error in the operation of the keyboard of the DSKY. The digit position being set to a binary 1 causes the CHECK FAIL indicator panel of the NAV. DSKY and the COMPUTER FAIL indicator of the MAIN DSKY to illuminate.

Bit 4 - TELEMETRY ALARM - This digit position is set to a binary 1 when a failure is detected in either the UPLINK or DOWNLINK telemetry systems. A binary 1 in this digit position causes the TL FAIL indicator panel of the NAV. DSKY to illuminate. A telemetry fail consists of one or more of the following:

a. UPLINK TELEMETRY bit rate exceeding 1600 bits per sec.

b. A detected error in the data transmitted to the AGC via the UPLINK telemetry system.

c. The DOWNLINK telemetry word rate from the AGC exceeding 50 words/sec. or by not having any words transmitted for a period of 120 ms.

Bit 3 - KEY RELEASE - This digit position, when set to a binary 1, indicates to the astronaut or the operator of a ground based keyboard that an AGC program desires to use the DSKY while the astronaut or the operator of the ground based keyboard is using the keyboard. The KEY RELEASE indicator panel on the NAV. DSKY and the KEY RELEASE indicator panel on the MAIN DSKY are illuminated whenever a binary 1 is placed in this digit position.

Bit 1 - PROGRAM ALARM - This digit position is set to a binary 1 whenever the AGC, through program control, determines an erroneous condition. Whenever an erroneous condition is detected, the PROG. ALARM indicator panel of both DSKY's is illuminated. Besides this, a particular VERB-NOUN code is displayed in the VERB and NOUN display panels and a numerical code is displayed in R1. The numerical code indicates what the detected erroneous condition was.

14.10.2.3 OUT 2 Register. The OUT 2 Register is used by the AGC to control the routing of pulses to various pieces of hardware. These pulses are used to control the generation of driving currents which position various portions of hardware.

In order to implement the generation of these pulse outputs, the OUT 2 Register is divided into three parts. One portion of the register, consisting of digits 15 through 9, is used for the generation of pulses to the CDU's and the IRIG's of the ISS. The second portion of the register, consisting of digits 8 through 4, is used in the generation of pulses to position the optical unit. The third portion of the register, consisting of digits 3, 2 and 1, is used to control the radar systems. These digit positions are not used at the present time.

Associated with each of the three portions of the OUT 2 Register is a counter implemented as one of the counter interrupts. Each of these counters is used to control the number of pulses routed to a particular piece of hardware as specified by the configuration of the binary 1's and 0's contained in the portion of the OUT 2 Register associated with the counter.

In order to provide control over the number of pulses, the AGC's program, which is required to pulse a piece of hardware, sets the counter associated with the hardware to overflow minus the number of desired pulses. The program then sets the portion of the OUT 2 Register to the proper bit configuration for the hardware it is required to pulse. At this time, a 3200 pps, 3 μ sec., pulse width signal is applied to the piece of hardware. This same waveform is routed within the AGC to the counter interrupt priority control circuitry of the AGC. Everytime an output pulse is developed, it causes a counter interrupt which increments the counter associated with the portion of the OUT 2 Register in use.

When the desired number of pulses has been developed, the counter associated with the portion of the OUT 2 Register overflows. This causes the portion of the OUT 2 Register to be reset to binary 0's which terminates the output pulse waveform.

Figure 14-56 shows the usage of the various digit positions and portions of the OUT 2 Register.

14.10.2.4 OUT 3 Register. The OUT 3 Register is presently a spare register.

14.10.2.5 OUT 4 Register. The OUT 4 Register is used exclusively to provide the DOWNLINK telemetry system with the AGC words. The outputs of this register are inputs to the serializing circuitry of the AGC. The serializing circuitry is controlled by control pulses developed by the telemetry programmer of the Communications and Instrumentation System. These control pulses control word rate and bit rate of the AGC word transmissions and also initiate the loading of the OUT 4 Register with a new AGC word to be transmitted (figure 14-57).

The loading of the OUT 4 Register is initiated by a TLEND (telemetry end) control pulse. When this pulse is present, it generates a request for the DOWNRUPT routine to be initiated through the program interrupt priority control circuitry of the AGC. The DOWNRUPT routine loads the OUT 4 Register with the AGC word to be transmitted to the ground via downlink telemetry.

Figure 14-58 lists all of the input-output registers and the use of their bit positions.

BIT	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
OUT "2" REGISTER		-	+	CDU	GYRO	X	Y	Z	-	+	OPT X	OPT Y	THRUST	RADAR A	RADAR B	RADAR C
		← OUT COUNTER 1 →							← OUT COUNTER 2 →					← OUT COUNTER 3 →		

Figure 14-56. OUT 2 Register Bit Assignments

BIT	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
OUT "4" REGISTER					D T	O E	W L	N E	L M	I E	N T	K R	Y			

PARITY BIT FORCED INTO BIT 15
FOR TRANSMISSION TO GROUND
STATION WHEN OUT "4" IS LOADED.

Figure 14-57. OUT 4 Register Bit Assignments

BIT / REGISTER	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
IN0		MARK	S.P. N.C.	G/N ENTRY MODE	G/N ΔV MODE	G/N ATT. CONT. MODE	SP. N.C.	SP. N.C.	SP. N.C.	IHIBIT UPSYNC	BLOCK UPLINK	KEY CODE 5	KEY CODE 4	KEY CODE 3	KEY CODE 2	KEY CODE 1
IN1		2	4		H	O	U	R		C	O	U	N	T	E	R
IN2		PARITY FAIL	G/N MON. MODE	SCS ΔV MODE	IMU FAIL	PIPA FAIL	CDU FAIL	SM/CM SEP	SIVB SEP	SATN ULL.	GUID REL	LIFT OFF	F T 200PPS	I I 400PPS	N M 800PPS	E E 1600PPS
IN3		OR OF CI-C33	COMP. CONTR. OPT.	SP NC	ZERO OPT	STAR PRES	TRKR ON	SP NC	SP NC	K5 ENTRY	TRN SW	K12 ATT. CONTR	K4 FINE ALIGN	K3 MANUAL CDU	K2 COARSE ALIGN	K1 ZERO ENCODE
OUT 0		RELAY WORD 4	RELAY WORD 3	RELAY WORD 2	RELAY WORD 1	RELAY BIT 11	RELAY BIT 10	RELAY BIT 9	RELAY BIT 8	RELAY BIT 7	RELAY BIT 6	RELAY BIT 5	RELAY BIT 4	RELAY BIT 3	RELAY BIT 2	RELAY BIT 1
OUT 1		SP NC	SP NC	ENG ON	SP NC	SP NC	BLOCK END PULSE	ID WORD	SP NC	RUPT 2 TRAP RESET	SP NC	CHECK FAIL	TEL ALARM	KEY RELEASE	COMP ACT.	PROG ALARM
OUT 2		−	+	CDU	GYRO	X	Y	Z	−	+	OPT X	OPT Y	THRUST	RADAR A	RADAR B	RADAR C
		← OUT COUNTER 1 →							← OUT COUNTER 2 →					← OUT COUNTER 3 →		
OUT 3						S	P	A	R	E	S					
OUT 4					D T	O E	W L	N E	L M	I E	N T	K R	Y			

NC= NOT CONNECTED

Figure 14-58. Input-Output Bit Assignments

14.10.3 OUTPUT DRIVE PULSES OF THE AGC. The AGC generates drive pulses of various frequencies which are continuous outputs or outputs controlled through program action. These output drive pulses are utilized within the G&N system for power supply control, stabilization and accelerometer loop control, positioning control of stable member and optical unit and other miscellaneous functions. The AGC also supplies the basic frequency standard for the entire spacecraft and furnishes various control functions for other spacecraft systems.

14.10.3.1 Program Controlled Drive Pulse Outputs. The AGC, through its program controlled output drive pulses, controls the positioning of the stable member. The AGC can also steer the spacecraft and control the spacecraft's attitude. Another function provided for by the program controlled drive pulses of the AGC is the positioning of the optical unit to a desired orientation.

All of the control pulse outputs mentioned above are developed by setting the OUT 2 Register to the proper configuration for the desired output. The OUT 2 Register, as previously discussed, is divided into three separate parts each of which has an associated counter in erasable memory. These counters are incremented when a pulse output is generated by its associated portion of the OUT 2 Register. To control the number of pulses developed to the hardware specified by the configuration of the OUT 2 Register, the associated counter is set to overflow minus the desired number of pulses. Then, as the pulses are developed, the counter is incremented towards overflow. When the desired number of pulses have been developed, the counter will be in the overflow state. This condition is used to reset the appropriate portion of the OUT 2 Register thereby terminating the generation of the pulses.

The outputs developed from the block diagram for the OUT COUNTER 1 portion of the OUT 2 Register are shown in figure 14-59. This portion of the OUT 2 Register consists of bit positions 15 through 9 and is capable of generating drive pulses to any one of the three IRIG's or CDU's in either the positive or negative direction. Only one of these pieces of hardware can be driven at any one time.

The procedure used by the AGC through program control to develop a given number of pulses to a particular piece of hardware is presented in this paragraph. First, the AGC would calculate the number of pulses required to position the stable member to a desired position. It sets the counter associated with the portion of the OUT 2 Register to be used to overflow minus the calculated number of pulses required. Assuming that an IRIG is to be driven, the counter that is set is the OUT COUNTER 1. The OUT 2 Register, bits 15 through 9, are set to the proper configuration. Assuming that the X IRIG is to be driven in the positive direction, these seven bits would be set to 0101100. After the OUT 2 Register is set to this configuration, the generation of pulses to the +X IRIG commences. These pulses form a 3200 pps, 3 μ sec. pulse width waveform which is routed to the + input of the X IRIG trinary current switch. This waveform, along with the GYRO RESET pulses, a continuous output, cause the X IRIG float to be torqued so that a positive rotation about the stable member X axis is achieved. For each of the output pulses developed, the OUT COUNTER 1 is incremented. This process continues until the OUT COUNTER 1 overflows which occurs when the desired number of pulses have been generated. The overflow state of the counter is then used to reset bits 15 through 9 of the OUT 0 Register to binary 0's. This terminates the generation of the output pulses.

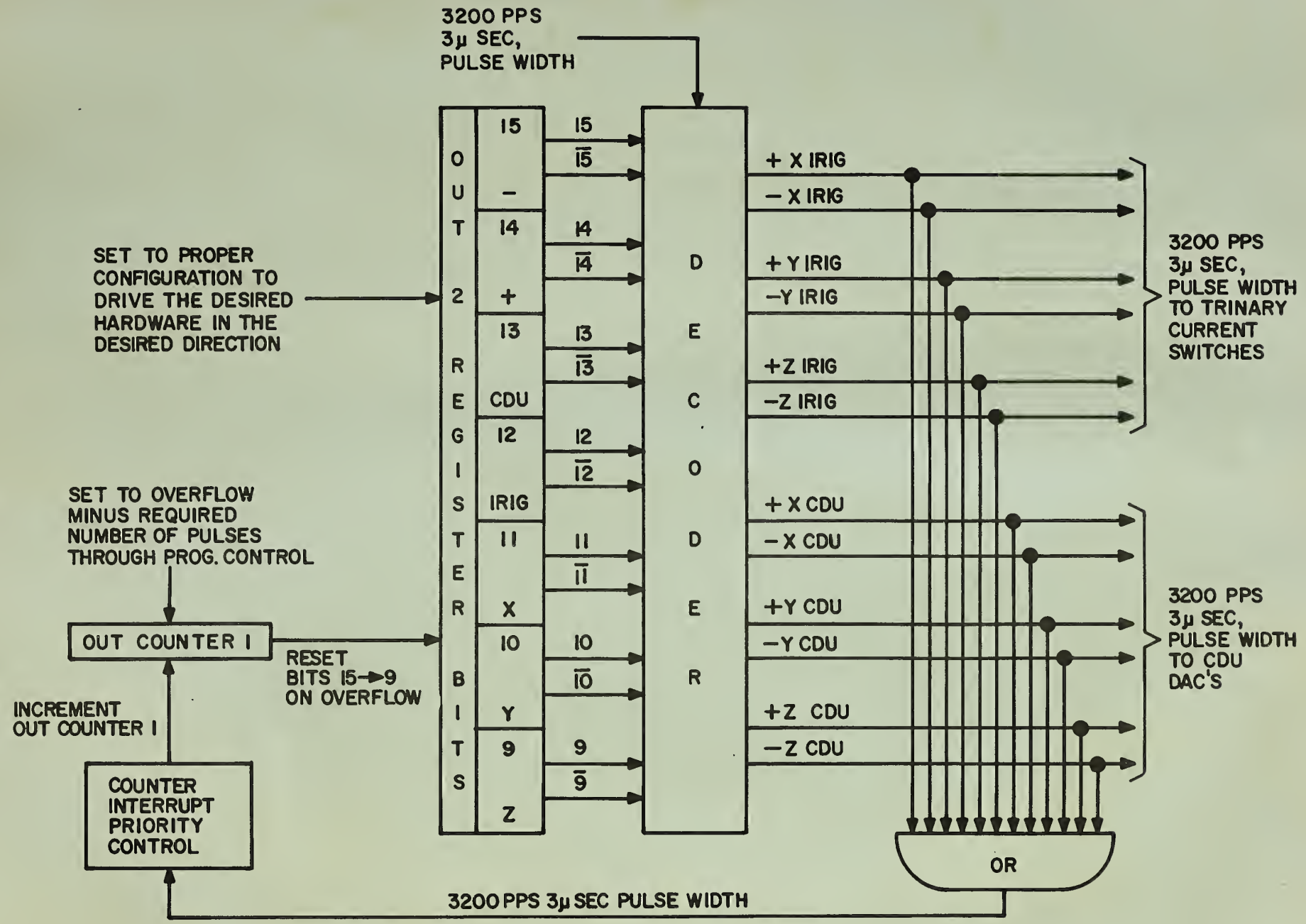


Figure 14-59. Development and Control of Program Controlled Drive Pulse Outputs

The outputs and the control of the number of output pulses is identical for the other two portions of the OUT 2 Register. The OUT COUNTER 2 portion of the OUT 2 Register utilizes bit positions 8 through 4 and the OUT COUNTER 2 in memory while the OUT COUNTER 3 portion of the OUT 2 Register utilizes bit positions 3 through 1 and the OUT COUNTER 3 in memory.

Another pulse type output controlled through program action is developed whenever bit 13 of the OUT 1 Register is set to a binary 1. This bit position, ENGINE ON, controls the firing of the service module engine. When this bit position is a binary 1, the signal generated to turn on the engine has a frequency of 102.4 K pps. Similarly, bit positions 15 and 14 develop a 102.4 K pps signal when set to a binary 1, but these positions are spare outputs at this time.

14.10.3.2 Continuous Drive Pulse Outputs. The continuous drive pulse outputs of the AGC are completely independent of program control. These pulse waveforms are generated whenever the AGC is in either the STANDBY or OPERATE modes and originate in the Scaler A of the AGC's timing circuitry. These output signals, their frequency and purpose are listed in table 14-12.

14.10.4 TELEMETRY INPUTS AND OUTPUTS. The AGC has the capability of receiving digital inputs and transmitting digital outputs using telemetry techniques. The transmission of data to the AGC is known as UPLINK while the transmission of data from the AGC is known as DOWNLINK. Both the uplink and downlink telemetry systems are used during the preflight checkout of the G&N system and during flight itself. During ground checkout, the data link is over hardwire. In flight, the data link is over an RF link.

14.10.4.1 Uplink Telemetry Inputs. Uplink refers to incoming serialized telemetry data. The uplink counter (0041_8) and the SHINC and SHANC instruction are used for serial to parallel conversion. Sixteen serialized input bits, when converted to parallel, make one word which constitutes a complete input datum. Figure 14-60 shows the uplink interface flow diagram. An input 1 pulse or 0 pulse is received and stored in a manner identical to the counter inputs for + or - pulses. A 0 input produces an $\overline{\text{INKL}}$ and a SHINC request which is applied to the sequence generator. A 1 pulse produces a SHANC request instead of a SHINC. The counter priority control circuits will generate a six-bit address calling out UPLINK counter location 0041_8. This address is written into the S Register via the write amps where it calls out the contents of the UPLINK counter, called C (CTR). If a SHINC is being executed, the C (CTR) is written into to X and Y inputs of the adder. Shifting results from this addition. For example, adding 1011 to 1011 results in 10110 which is shifted to the left. Notice that the new bit shifted in is a zero which represents the incoming NO bit. If a SHANC (Shift and increment) is being executed, the C (CTR) is read into both inputs of the adder.

A one is then added to the shifted contents. For example, 1011 plus 1011 plus 1 is 10111. Notice that the new bit is a 1 and the previous content has been shifted. The new counter content is then returned to memory in location 0041_8. Each of the sixteen bits entering causes a separate SHINC or SHANC.

The first uplink bit in each word is always a binary one. Thus, after 16 shifts, when the word is completely converted to a parallel, a one is detected in bit 16 which causes the generation of UPRUPT within program interrupt priority control. The AGC then transfers control to a specified routine that reads the contents of the uplink counter then resets it to all zeros.

Table 14-12. Continuous Drive Pulse Outputs

Signal	Frequency	Purpose
Master clock	1.024 mc	CTE frequency reference
Gyro reset	102.4 K pps	Ternary current switch reset
PIPA interrogate	3200 pps	PIPA loop control
PIPA switch	3200 pps	PIPA loop control
Discrete carrier	102.4 K pps	Star tracker
PSA set	800 pps	PSA power supply control
PSA reset	800 pps	PSA power supply control
PSA set	3200 pps	PSA power supply control
PSA reset	3200 pps	PSA power supply control
PSA set	25.6 K pps	PSA power supply control
PSA reset	25.6 K pps	PSA power supply control
PSA sync	12.8 K pps	PSA power supply control
PSA discrete carrier	102.4 K pps	PSA power supply control
Power supply sync	800 pps	Nav & main DSKY power supply sync
Flash	1.56 pps	Flash of noun-verb display panels of DSKY's

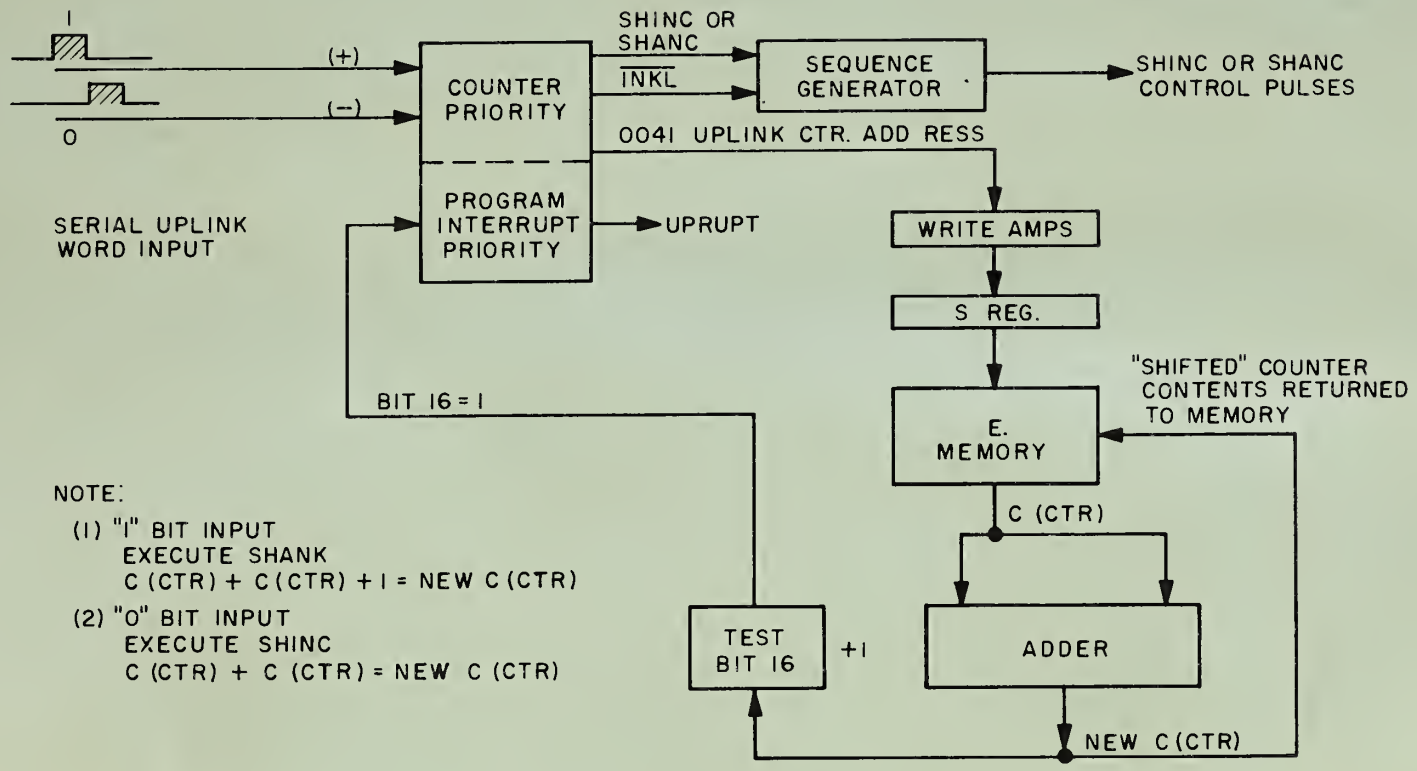


Figure 14-60. Uplink Interface Flow Diagram

The remaining fifteen bits of information transmitted to the AGC by one 16 bit uplink word are made up of three copies of a five digit keycode identical to those generated by the DSKY keyboard. Of the three copies of the keycode, one is in the complemented form. These three copies of the keycode are used by the UPRUPT routine to verify the transmission. The word format is shown in figure 14-61.

The UPTL switch on the main panel DSKY when placed in the block position inhibits the uplink data from being shifted in and from causing an UPRUPT. This input indication is routed to bit 6 of the IN 0 Register.

A detector circuit associated with the uplink telemetry input is used to check to see if the bit rate of the uplink data is too high. If the rate exceeds 1600 bits/sec., a binary 1 is placed into bit 7 of the IN 0 Register (INHIBIT UPSYNC). The nominal transmission rate is 1000 bits/sec with a maximum word rate of 10 words/sec.

14.10.4.2 Downlink Telemetry Outputs. Downlink, as far as the computer subsystem is concerned, consists of the downlink converter which operates in response to external telemetry programmer control. A downlink computer program is necessary to "load" the appropriate data into the OUT 4 register which is to be used by the downlink converter. Two different rates are used for the downlink telemetry system. 50 word/sec, 51.2 K bits/sec; 10 word/sec, 1.6 K bit/sec.

Three incoming signals control the AGC downlink converter. These are plotted on figure 14-62. The telemetry system transmits data to the ground at the rate of 50 frames per second. A frame consists of 128 eight bit telemetry words. Five of these words are allotted for AGC in each frame; therefore, AGC data is sent out every 20 milliseconds. One 16 bit computer word is sent out twice each frame (figure 14-63). Telemetry words one and two contain bits 16 through 9 bits 8 through 1 respectively. Telemetry words 3 and 4 contain a repeat of words 1 and 2. Word 5 contains the "word order bits". These 8 bits contain all ones whenever a computer data word is being transmitted. Any other time the word order bits contain all zeroes.

(1) Identification Word

(2) Data Word

(3) Relay Word

(4) Input Character Word.

An identification word is issued at the beginning of every four computer data words. The ID word identifies the kind of data contained within the following four data words. The data word (computer data word as opposed to the 8 bit telemetry data words) contains computer data which is obtained from various erasable memory locations. Examples of computer data words are the contents of the PIPA counters, CDU counters, TIME counters, etc. There are approximately 30 different locations in erasable memory supplying AGC data. All of these will be sampled once per second. The Relay Word is the word loaded into OUT 0 used to cause DSKY displays or G&N moding changes. This word is transmitted when a change occurs. The input character word contains uplink or keyboard inputs. Again, this word is transmitted when one of these changes occur. Thus, all input information to the computer via the keyboard or UPLINK is transmitted back to the ground tracking station. In addition, displays and moding changes will be transmitted to the ground. In effect, the critical interfaces between the astronaut and the computer subsystem are duplicated at the ground tracking station.

BIT	16	15 14 13 12 11	10 9 8 7 6	5 4 3 2 1
CONTENTS	1	KEYCODE	$\overline{\text{KEYCODE}}$	KEYCODE

Figure 14-61. Uplink Word Format

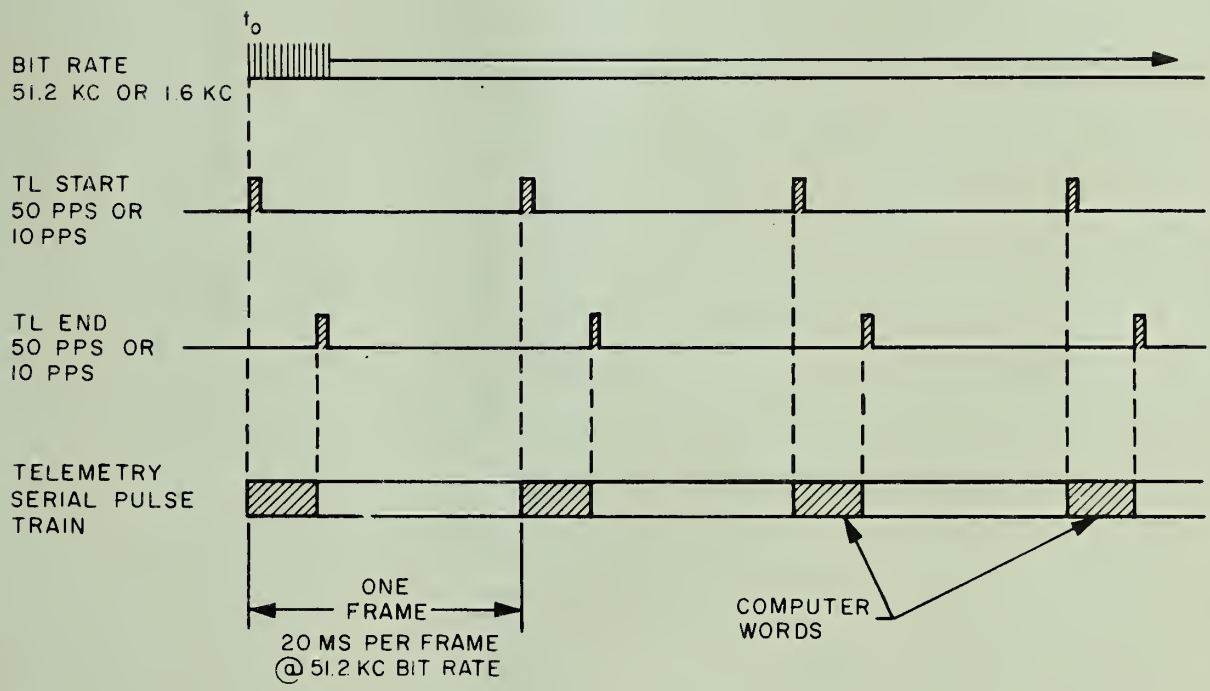


Figure 14-62. Telemetry Timing

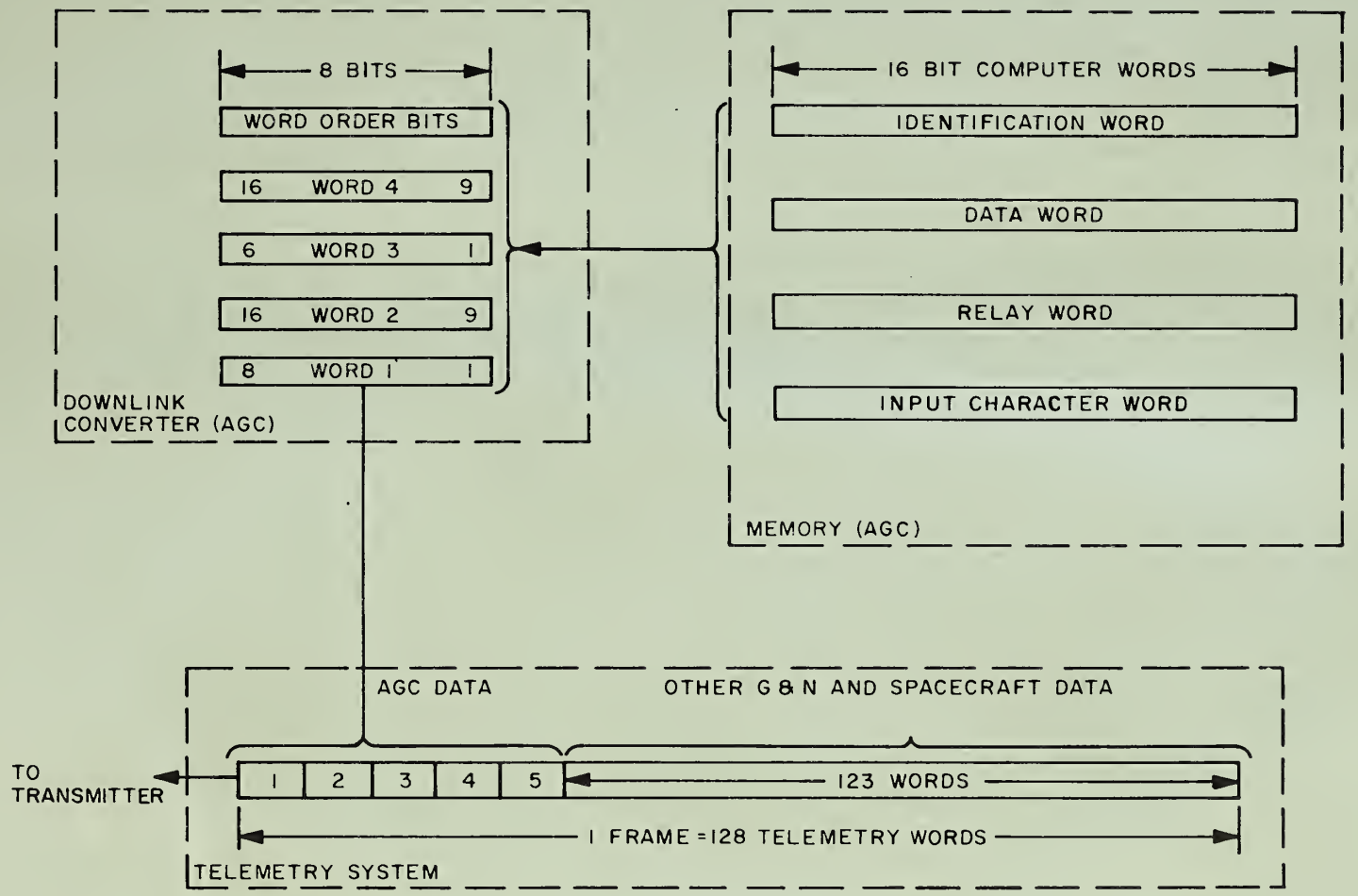


Figure 14-63. Downlink Formats

Figure 14-64 shows a downlink converter interface flow diagram. The downlink converter operates asynchronously to the AGC timing. The three external inputs control the downlink converter. The OUT 4 Register always contains the next computer word to the serialized and sent to the telemetry system. The action begins at the receipt of the TL START pulse which occurs 50 times per second. This signal sets a start flip-flop which passes the 51.2 KC bit rate as a trigger to a 32:1 binary counter. As the 32 pulses are counted, sample pulses are applied to the parallel to serial converter which twice serializes the parallel sixteen-bit word in the OUT 4 Register. These words are applied in serial form where they are synchronized by the 51.2 KC basic bit rate. After four telemetry words are sent out (32 bits) the 32:1 counter overflows and sets the RESET flip-flop. The set output of the RESET flip-flop resets the start flip-flop and the 32:1 counter which prevents further parallel to serial conversion of the OUT 4 word. In addition, the word order gate is enabled. The word order bits are now injected in serial form. They will contain all 1's if there is a logic 1 in bit number 9 of the OUT 1 Register. They will contain all 0's if the bit number 9 of the OUT 1 Register is 0. After the 8 word order bits are sent out, the TLEND pulse will be present from the telemetry programmer. This pulse will cause the RESET flip-flop to reset which will disable the word order gate. If the BLOCK END PULSE is present, however, the TLEND pulse will have no effect. Notice that the block end pulse must be programmed via OUT 1 bit number 10. The block end pulse occurs when a programmed test on the incoming TLEND pulses shows the telemetry programmer has malfunctioned.

The arrival of the TLEND pulse also generates signal DKEND which is applied to the program interrupt priority control where a downrupt results. A routine is then entered which loads the OUT 4 Register with a new computer word and sets OUT 1 bit 9 to the appropriate configuration. The process repeats upon the arrival of a new TLSTART pulse from the telemetry system. At the reduced bit rate of 1.6 KC, the TLSTART and TLEND pulses occur at the rate of 10 pps. Ten frames per second are then transmitted. The downlink converter will operate in a similar manner using the 10 pps frame rate.

14.10.5 AGC MALFUNCTIONS. The AGC has the capability of detecting and displaying a number malfunctions associated with its operation. Some of these malfunctions are detected through hardware or circuit functions while others are detected and displayed through program action. Most of these malfunction conditions are displayed on the navigation and main panel DSKY's.

14.10.5.1 Program Detected Malfunctions. The program detected malfunctions of the AGC consist of the following:

a. PROGRAM ALARM

b. CHECK FAIL

c. TELEMETRY FAIL

These alarm conditions are presented in the AGC programs portion of the course. In general, these alarm conditions are caused by:

a. PROGRAM ALARM -- procedural problems involving the execution of the AGC's program.

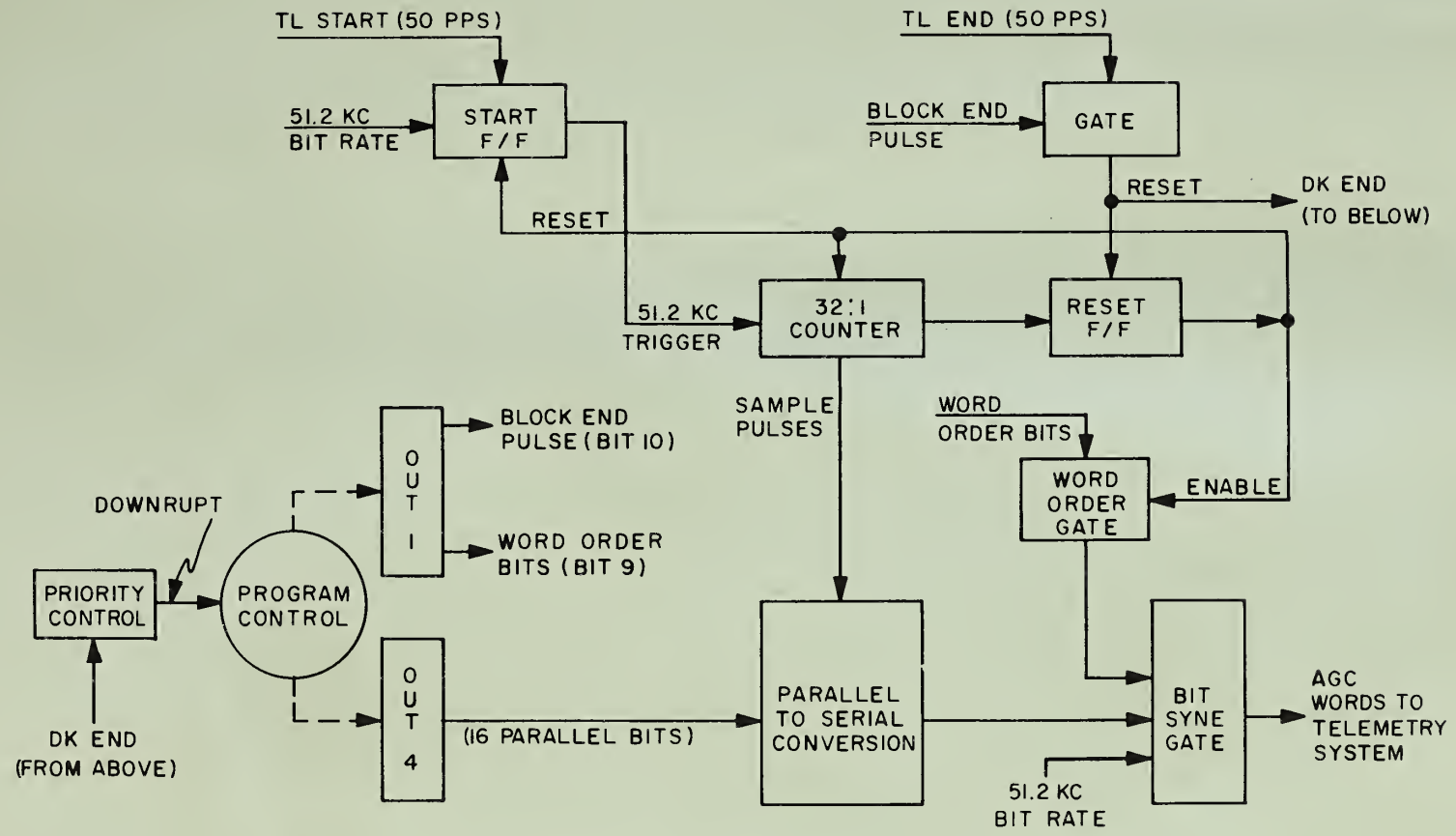


Figure 14-64. Downlink Converter Interface Flow Diagram

b. CHECK FAIL -- procedural problems involving the entry of information through the DSKY keyboard or by uplink telemetry.

c. TELEMETRY FAIL -- caused by either uplink or downlink telemetry problems.

Telemetry malfunctions are caused by:

a. A downlink telemetry word rate which is too high or too low.

b. An uplink telemetry bit rate which is too high.

c. An erroneous transmission of uplink telemetry.

14.10.5.2 Circuit Detected Malfunctions. The following AGC malfunctions are detected through circuit functions:

a. AGC POWER FAIL

b. TC TRAP

c. COUNTER FAIL

d. RUPT LOCK

e. SCALER FAIL

f. PARITY FAIL

The circuits for these malfunctions are activated by the following conditions:

a. AGC POWER FAIL -- this malfunction is caused by the +3 or +13 volt power supply outputs being out of tolerance or a complete failure of one of these power supplies. Also, this circuitry monitors the +28 volt prime power input to assure that its voltage does not drop below a specified level.

b. TC TRAP -- The TC TRAP alarm circuit generates this alarm if a TC instruction has continuously been in effect or if no TC instruction has been executed during a 10 ms period of time.

c. COUNTER FAIL -- The COUNTER FAIL alarm circuit generates this alarm if a request for a counter increment is present and it is not executed or if a counter interrupt is continuously in process during a 10 ms period of time. If a counter interrupt is in process continuously for 10 ms, the TC TRAP alarm is also generated.

d. RUPT LOCK -- The RUPT LOCK alarm circuitry generates this alarm if a program interrupt is in process longer than 10 ms or if there have been no program interrupts for an 80 ms period of time.

e. SCALER FAIL -- The SCALER FAIL alarm circuitry monitors the 100 pps signal output of SCALER A of the AGC timing circuitry. If this signal is not present, the alarm condition is generated.

f. PARITY FAIL -- The PARITY FAIL alarm is generated whenever the AGC parity checking circuitry checks a word from memory which does not have odd parity. The PARITY FAIL, RUPT LOCK, TC TRAP and COMPUTER POWER FAIL conditions cause a restart of the AGC program in process. In addition to restarting the program in process, many routing flags and other quantities within the AGC are initialized and the program interrupt request flip-flops are cleared.

14.11 POWER

AGC power (figure 14-65a) is furnished by two switching-regulator power supplied: a +3 and a +13 volt power supply which are energized by fuel cells in the Electrical Power System.

Input voltage from the Electrical Power System is chopped at a variable duty cycle and then filtered to produce the required voltages. Chopping is accomplished by varying the pulse width of a signal having a fixed repetition rate and known amplitude. Referring to figure 14-65b, V_{out} can be stated as:

$$V_{out} = V_{max} \frac{\Delta}{A}$$

where: A is the fixed repetition rate,

Δ is the pulse width,

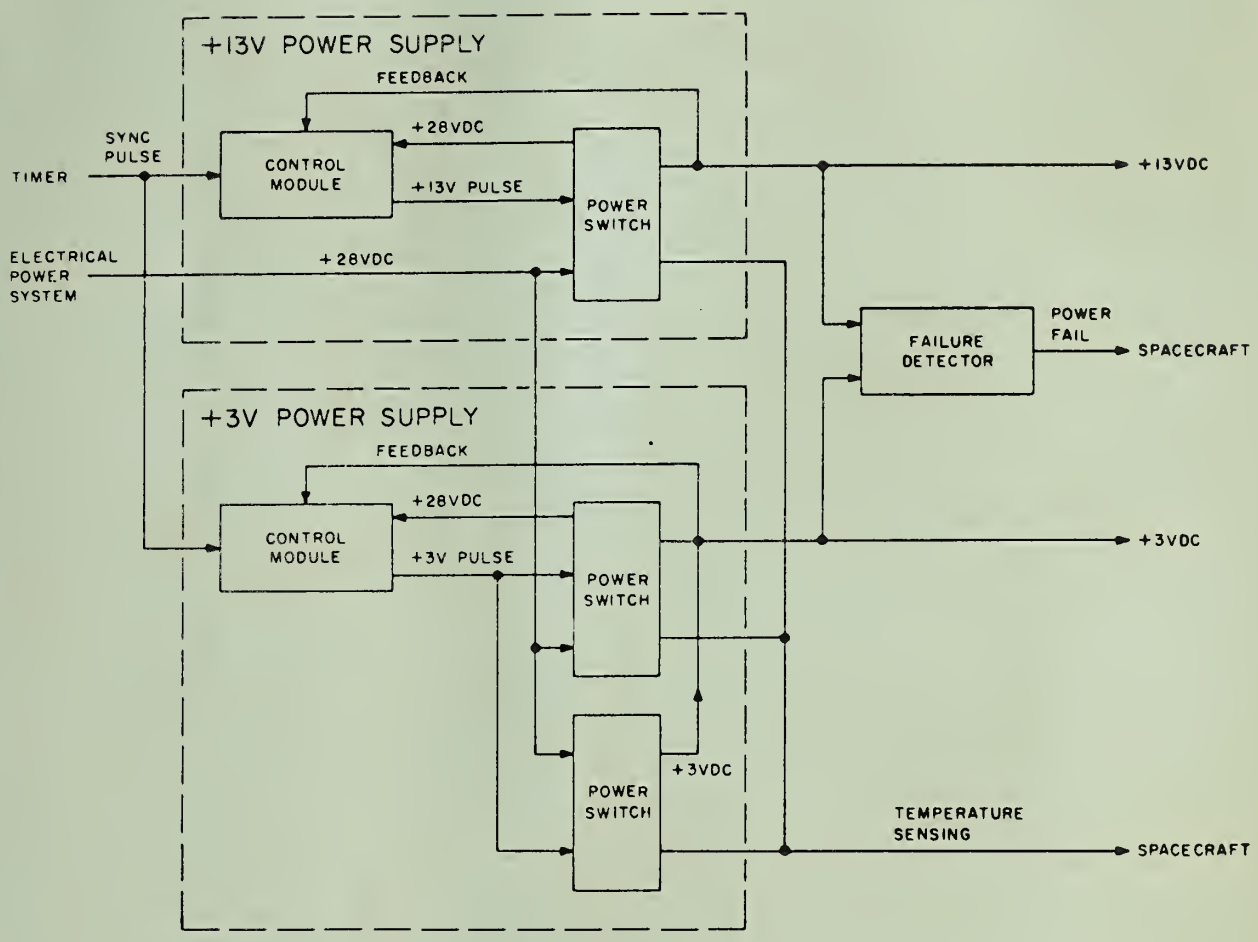
V_{max} is the known input amplitude.

Therefore, V_{out} can be varied by changing the pulse width, Δ. Operation of the +13 volt power supply, which is typical of both, is discussed.

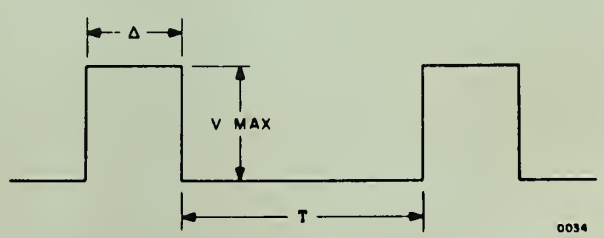
Source voltage, +28 vdc, is supplied from the Electrical Power System through the power switch to the control module. The control module, essentially a pulse generator, detects the difference between the primary feedback output of the power supply and a refernce voltage. (A secondary feedback path is connected to the CTS for marginal-voltage test operations.) A differential amplifier detects any change in the output voltage from the desired level. The output of the differential amplifier and a 51.2 kilocycle sync pulse from the timer drives a one-shot multivibrator in the control module. The differential amplifier output determines the multivibrator pulse width. The resultant +13 volt pulse is supplied to the power switch.

The power switch filters the control module output to produce the desired dc voltage. Additional filtering action protects the Electrical Power System from the wide load variations caused by the chopping action of the power supply. The power switch also contains a temperature sensing circuit. The +3 volt power supply requires two power switches due to load requirements.

The power supply outputs are monitored by a failure detector consisting of four differential amplifiers. There are two amplifiers for each power supply, one for overvoltage and one for undervoltage detection. If an overvoltage or undervoltage condition exists, a relay closure signal indicating a power fail is supplied to the spacecraft.



(a)



(b)

Figure 14-65. Power Supplies

14.12 SUMMARY OF AGC DATA FLOW

To obtain a new instruction, the content of the Register Z is read into the S Register via the write amps. This selects the proper instruction since the Z Register always contains the a address of the next instruction. The new instruction word is gated out of memory into the G Register where the parity bit is removed and routed to the parity circuitry, P. The new instruction is then written into the B Register for temporary storage. Simultaneously it is written into the parity block so that a parity check can be performed. The instruction counter, Z, is updated by 1 so that it will contain the address of the next instruction. This process of obtaining an instruction takes 1 MCT. Now it is time to carry out the instruction.

The instruction word is gated out of the B Register. Bits 1 through 12, which constitute the address portion of the instruction word, are gated into the S Register. Here they will provide the code necessary to locate and address the appropriate data word. The order code portion of the instruction word is entered into the SQ register where it is then routed to the sequence generator. The sequence generator interprets the order code to determine what operation is to be carried out. It combines this information with basic timing pulses from the timer to produce sequential sets of control pulses that are used to gate and manipulate the data word called out from memory. This process of obtaining and manipulating the data word takes at least one MCT. If an addition had been performed, the sum would now be in the A Register.

The AGC is now ready to obtain the next instruction using the Z Register and the process begins again. This general flow of information is a continuous process with the AGC unless an interruption occurs breaking the normal sequence of operation. External signals of the counter increment variety or program interrupts could cause this to occur. An input into priority control would be stored. The sequence generator would be told that a request is present. The sequence generator then would generate the pulses necessary to carry out the requested involuntary instruction. The address of the "counter" or the address of the new requested program would be generated by the priority control and "forced" into the S or Z Registers, respectively, via the WA's. Input discretes are routed directly through the input interface to the IN registers where they are stored. The AGC can then examine the contents of the IN registers by addressing them. Outputs are initiated by addressing the OUT registers. In some cases, the bits are sent out as discretes from the OUT registers via the output interface. In other cases, the OUT registers are enabled to pass pulse outputs. An example of this would be the torquing of the stabilization gyros. The input and output interface is used to isolate external signals from the AGC internal circuitry because of noise considerations.

14.13 SUMMARY

The AGC is a general purpose and control computer which is the "brain" center of the G&N system. The AGC performs calculations and control functions according to a series of instructions which is a result of conditions internal and external to the AGC. As a general purpose computer, the AGC solves the guidance and navigation problems associated with the Apollo Mission. As a control computer, the AGC interfaces with the G&N and other spacecraft systems to direct action of the associated hardware.

The AGC uses 16 bit words and odd parity, i.e., all words in memory contain an odd number of 1's. The adding circuitry of the AGC is found in the central processor and can manipulate both angular and non-angular data. The central processor consists primarily of flip-flop registers which have a non-destructive readout.

Fixed and erasable memories both utilize cores as storage devices. These cores are used differently, however, in each memory. One sense line is associated with each core in erasable memory but 128 sense lines are associated with each core in fixed memory.

REVIEW QUESTIONS FOR SECTION XIV

T F 1. The AGC uses negative logic.

T F 2. The AGC uses the binary twos complement method for addition.

T F 3. An instruction word in memory contains an address code and an order code.

T F 4. Parity bits are only included in words which are stored in memory.

T F 5. The result of an addition is normally stored in the B Register.

T F 6. The sequence generator controls and directs the execution of machine instructions.

T F 7. Information may be loaded into the fixed memory by the operator using the main DSKY.

T F 8. The order code of an instruction word is sent to the counter increment priority control.

T F 9. Readout of the hardware registers in non-destructive.

T F 10. The function of the BANK Register is to select a given core in fixed memory.

T F 11. Positive pulse have priority over negative pulses in priority control.

T F 12. Continuous drive pulse outputs are generated while the AGC is in the STANDBY mode.

T F 13. The G Register is located in the central processor.

SECTION XV

DISPLAY AND KEYBOARD FUNCTIONAL DESCRIPTION

INTRODUCTION

The CSS has two DSKY's associated with it: navigation panel DSKY (figure 15-1), main panel DSKY (figure 15-2). The nav panel DSKY is mounted to the right and slightly above the G&N indicator control panel. The main panel DSKY is mounted on the main display and control panel. Except for a few differences, the DSKY's are functionally identical.

The DSKY's provide the interface between the astronauts and the AGC. They enable the astronauts to (1) load information into the AGC, (2) request information from the AGC, (3) initiate various programs stored in the AGC's memory and (4) perform tests on the AGC and other portions of the G&N System. The DSKY's also provide indications of failures and operational changes which may occur within the AGC and G&N System. The AGC can, under its own control, initiate a display of information or request the astronaut to perform an action.

15.1 NAVIGATION PANEL DSKY KEYBOARD

The nav panel DSKY keyboard (figure 15-1) consists of ten digit keys (0 through 9), nine operation keys (+, -, VERB, NOUN, ENTER, CLEAR, KEY RLSE, ERROR RESET, TEST ALARM) and a BRIGHTNESS control. The BRIGHTNESS control varies the brightness of the display indicators.

Whenever a key, with the exception of the TEST ALARM key, is pressed, +13 VDC is applied to a diode matrix which generates a unique five bit code (keycode) associated with that key. The keys and their respective codes are shown in figure 15-3. The keycode is inserted into bits 5 through 1 of the AGC's IN 0 register. It is then logically ORed within the AGC to form the input request for a KEYRUPT. When any DSKY key is released, a KEYBOARD TRAP RESET signal resets the keyboard trap circuit of priority control. A key must be released before another key is pressed if information is to be properly processed by the AGC. The TEST ALARM key does not have a keycode associated with it: it is hard-wired directly to the AGC's alarm circuitry. The ERROR RESET key has a keycode associated with it; however, it is also hard-wired directly to the AGC's alarm circuitry.

15.2 MAIN PANEL DSKY KEYBOARD

The main panel DSKY keyboard (figure 15-2) consists of ten digit keys, eight operation keys, a BRIGHTNESS control and an UP TL switch. The main panel DSKY does <u>not</u> contain a TEST ALARM key.

The UP TL switch provides the astronaut with the capability of blocking or accepting uplink telemetry information. If this switch is placed in the BLOCK position, a logic 1 is inserted into bit 6 of the IN 0 register (figure 15-3). Note that the nav panel DSKY does not contain an UP TL switch.

Table 15-1 lists the keys on the main panel and nav panel DKSY's and states their functions. This table should be referred to while reading the rest of this section and Section XVI.

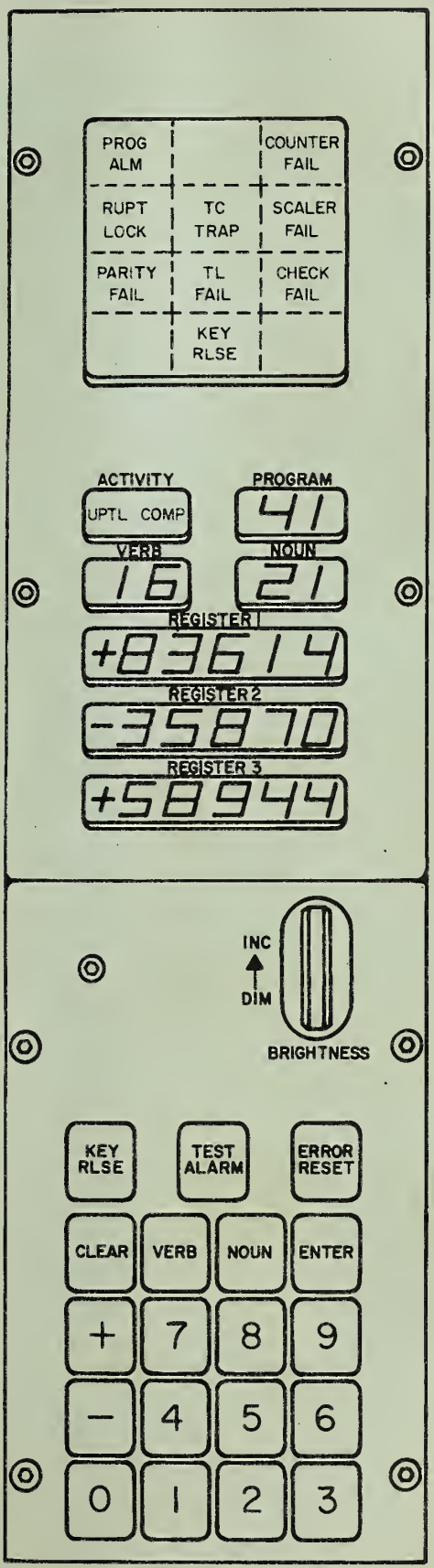


Figure 15-1. Navigation Panel Display and Keyboard

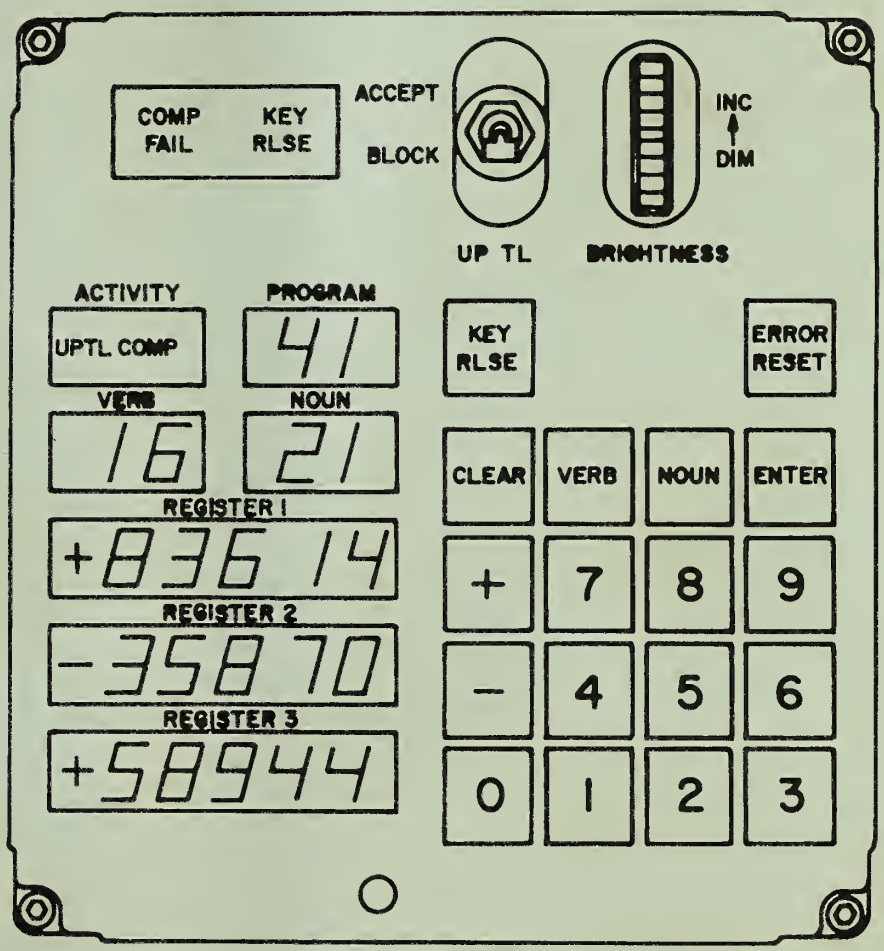


Figure 15-2. Main Panel Display and Keyboard

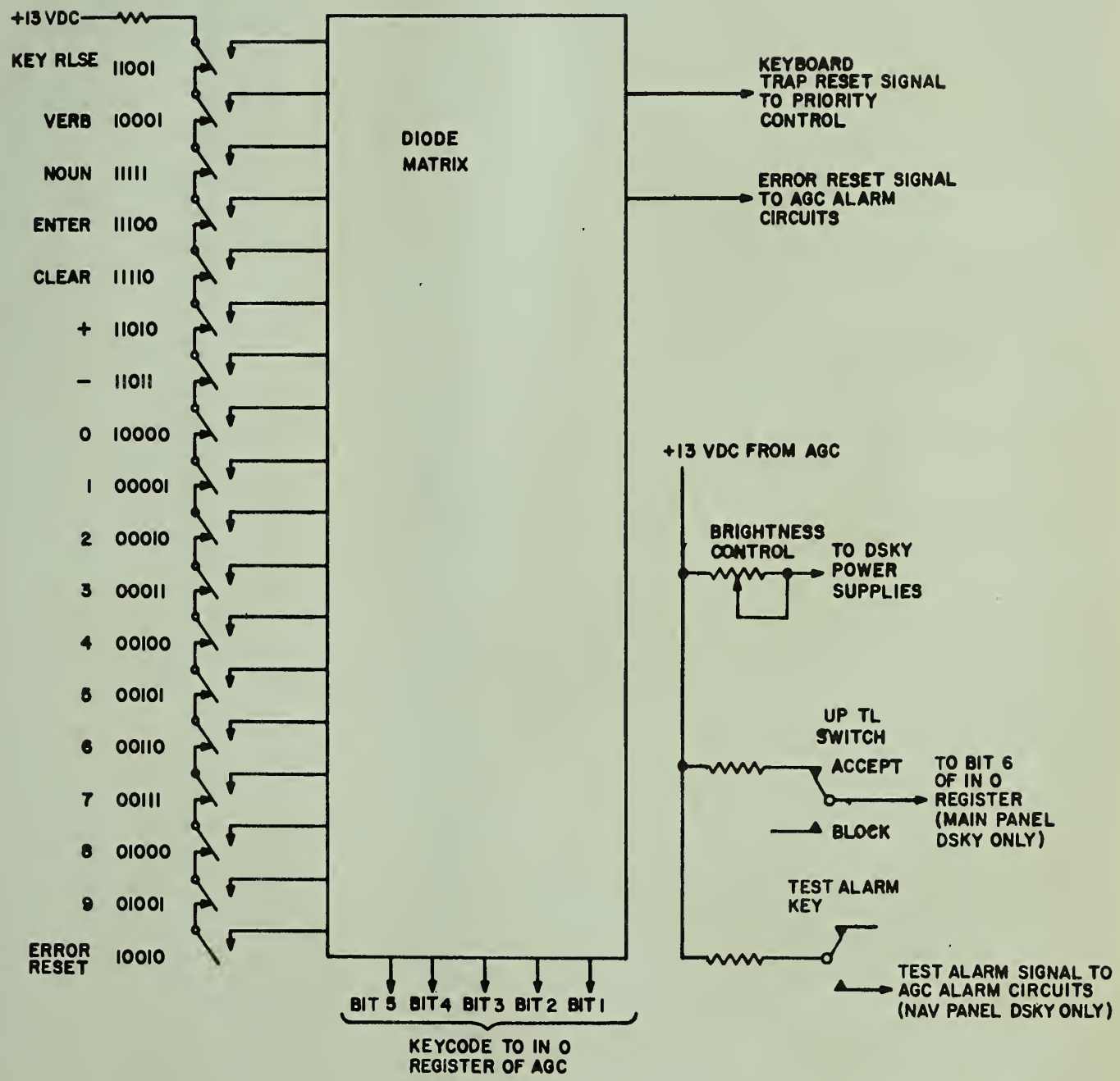


Figure 15-3. DSKY Keyboard and Associated Keycodes

Table 15-1. DSKY Keys and Functions

Key	Function
0 - 9	Enters digital data into the DATA, VERB, NOUN and PROGRAM displays.
+ and -	Enter the proper sign into the DATA displays for decimal data.
VERB	Blanks the VERB display and conditions the AGC to interpret the following two digital inputs as a verb code.
NOUN	Blanks the NOUN display and conditions the AGC to interpret the following two digital inputs as a noun code.
ENTER	Informs the AGC that the assembled data is complete and to execute the requested function.
CLEAR	Clears data contained in DATA display currently being used. Successive pressings clear the upper DATA displays.
TEST ALARM	Lights the PARITY FAIL, COUNTER FAIL, RUPT LOCK, TC TRAP and COMP FAIL alarm indicators to insure that they are properly working.
ERROR RESET	Tests for the presence of a transient or continuous alarm in the AGC.
KEY RLSE	Transfers control of the DSKY displays from the keyboard to the AGC program.

15.3 NAVIGATION PANEL DSKY DISPLAY

The nav panel DSKY display consists of six registers (figure 15-4). Registers 1 through 3 are also referred to as the DATA displays. Register 4 consists of the NOUN display and the VERB display. Register 5 consists of the PROGRAM display and the ACTIVITY display. Register 6 consists of eight alarm indicators and one condition indicator.

The DATA displays consist of five digit indicators and one sign indicator. Register 1, for example, consists of digit indicators R1D1 through R1D5 and sign indicator R1S. The VERB, NOUN and PROGRAM displays consist of two digit indicators each. The PROGRAM display, for example, consists of digit indicators P1 and P2. The ACTIVITY display consists of two condition indicators, UPTL and COMP. The condition indicator in Register 6 is the KEY RLSE indicator.

Associated with each digit indicator is a set of seven electro-luminescent lamps. Each set of lamps is controlled by a set of five bistable relays (figure 15-5). Associated with each sign indicator are three electro-luminescent lamps which are controlled by a set of two bistable relays (figure 15-6).

The relays mentioned in the preceding paragraph are controlled by the AGC through its OUT 0 register (figure 15-7). Other relays are also controlled by the OUT 0 register. The relay matrix shown on figure 15-7 consists of fourteen banks of eleven bistable relays. Any two of these fourteen banks can be interchanged. Bits 15 through 12 of the OUT 0 register form a four bit code which is sent to a set of four relay drivers. Each relay driver then generates two logic level outputs for its particular input: (1) the logic level of the input and (2) the complement of the logic level of the input. The eight bit code generated by these relay drivers is sent to a diode decoder which then supplies a ground to one of the fourteen banks of eleven bistable relays. This bank is uniquely specified by the eight bit code which, of course, is uniquely specified by the four bit code. The other thirteen banks receive no ground. The outputs of the relay drivers associated with bits 11 through 1 of the OUT 0 register are tied to the set and reset coils of the relays in each of the fourteen banks. Therefore, the outputs of the relay drivers associated with bits 11 through 1 of the OUT 0 register will set or reset those bistable relays in that bank to which ground has been applied. Consequently, if bits 15 through 12 of the OUT 0 register are 0, 0, 1, 1 respectively, bistable relays R23 through R33 will be set or reset depending on the configuration of bits 11 through 1 of the OUT 0 register.

The DSKY relay matrix contains 121 R (read) relays and 33 C (command) relays. With the exception of R88 and R110, all R relays are utilized directly by the sign and digit indicators. Figure 15-8 lists the R relays and codes them to the proper indicators. For example, R39 through R43 determine the number appearing in digit position 3 of Register 2.

The C relays are used for commanding modes, controlling failure indicators and providing control outputs to other areas of the spacecraft. These relays are unlike the R relays in that each C relay is associated with a separate function, i.e., a particular output discrete. Signals such as IMU FAIL, CDU FAIL, CM/SM SEPARATE, etc. are generated by the C relays. When any C relay is energized, an OR signal is developed and routed to bit 15 of the AGC's IN 3 register. A complete listing of the C relays and their associated signals will not be given because they will change from flight to flight. This information can be found in appropriate prints and documents.

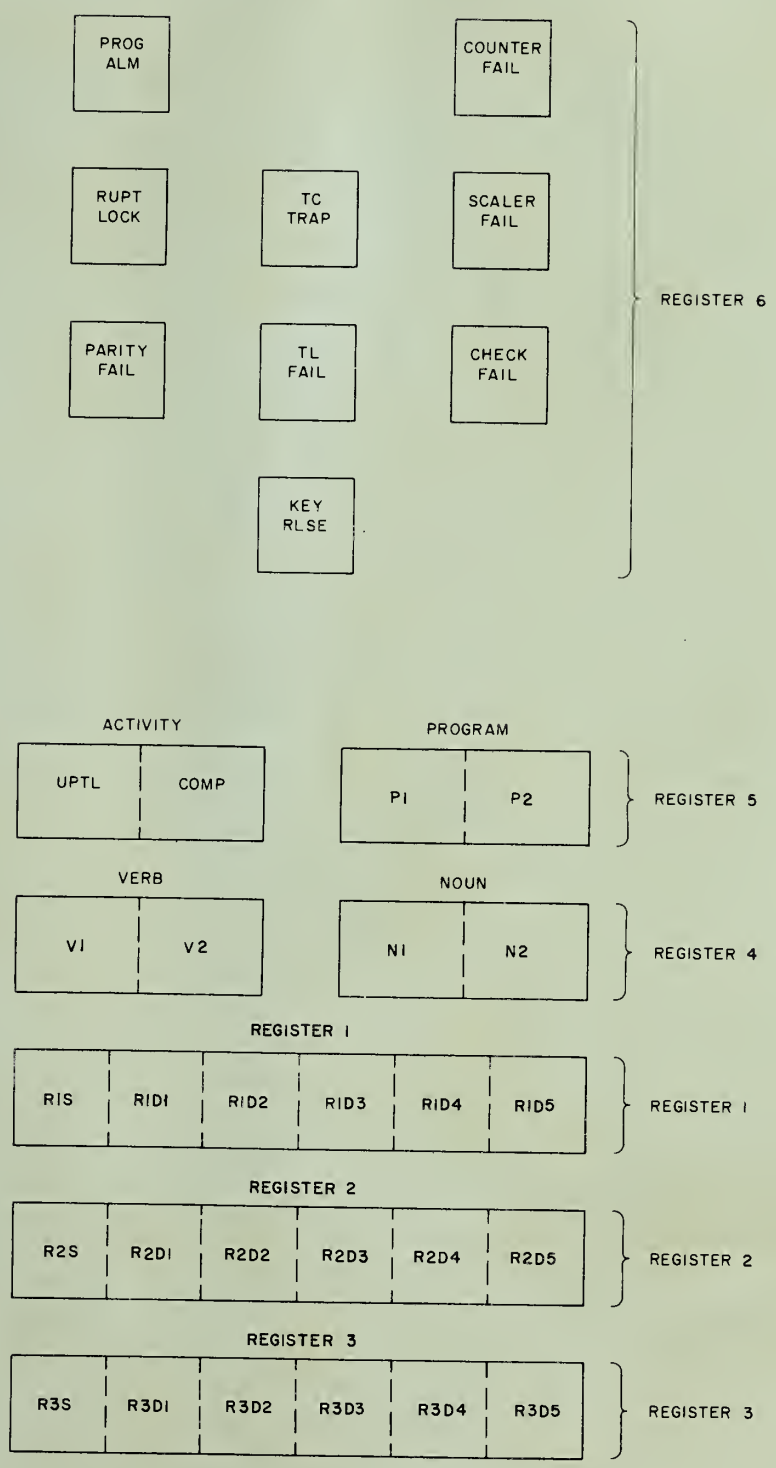
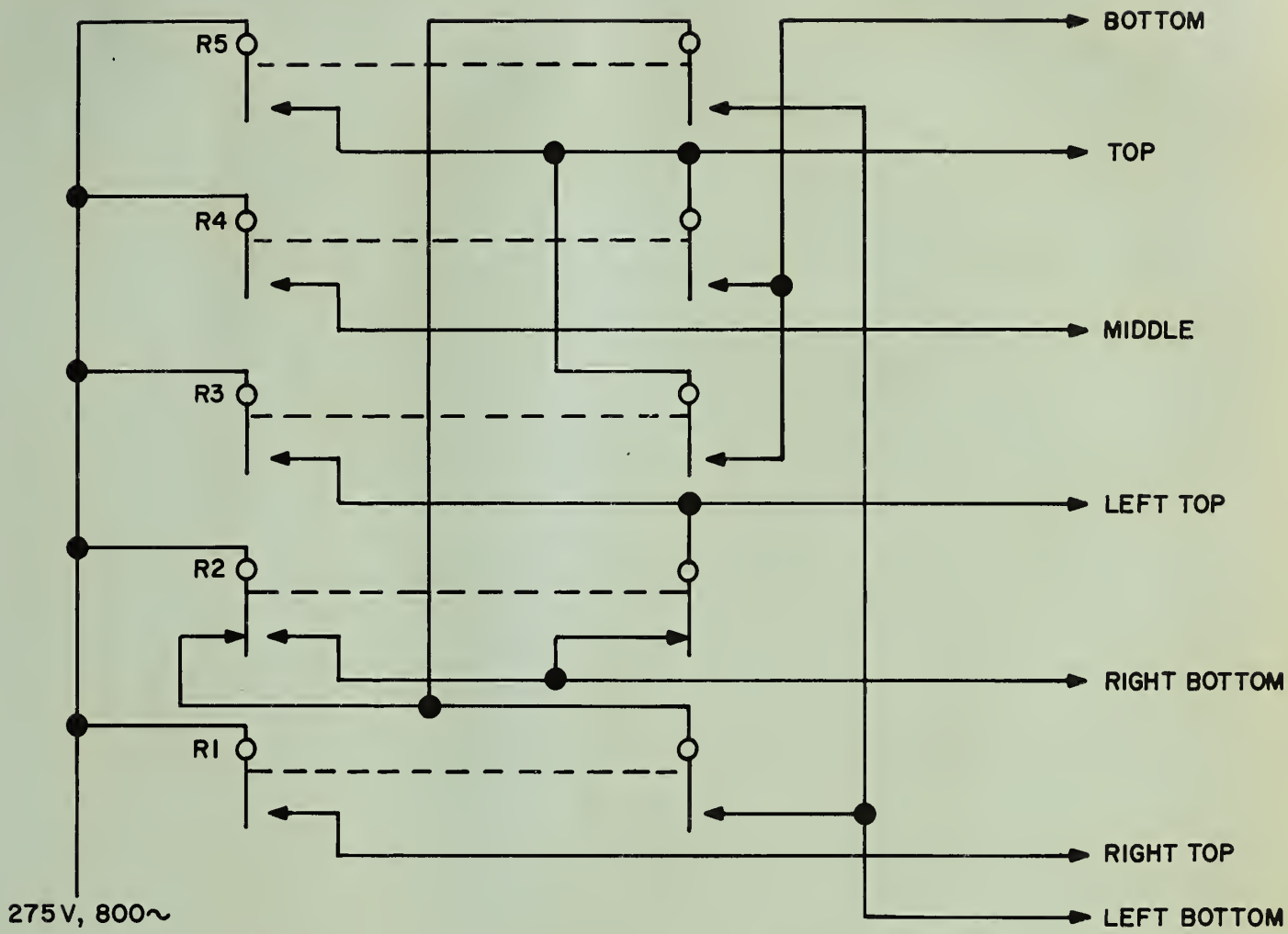
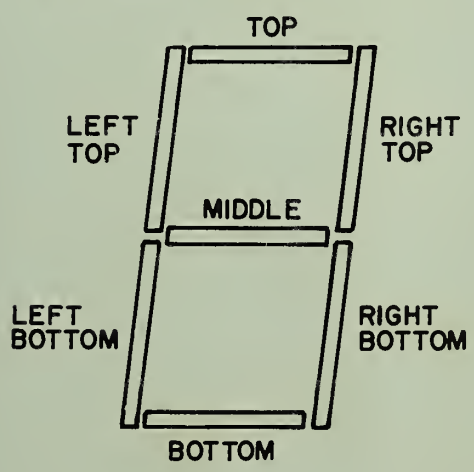


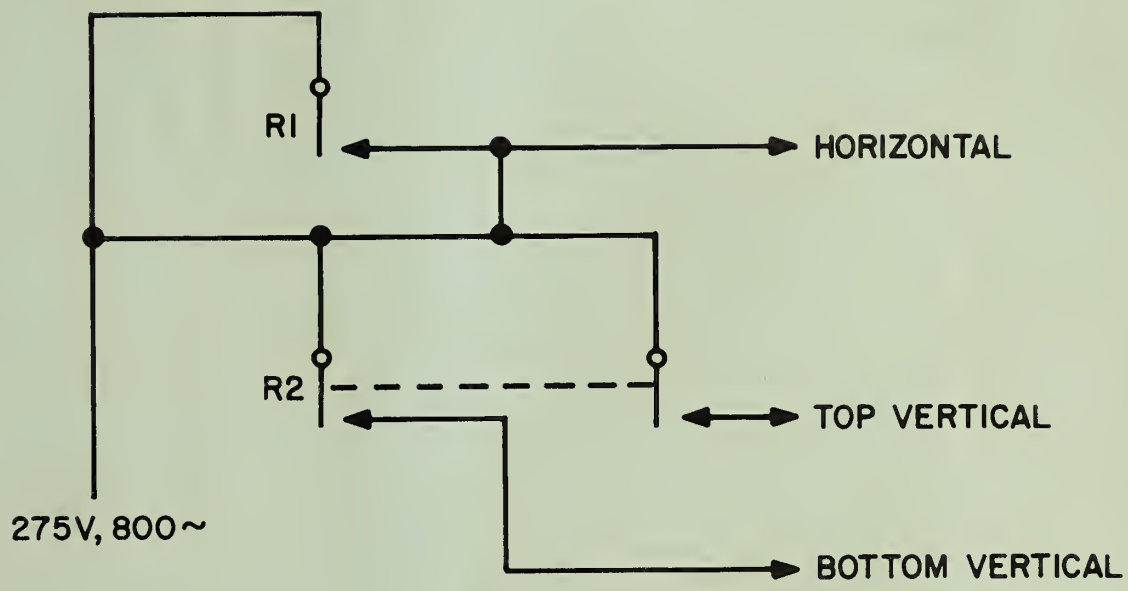
Figure 15-4. Navigation Panel DSKY Indicators

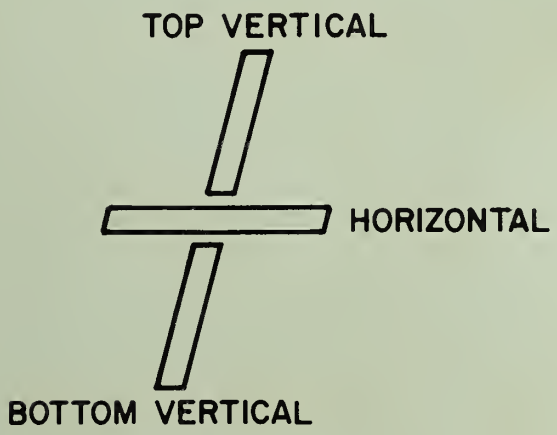




RELAYS					DIGIT
R5	R4	R3	R2	RI	DISPLAYED
1	0	1	0	1	0
0	0	0	1	1	1
1	1	0	0	1	2
1	1	0	1	1	3
0	1	1	1	1	4
1	1	1	1	0	5
1	1	1	0	0	6
1	0	0	1	1	7
1	1	1	0	1	8
1	1	1	1	1	9

Figure 15-5. Digit Indicator Relay Logic





RELAYS		SIGN
R1	R2	DISLAYED
1	0	−
0	1	+

Figure 15-6. Sign Indicator Relay Logic

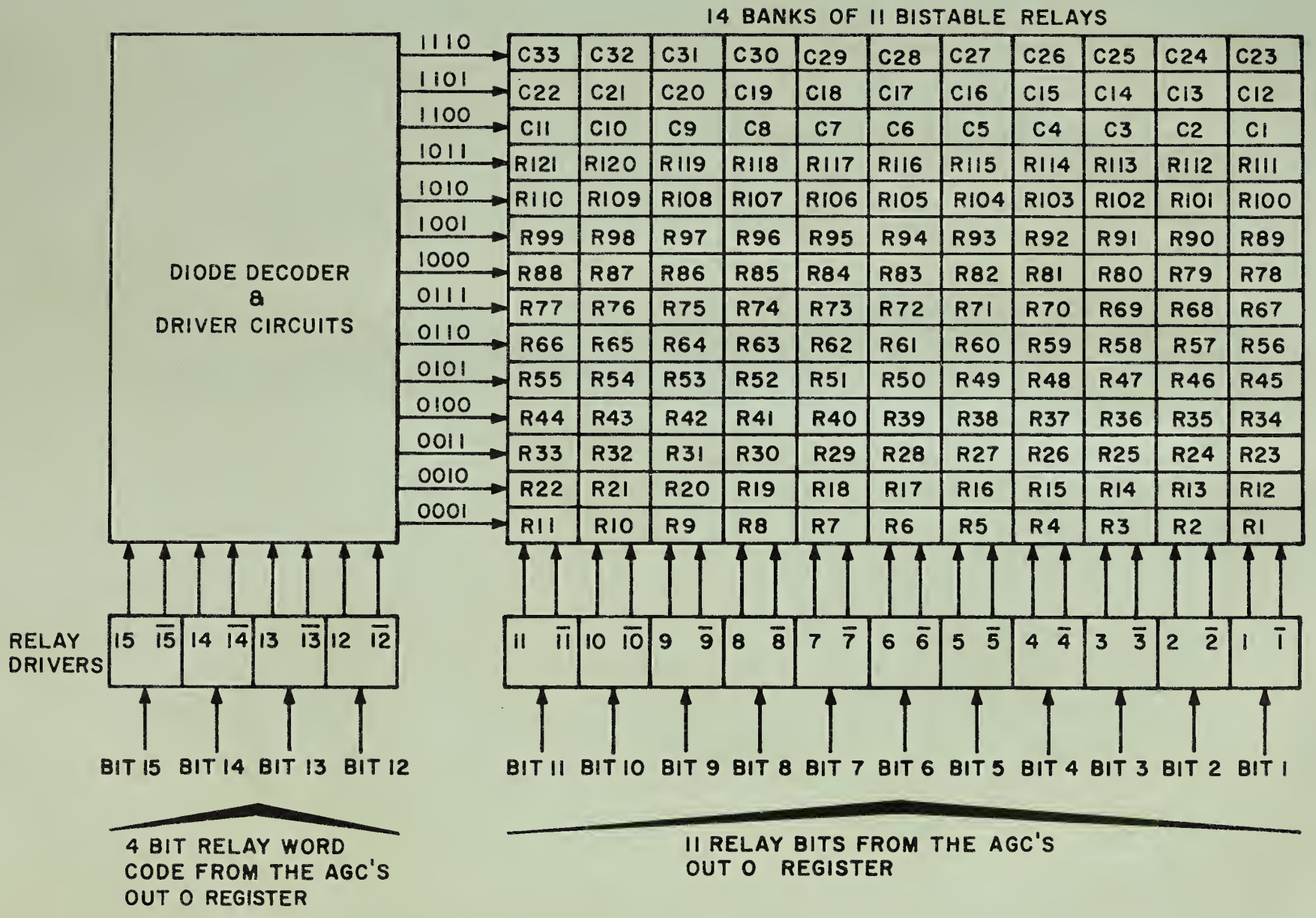


Figure 15-7. DSKY Read and Command Relay Circuitry

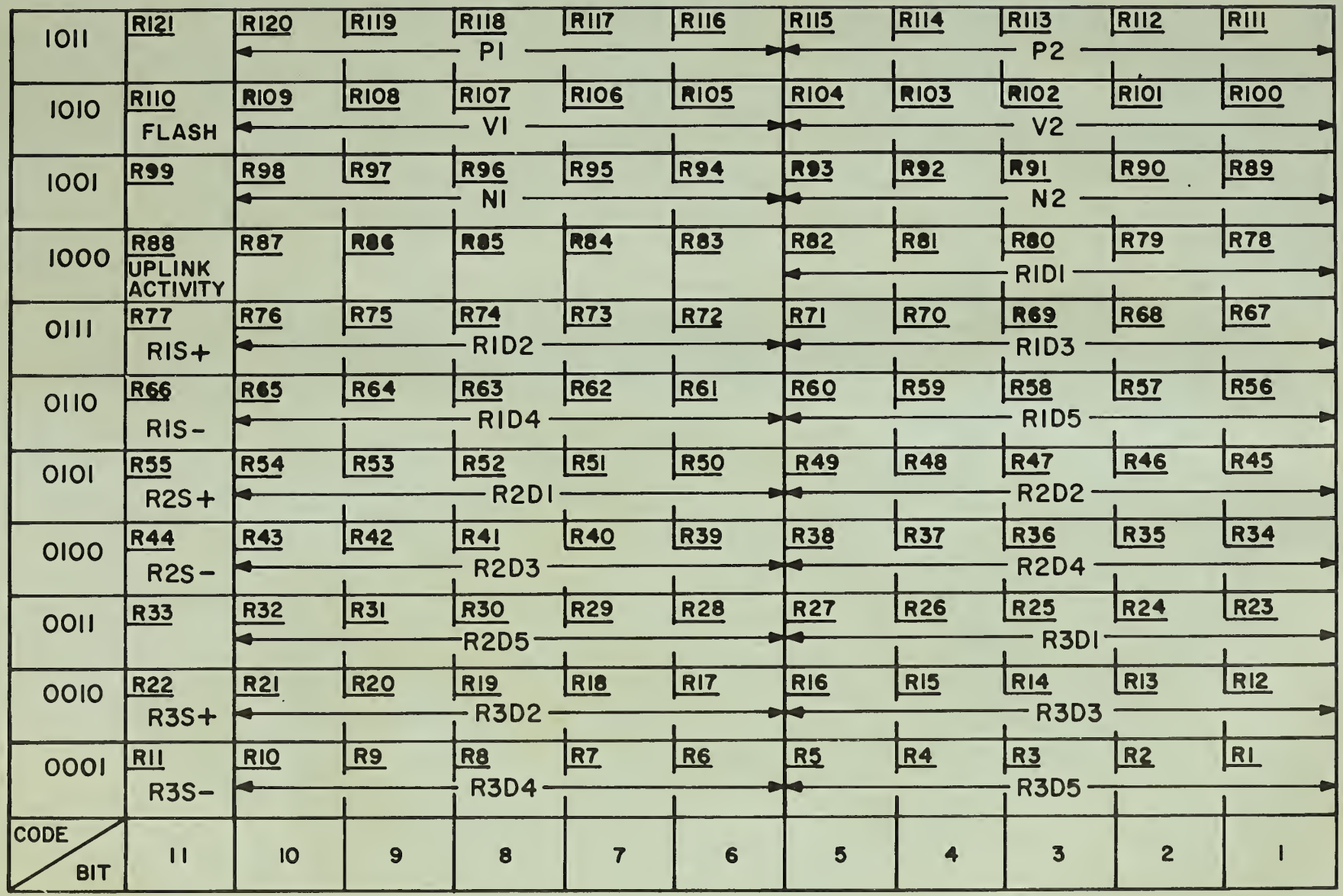


Figure 15-8. DSKY R Relay Usage

Relay R110 is associated with the VERB and NOUN displays. If this relay is set, a 1.3 cps signal will flash the VERB and NOUN displays. If relay R88 is set and the UP TL switch is in the ACCEPT position, the UPTL indicator will light.

15.4 MAIN PANEL DSKY DISPLAY

The main panel DSKY display consists of six registers (figure 15-9). Only Register 6 differs from its counterpart on the nav panel DSKY: the main panel DSKY has a COMP FAIL indicator in place of the eight alarm indicators on the nav panel DSKY. Figures 15-5 through 15-8 are valid for the main panel DSKY.

15.5 DSKY CONDITION AND ALARM INDICATORS

The nav panel DSKY contains eight alarm indicators and three condition indicators.

Alarm	Condition
1. PROG ALM (Program Alarm)	1. KEY RLSE (Key Release)
2. RUPT LOCK	2. UPTL (Uplink Telemetry)
3. PARITY FAIL	3. COMP
4. TC TRAP	
5. TL FAIL (Telemetry Failure)	
6. COUNTER FAIL	
7. SCALER FAIL	
8. CHECK FAIL	

The main panel DSKY contains one alarm indicator and three condition indicators. The condition indicators are the same as those on the nav panel DSKY. The alarm indicator is the COMP FAIL indicator.

Table 15-2 lists the alarm and condition indicators on the DSKY's and the states they represent if lighted. The DSKY's receive alarm and condition signals from the AGC's alarm circuits and OUT 1 register. The alarm signals from the OUT 1 register are CHECK FAIL, TELEMETRY FAIL and PROGRAM ALARM. The alarm signals from the AGC's alarm circuits are TC TRAP ALARM, RUPT LOCK ALARM, COUNTER FAIL ALARM, PARITY FAIL ALARM, and SCALER FAIL. The condition signals from the OUT 1 register are KEY RELEASE and COMPUTER ACTIVITY.

If the TEST ALARM key on the nav panel DSKY is pressed, signal TEST ALARMS (figure 15-3) is sent to the AGC and sets the COUNTER FAIL, RUPT LOCK, TC TRAP and PARITY FAIL alarm circuits. Signals COUNTER FAIL ALARM, RUPT LOCK ALARM, TC TRAP ALARM and PARITY FAIL ALARM are then sent to the DSKY's from the AGC. This causes the COMP FAIL indicator on the main panel DSKY and the corresponding indicators on the nav panel DSKY to light.

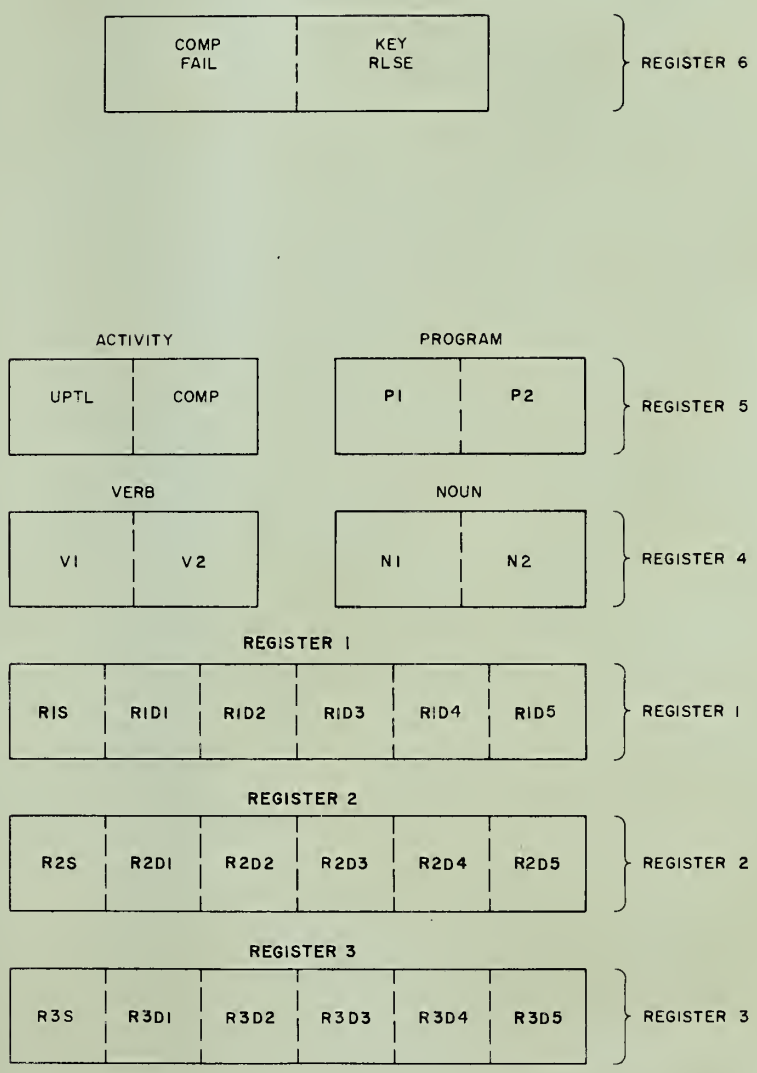


Figure 15-9. Main Panel DSKY Indicators

Table 15-2. DSKY Alarm and Condition Indicators

Indicator	Function
PROG ALM	Indicates procedural problems in the execution of the AGC's program.
PARITY FAIL	Indicates that data has been incorrectly transferred from memory.
CHECK FAIL	Indicates an illegal DSKY operation (usually caused by an operator error).
COUNTER FAIL	Indicates a failure in the normal sequence of input pulse counting.
RUPT LOCK	Indicates that the AGC has been in an interrupted state too long or that an interrupt has not occurred within a specified time.
TC TRAP	Indicates that the AGC is in an endless loop of instructions or has not transferred control within a specified time.
SCALER FAIL	Indicates a failure of the AGC's timing circuitry.
TL FAIL	Indicates: 1. Downlink word rate too high or too low. 2. Uplink bit rate too high or incorrect transmission of data.
KEY RLSE	Indicates that an internal program wishes to display information on the DSKY but has found the keyboard in use by the operator.
UPTL	Indicates that uplink telemetry data is present and that the UP TL switch is in the ACCEPT position.
COMP	Indicates that the AGC is in a program other than "dummy job".
COMP FAIL	Indicates the logical OR of the first seven alarm indicators in this list.

The ERROR RESET key is pressed whenever the COMP FAIL indicator is on. This key may be used to test for the presence of a transient rather than a continuous alarm in the AGC. The associated keycode disables the alarm circuits associated with the OUT 1 register. In addition to a keycode, the ERROR RESET key initiates a signal which resets the AGC alarm circuits set by the TEST ALARMS signal. This extinguishes the COMP FAIL, COUNTER FAIL, RUPT LOCK, TC TRAP and PARITY FAIL indicators.

Figure 15-10 shows the circuitry associated with the alarm and condition indicators on the nav panel DSKY. The relays are non-latching. Figure 15-11 is a drawing of comparable circuitry in the main panel DSKY.

15.6 DSKY POWER SUPPLY

Each DSKY contains a power supply. These power supplies produce 275V, 800 cps power in lighting the various electro-luminescent lamps. In generating this display power, the DSKY power supply uses inputs from the +13 VDC AGC power supply, the +28 VDC prime power supply and the 800 pps sync signal from the AGC.

15.7 SUMMARY

The DSKY keyboards are used to insert data into the computer. When a key is pressed, a five bit code is applied to the AGC's IN 0 register. Each DSKY display consists of six registers. These registers, in turn, consist of sign, digit, alarm and condition indicators. A number or sign can be formed on an indicator by lighting the proper combination of electro-luminescent lamps. This lamp configuration is determined by the AGC's OUT 0 register.

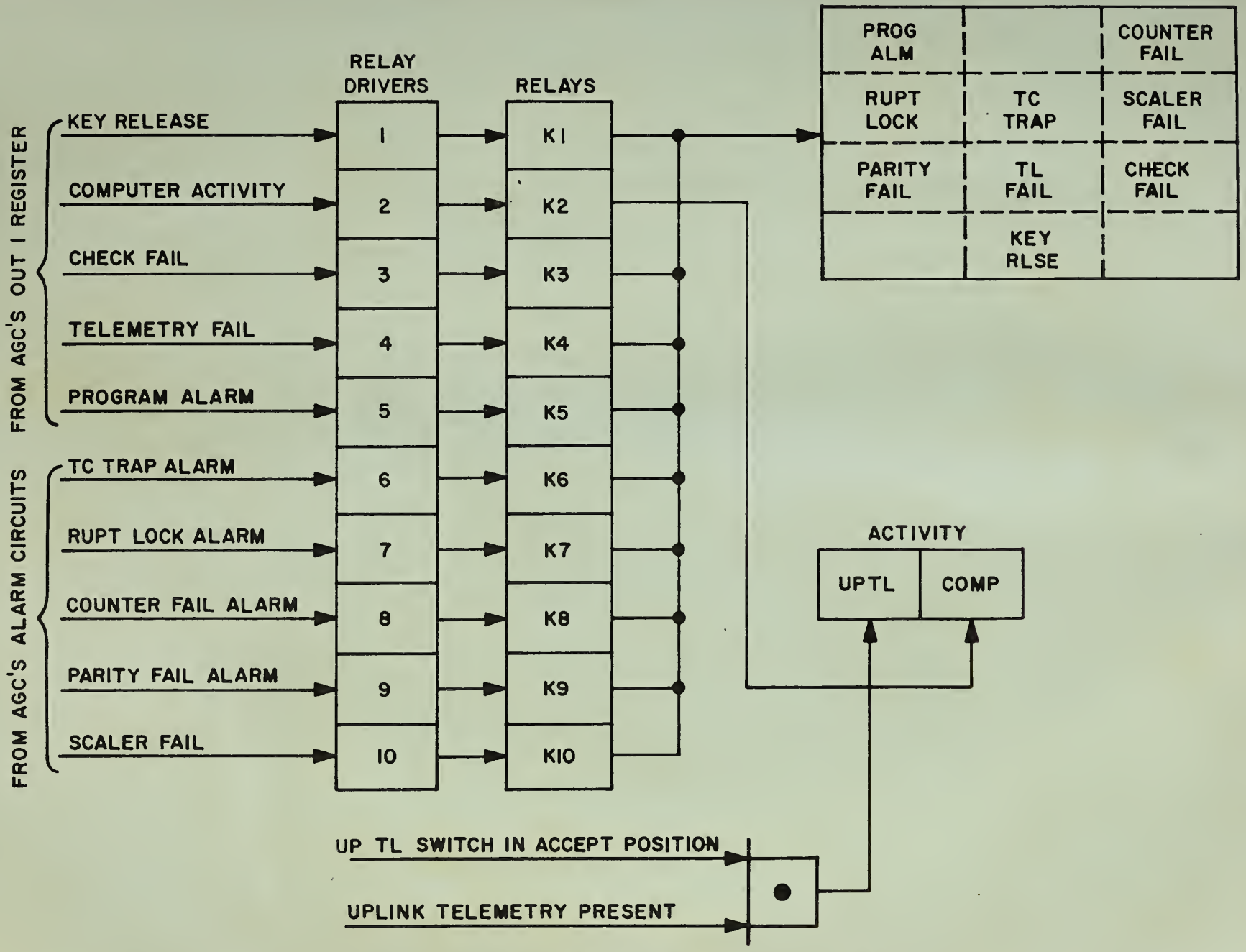


Figure 15-10. Navigation Panel DSKY Alarm Circuitry

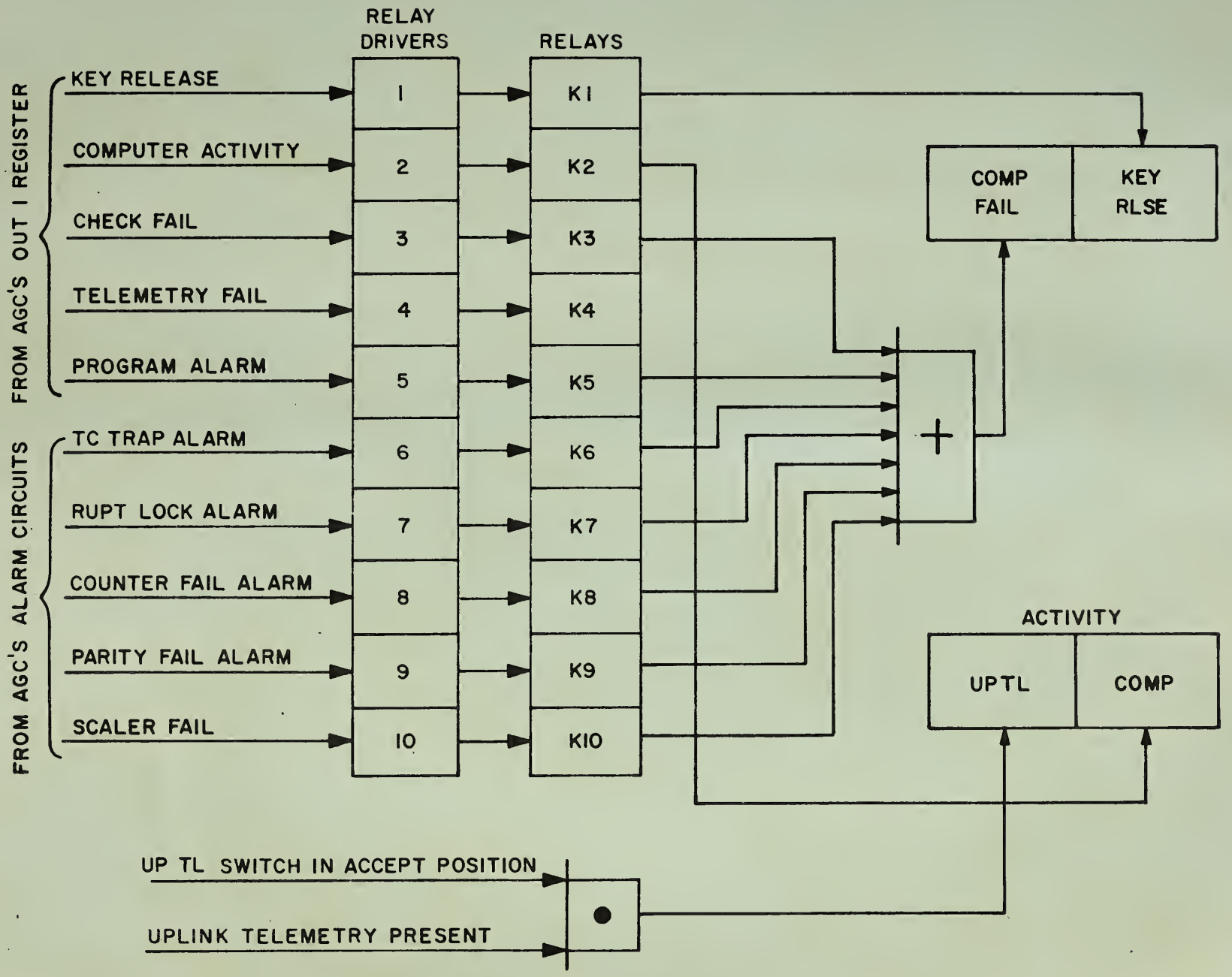


Figure 15-11. Main Panel DSKY Alarm Circuitry

REVIEW QUESTIONS FOR SECTION XV

T F 1. The alarm indicators receive inputs from the AGC's OUT 0 register.

2. Which indicator will light if the AGC wishes to display information on the DSKY's?

T F 3. A keycode is associated with every DSKY key.

4. Where is the UP TL switch located?

T F 5. The TELEMETRY FAIL signal from the AGC will light the COMP FAIL indicator on the main panel DSKY.

SECTION XVI

DSKY OPERATIONAL PROCEDURE

INTRODUCTION

This section describes the procedures used for operating the DSKY's. A list of VERB and NOUN codes are provided for reference. Additional information on computer operation is provided in the Computer Programing Course C1100.

16.1 CSS/ASTRONAUT

The CSS interface with the astronaut is through the DSKY's. The operator of the DSKY can communicate with the AGC by the depresssion of a sequence of keys on the DSKY keyboard. Each depression of a key inserts a five bit code into the AGC. The AGC responds by initiating an internal action or returning a code to the DSKY which controls an indicator on a particular display. The AGC can, under its own control, initiate a display of information or request an action to the operator.

The basic communication language used in this interchange of information is a pair of words known as the VERB and NOUN. Each of these words is represented by a two digit octal code. The VERB code specifies that an action of some sort is to be performed. The NOUN code, which is used in conjunction with the VERB code, specifies on what the action is to be performed. An example of a VERB-NOUN code combination is given below:

VERB 16 -- MONITOR IN DECIMAL ALL COMPONENTS OF -- NOUN 21 -- PIPAS

This combination of VERB-NOUN codes causes the accumulation of PIPA counts (as accumulated by the AGC) from each of the PIPAS to be displayed in REGISTER 1 (R1), REGISTER 2 (R2) and REGISTER 3 (R3).

The standard procedure of inserting the VERB-NOUN codes into the keyboard is the sequential depression of seven keys. Using the VERB-NOUN codes previously discussed, the sequence of key depressions is as follows:

1. VERB
2. 1
3. 6
4. NOUN
5. 2
6. 1
7. ENTER

Depressing ENTER key indicates to the AGC that it should perform the operation indicated by the VERB-NOUN codes.

An alternate sequence of key depressions, which would accomplish the same insertion of information, is as follows:

1. NOUN
2. 2
3. 1
4. VERB
5. 1
6. 6
7. ENTER

Whenever the VERB key is pressed, the two VERB display panels are blanked. Then, as the digits of the VERB code are keyed in, the digits are displayed in the two VERB display panels. For example:

VERB key pressed -- VERB display panels V1 and V2 blanked

1 key pressed -- 1 displayed in V1

6 key pressed -- 6 displayed in V2

Whenever the NOUN key is pressed, the two NOUN display panels are blanked. As the two digits of the NOUN code are keyed in, the NOUN display panels display the digits of the NOUN code.

If the VERB-NOUN codes, displayed in the VERB-NOUN display panels, are those desired for the next entry of information, the VERB-NOUN codes need not be keyed in again. All that is required is the depression of the ENTER key. This indicates to the AGC to use these codes again.

Prior to pressing the ENTER key, after entering the proper VERB-NOUN codes, the VERB-NOUN codes should be verified. If they are not verified, the wrong action could be initiated which might cause damage to the overall system operation.

Some VERB-NOUN codes require more information than the VERB-NOUN codes to be keyed in. If more data is required after the depression of the ENTER key, the VERB-NOUN display panels flash on and off at a 1.3 cps rate. These display panels continue to flash until all the necessary information associated with the VERB-NOUN code has been keyed in. For example, using VERB 21 (WRITE 1ST COMPONENT INTO) NOUN 17 (TIME IN SECONDS), the entry sequence is as follows:

1. VERB
2. 2
3. 1
4. NOUN
5. 1
6. 6
7. ENTER

After the ENTER key is pressed, the VERB-NOUN display panels flash 21 and 16 respectively. This indicates that more information is required. In this case, it is a time in seconds. Assuming that the time to be entered is +75.25 seconds, the entry procedure is as follows:

1. +
2. 0
3. 7
4. 5
5. 2
6. 5
7. ENTER

After the ENTER key is pressed, the VERB-NOUN display panels stop flashing and display VERB 21, NOUN 16. As the various keys are pressed while inserting the data, the digits are displayed in positions of one of the display registers, corresponding to the order in which they wer entered. For instance, when +75.25 seconds is being entered, the + key is pressed first and + is displayed in R1S (Register 1, Sign Digit). The 0 key is pressed and 0 is displayed in R1D1 (Register 1, Digit 1). The 7 key is pressed and 7 is displayed in R1D2. This continues until the information is completely keyed in. Pressing the ENTER key, after keying the desired information, not only stops the flashing of the VERB-NOUN displays but indicates to the AGC that it should proceed and perform the specified operation.

VERB 21 (WRITE 1ST COMPONENT INTO), 22 (WRITE 2ND COMPONENT INTO), 23 (WRITE 3RD COMPONENT INTO), 24 (WRITE 1ST AND 2ND COMPONENTS INTO) and 25 (WRITE 1ST, 2ND AND 3RD COMPONENTS INTO) are used to enter one, two or three components or portions of data into the AGC. For example, when VERB 25 (WRITE 1ST, 2ND AND 3RD COMPONENTS INTO) is entered, the VERB display will illuminate and display 25. When the ENTER key is pressed after keying in the NOUN code, VERB 21 (WRITE 1ST COMPONENT INTO) will be displayed and flashing. After the first component has been keyed in and displayed in R1 and the ENTER key pressed, VERB 22 (WRITE 2ND COMPONENT INTO) will be displayed and flashing. After the second component has been keyed in and displayed in R2 and the ENTER key pressed, VERB 23 (WRITE 3RD COMPONENT INTO) will be displayed and flashing. After the third component is entered and displayed in R3 and the ENTER key is pressed, the VERB display stops flashing and displays VERB 25. The AGC then proceeds to use the information entered.

Any time prior to pressing the ENTER key for the last time in the loading sequence, i.e., the ENTER after the third component was inserted in the previous paragraph, erroneous information can be corrected. To correct erroneous data, the CLEAR key is used. This key causes R1, R2 or R3, last loaded, to be cleared and also clears the corresponding information loaded into the AGC. For example, if a three component load is being keyed in and it is discovered that an error exists in R1 after R3 has been loaded but prior to the last enter, the following must be done to correct the data:

Press CLEAR key - - R3 blanked (VERB 23 remains displayed)

Press CLEAR key - - R2 blanked (VERB 22 is displayed)

Press CLEAR key - - R1 blanked (VERB 21 is displayed)

Reload R1, R2 and R3

The CLEAR key is <u>not</u> used to clear the VERB, NOUN or PROGRAM displays.

Decimal and octal displays or loadings are distinguished by use of the + and - displays or key inputs. Whenever decimal data is to be loaded, the + or - key must be depressed prior to keying in the digits of the data to be loaded. If the sign keys are not used, the data is assumed to be octal by the AGC. Whenever data is displayed using a + or -, the displayed data is in decimal. Otherwise, when the sign is not used and R1S, R2S or R3S are blanked, the data is in octal.

Whenever a display type VERB is used, the requested data is transferred to the DSKY display panels only once for every time the data is requested. Monitoring type VERBS, in contrast, are periodically updated, and the display of the requested data changes as the requested data in the AGC changes. The updating of the displayed data for a monitor type VERB is accomplished approximately every 1/2 second.

The major mode refers to system operations in the various phases of a flight or while operating on the ground. Examples of major modes are: system test, prelaunch alignment, etc.

In order to request that the system initiate one or more of these major modes of operation, a different sequence of entering information through the DSKY is required. The procedure is as follows using VERB 37 (CHANGE MAJOR MODE TO):

1. VERB
2. 3
3. 7
4. ENTER

When the ENTER key is pressed, after keying in VERB 37, the VERB display panels flash and the NOUN display panels are blanked. Now the two digit octal code for the desired major mode and phase of the major mode can be entered through the keyboard. As the appropriate keys are pressed, the digits of the code are displayed in the PROGRAM display panels. When the ENTER key is pressed after keying in the two code digits, the major mode code is displayed in the two PROGRAM display panels P1 and P2. If the operator wants to initiate the major mode prelaunch alignment which uses code 01, the following keying must be used:

1. VERB
2. 3
3. 7
4. ENTER
5. 0 entry, for prelaunch alignment mode request
6. 4 entry, indicating phase to enter prelaunch alignment
7. ENTER

The PROGRAM display panels now display 01.

Another group of VERBS enables the operator to initiate system tests and modes of operation. Examples of these are:

PERFORM GYRO DRIFT TEST - - VERB 70

FINE ALIGN IMU - - VERB 42

ZERO - - VERB 40

Some of these VERBS do not require an associated NOUN code. For example, if the gyro drift test is to be initiated, the procedure is:

1. VERB
2. 7
3. 0
4. ENTER

This causes the system to enter the gyro drift test. Other VERBS do require NOUN codes, e.g., VERB 40 (ZERO). This VERB refers to CDU's and the NOUN code required with this VERB code specifies either the inertial or optical CDU's (NOUN 20, inertial CDU's; NOUN 55, optical CDU's). If it is desired to ZERO the inertial CDU's, the keying procedure is:

1. VERB
2. 4
3. 0
4. NOUN
5. 2
6. 0
7. ENTER

Display and monitoring of various data can be accomplished by the AGC on its own initiative, without requests for the data by the operator. The appropriate VERB-NOUN codes are displayed with the data so that it can be properly identified and used by the operator. Whenever the AGC has initiated the display or monitoring of some data, the data is displayed for at least 10 seconds. After this time duration, the AGC is free to change the data displayed, if it so desires.

The AGC is also capable of requesting the operator to perform an action. The action that is requested is usually specified by a combination of VERB-NOUN codes and additional information displayed in one or more of registers R1, R2 and R3. For example, if VERB 50 (PLEASE PERFORM) NOUN 25 (CHECKLIST) is displayed in the VERB-NOUN display panels, R1 will display a numerically coded checklist item. When the operator has performed the requested action, the ENTER key is pressed. This indicates to the AGC that the operation has been completed. If the operator does not wish to perform the action requested, he may use VERB 33 (PROCEED WITHOUT DATA) or VERB 34 (TERMINATE). These VERB codes indicate to the AGC to continue without the data or requested action as best it can or to terminate the function it is trying to do.

While the operator of the DSKY is using the DSKY to load, display, etc., the AGC cannot interrupt this process. An interlock is set up by the AGC inhibiting itself from using the DSKY. Therefore, the DSKY operator should remove this interlock when he is finished using it. This is accomplished by pressing the KEY RELEASE key.

The AGC is capable of requesting that the DSKY operator release the DSKY so the AGC may use it. This indicates that the AGC has some data to display to the operator. It is accomplished by illuminating the KEY RELEASE indicator on the DSKY display. The operator does not have to release control of the DSKY if he wishes to continue to use it.

As previously mentioned, when the AGC has initiated a display of data, the data is displayed for at least 10 seconds before the AGC is able to display different data. This is an interlock the AGC imposes on itself to enable the operator time enough to read the data displayed. After 10 seconds have elapsed, the AGC drops the interlock and is free to display different data to the operator.

16.2 VERB-NOUN LIST

Contained in this section of the study guide is a complete listing of the VERB and NOUN codes. A brief description is also given for each of the VERB and NOUN codes along with the scaling of the data converted and displayed on the DSKY as a result of NOUN code usage. Keep in mind that many combinations of these codes exist; however, some of the combinations are non-sensical or illegal. Some VERB codes do not require a NOUN code to completely specify the desired action.

16.2.1 VERB CODES. The VERB codes are divided into two groups - Ordinary and Extended VERBS. The ordinary verbs generally are involved in the manipulation (loading display, etc.) of data. The extended verbs, in general, are used for initiation of actions such as moding requests.

16.2.1.1 Ordinary Verbs

Verb Code	Function	Display Location
00	Illegal	
01	Display (in octal) 1st component of:	R1
02	Display (in octal) 2nd component of:	R1
03	Display (in octal) 3rd component of:	R1
04	Display (in octal) 1st and 2nd components of:	R1, R2
05	Display (in octal) 1st, 2nd and 3rd components of:	R1, R2, R3
06	Display (in decimal) all component(s) of:	As appropriate
07	DP decimal display	R1, R2
10	Enter Request to Waitlist	
11	Monitor (in octal) 1st component of:	R1
12	Monitor (in octal) 2nd component of:	R1
13	Monitor (in octal) 3rd component of:	R1
14	Monitor (in octal) 1st and 2nd components of:	R1, R2
15	Monitor (in octal) 1st, 2nd and 3rd components of:	R1, R2, R3
16	Monitor (in decimal) all component(s) of:	As appropriate
17	Monitor DP decimal	R1, R2
20	Enter Request to Executive	
21	Write 1st component into:	R1
22	Write 2nd component into:	R2
23	Write 3rd component into:	R3
24	Write 1st and 2nd components into:	R1, R2
25	Write 1st, 2nd and 3rd components into:	R1, R2, R3
26	Spare	
27	Spare	
30	Spare	
31	Bank Display	R1
32	Bump Displays c(R2) into R3, c(R1) into R2	
33	Proceed without Data	
34	Terminate	
35	Release Display System	

Verb Code	Function	Display Location
36	Fresh Start	
37	Change Major Mode to:	

16.2.1.2 Extended Verbs

40	Zero (used with noun ICDU or OCDU only)	
41	Coarse Align (used with noun ICDU or OCDU only)	
42	Fine Align IMU	
43	Lock IMU	
44	Set IMU to Attitude Control	
45	Set IMU to Re-entry Control	
46	Return IMU to Coarse Align	
47	Spare	
50	Please Perform (Flash)	
51	Please Mark (Flash)	
52	MARK Reject	
53	Free (used with noun ICDU or OCDU only)	
54	Pulse Torque GYRO's	
55	Align	
56	Perform Banksum	
57	Do System Test	
60	Prepare for Standby	
61	Recover from Standby	
62	Spare	
63	Spare	
64	Calculate Orbital Parameters	
65	Calculate Time of Arrival at Longitude	
66	Calculate Latitude and Longitude at Specified Time	
67	Calculate Maximum Declination and Time of Arrival	
70	Perform GYRO Drift Test	
71	Perform PIPA Scale Test	
72	Spare	
73	Return to Earth Aim Point Update	
74	Orbit Change Aim Point Update	
75	Spare	
76	Spare	
77	R, V, T Update	

16.2.2 VERB DESCRIPTIONS.

16.2.2.1 Ordinary Verbs

Verbs 01-05	Perform octal displays of data.
Verb 06	Performs decimal display of data. The scale factors, types of scale factor routines and component information are stored within the machine for each Noun which is required to display in decimal.
Verb 07	Performs a double precision decimal display of data. It does no scale factoring. It merely performs a 10 character fractional decimal conversion of two consecutive erasable registers using R1 and R2 (the sign is placed in the R1 sign position; the R2 sign position is blank). It cannot be used with Mixed Nouns. Its intended use is primarily with "Machine Address to be Specified" Nouns.
Verb 10	Enters request to Waitlist Routine for any machine address with any delay. This Verb assumes that the desired number of 10 millesecond units of delay has been loaded into the low order bits of the Prio/ Delay register (Noun 26). This Verb is used with the "Machine Address to be Specified" Noun. The complete address of the desired location is then punched in.
Verbs 11-17	Update data displays every one-half second.
Verb 20	Enters request to Executive Routine for any machine address with any priority. This Verb assumes that the desired priority has been loaded into bits 10-14 of the Prio/ Delay register (Noun 26). This Verb is used with the "Machine Address to be Specified" Noun. The complete address of the desired location is then punched in.
Verbs 21-25	Perform data load. Octal quantities are unsigned. Decimal quantities are preceded by a + or - sign.
Verb 31	Bank Display. This Verb is included to permit displaying the contents of fixed memory in any bank. Its intended use is for checking program ropes and the BANK position of program ropes.
Verb 32	Display Shift. Useful for preserving an existing display of a quantity while displaying another quantity.

Verb 33 — Proceed Without Data. Informs routine requesting data to be loaded that the operator chooses not to load fresh data, but wishes the routine to continue as best it can with old data. Final decision for what action should be taken is left to requesting routine.

Verb 34 — Terminate. Informs routine requesting data to be loaded that the operator chooses not to load fresh data, and wishes the routine to terminate. Final decision for what action should be taken is left to requesting routine. If Monitor is on, it is turned off.

Verb 35 — Releases Keyboard and Display System for internally initiated use. Performs the same function as the Key Release button. It is included for use with those early keyboard which have no Key Release button.

Verb 36 — Initializes the program control software and Keyboard and Display System Program.

Verb 37 — Changes to New Major Mode.

16.2.2.2 Extended Verbs

Verb 40 — Must be used with Noun 20 (ICDU) or Noun 55 (OCDU) only. Sets the CDU counters to zero.

Verb 41 — Must be used with Noun 20 (ICDU) or Noun 55 (OCDU) only.

Verbs 42-47 — Call programs that perform the indicated G & N System procedure.

Verb 50 — This verb is used only by internal routines that wish the operator to perform a certain task. It should never be keyed in by the operator. It is usually used with Noun 25 (Checklist). The coded number for the Checklist Item to be performed is displayed in register R1 by the requesting routine.

Once the operator has performed the requested action, he should press ENTER to indicate that the Checklist Item has been performed. If he wishes not to perform the requested action, he should key in the Verb "Proceed Without Data".

Verb 51 — Verb 51 is used only by internal routines that wish the operator to MARK. It should never be keyed in by the operator. It is usually used with Noun 30 (Star Numbers). The numbers of the stars to be marked are displayed in registers R1, R2, R3 by the requesting routine.

Verb 52	Used to reject a bad "MARK".
Verb 53	Calls up programs that perform the indicated G&N System procedure. Used only with Nouns 20 and 55.
Verb 54	Calls up programs that perform the indicated G&N System procedures.
Verb 60	Prepares AGC for Standby Operation.
Verb 61	Prepares AGC for normal operation.
Verb 66	Performs calculations of latitude and longitude that spacecraft will attain at specified time.
Verb 67	Performs calculation of maximum declination and time at which maximum declination will be reached.
Verbs 70, 71	Calls programs that perform the indicated G&N System test.
Verb 73	Calls for calculation of new aim point for re-entry.
Verb 74	Calls for calculation of new aim point for orbit change.
Verb 76	Calls for calculation of new state vectors.

16.2.3 NOUN CODES. The NOUN codes are divided into two groups - normal and mixed nouns. The mixed nouns are those whose components refer to non-consecutive addresses or have different scale factors.

16.2.3.1 Normal Nouns

Noun Code	Function
00	Not in use.
01	Specify Machine Address (Fractional)
02	Specify Machine Address (Whole)
03	Specify Machine Address (Degrees)
04	Specify Machine Address (Hours)
05	Specify Machine Address (Seconds)
06	Specify Machine Address (GYRO Degrees)
07	Specify Machine Address (Y OPTICS Degrees)
10	Spare
11	Engine on Enable - used with please perform
12	ΔV Allowable
13	ΔV Measurement
14	ΔV Counter Setting
15	Increment Machine Address
16	Time Seconds
17	Time Hours
20	ICDU
21	PIPA's

Noun Code	Function
22	New Angles I
23	Delta Angles I
24	Delta Time (Seconds)
25	Checklist
26	Prio/Delay
27	Self Test On/Off Switch
30	Star Numbers
31	Failreg
32	Decision Time
33	Ephemeris Time
34	Event Time
35	Delta-Event Time
36	Delta-Event Time (Display only)
37	Spare
40	Gamma (γ) - inertial flight path angle Inertial Velocity (VI) Altitude Above Launch Pad (h_{pad})
41	Maximum Acceleration (G_{max}) Perigee Altitude (h_p) Free-Fall Time (t_{ff})
42	Miss Distance (ΔR) Perigee Altitude (h_p) Free-Fall Time (t_{ff})
43	Perigee Altitude (h_p) Apogee Altitude (h_a) Free-Fall Time (t_{ff})
44	Latitude Longitude Altitude (above spherical earth)
45	Perigee Altitude (h_p) Apogee Altitude (h_a) Delta-Velocity-Required (ΔV_{req})
46	Time-To-Event Velocity-To-Be-Gained (V_g) Perigee Altitude (h_p)
47	Flight Path Angle (γ) Miss Distance (ΔR)
50	Time-To-Event Delta-T-Burn

Noun Code	Function
51	Time-To-Event Velocity-To-Be-Gained (V_g) Measured Velocity Change Along X_{SC}
52	Time-To-Event Velocity-To-Be-Gained (V_g) Free-Fall Time (t_{ff})
53	Maximum Acceleration (G_{max}) Free-Fall Time (t_{ff})
54	Commanded Roll Angle (β) Present Acceleration (G)

16.2.3.2 Mixed Nouns

Noun Code	Function	
55	OCDU	X (SDA) Y (PDA)
56	Uncalled Mark Data	X (SDA) T (PDA)
57	New Angles OCDU	X (SDA) Y (PDA)
60	IMU Mode Status	IN 3 WASKSET OLDERR
61	Target Azimuth Elevation	
62	Delta-Velocity-Insert (ΔV_{ins}) Miss Distance (ΔR) Free-Fall Time (t_{ff})	
63	Spare	
64	Spare	
65	Sampled Time (Fetched in Interrupt)	
66	System Test Results	
67	Delta Gyro Angles	X Y Z
70	Pitch Trim Yaw Trim Delta-Velocity-Tail-Off	

Noun Code	Function
71	Spare
72	Delta Position
73	Delta Velocity
74	Spare
75	Delta Position Magnitude Delta Velocity Magnitude
76	R
77	V

16.2.3.3 Noun Scale Factors

The Keyboard and Display Routines are able to handle decimal/binary and binary/decimal scale factoring for the following situations:

1. fractional

2. whole

3. degrees (maximum ±359.99)

4. time in seconds (maximum +999.99)

5. time in hours (maximum +745.65).This may be used for display only. Loading of time in hours is not allowed.

6. GYRO degrees (maximum ± 9.9999)

7. Y OPTICS degrees. There are two different ranges, selected according to bit 13 of register WASOPSET. Bit 13 = 0 for range I; bit 13 = 1 for Range II. Range I maximum + 179.99 degrees, Range II maximum +89.999 degrees (in Range II a bias of 19.776 degrees is added for display; subtracted for loads).

In all cases, a single precision (5 decimal character) word is handled.

16.2.4 NOUN DESCRIPTIONS

16.2.4.1 Normal Nouns

Noun 00	Not in use.
Nouns 01-07	The machine address for these nouns is not stored within the machine, but is supplied by the operator. This allows any address to be loaded, displayed, or monitored. When ENTER is pressed with one of these nouns, the Flash is activated, but the Verb is left unchanged. This indicates to the operator that he should type in the 5 character OCTAL address, followed by an ENTER. It is displayed in R3, and the Flash is turned off. Thereafter, the execution of the Verb continues, just as in the case of any other noun. Seven different "Machine Address to be Specified" nouns are provided so that any of the decimal scale factors may be applied to the contents of any machine address.
Noun 15	This is used to increment the machine address already specified. It is useful for loading or displaying a group of consecutive addresses. OCTAL only.
Noun 16-17	These nouns refer to the time counters TIME 1, TIME 2, and are not normally loaded. If decimal is desired, Noun 16 gives seconds modulo 1000 (maximum +999.99 seconds); Noun 17 gives hours up to a machine maximum of 745.65 hours. *
Noun 20	This refers to the 3 ICDU counters. They are not normally loaded. If decimal is desired, the form is XXX.XX degrees (maximum of ± 359.99). *
Noun 21	This refers to the 3 PIPA counters, and is not normally loaded. In decimal, register contents are presented as whole decimal, representing the number of PIPA counts (maximum ±16,383).*
Noun 22	This refers to the desired platform angle registers (THETAD). (Decimal scale, ±359.99 degrees maximum.)
Noun 23	This refers to the Temporary Data Buffer. (Decimal scale ±359.99 degrees maximum.)

Noun 24 — This refers to the Temporary Data Buffer. (Decimal scale +999.99 seconds maximum.)

Noun 25 — Usually used with Verb 50, refers to Temporary Data Buffer. (If decimal is desired, whole scale is used.)

Noun 26 — This Noun is to be preloaded with the desired PRIORITY for use with VERB 20 (REQUEST EXECUTIVE); with the desired DELAY, when used with VERB 10 (REQUEST WAITLIST). OCTAL is to be used for the PRIORITY; decimal whole scaling is provided for the DELAY.

Noun 27 — + 0 loaded into this Noun causes the idle job to be done for Executive Backup.

-NZ loaded into this Noun causes the AGC Self Check routine to be done for the Executive Backup indefinitely.

+NZ loaded into this Noun causes the AGC Self Check routine to be done for the Executive Backup N times, where N is the number loaded. (If decimal is used, whole number scale.)

Noun 30 — Refers to the Temporary Data Buffer. Intended for star identification numbers. The decimal scale for each is whole. This Noun is usually used with Verb 51, described.

Noun 31 — Used to display system failure conditions. A coded number to identify the failure is displayed in R1. (Octal only.)

*Since this noun refers to counter registers, it is not normally loaded. However, the capability exists and loading may be useful in special applications.

16.2.4.2 Mixed Nouns

Noun 55 — Refers to the OCDU counters. (Decimal scale: X OPTICS scale is +359.99 degrees maximum. Y OPTICS scale is either +179.99 degrees maximum, or +89.999 degrees maximum. *)

Noun 56 — Refers to Temporary Data Buffer. Noun is used by internal routines to display the OCDU angles and time (seconds) when an unrequested MARK is performed. (Optics decimal scale is same as Noun 55.)

Noun 57 — Refers to the desired optics angle registers (DESOPTX, DESOPTY). (Optics decimal scale is same as Noun 55.)

Nouns 60-64 — Refers to each of the ICDU and OCDU counters separately, and time counter (in seconds). The ICDU decimal scales are ±359.99 degrees maximum. (Optics decimal scales are same as Noun 55.)*

Noun 65 — Refers to TIME 1, TIME 2 counters. (Decimal scales: hours scale, +745.65 maximum; seconds scale, +999.99 maximum. *)

Noun 66	Refers to Temporary Data Buffer. Decimal scales are whole, fractional, whole.
Noun 67	Refers to the desired delta GYRO angle registers (GYROD). Decimal scale is ±9.9999 degrees maximum.

* Since this noun refers to counter registers, it is not normally loaded. However, the capability exists and loading may be useful in special applications.

16.3 SUMMARY

The insertion of nouns and verbs into the computer is the basic communication method used to operate the computer. This display or monitoring of data can be initiated by the operator or by the computer. The computer is also capable of requesting the operator to perform an action.

The verb codes are divided into two groups - ordinary and extended. The noun codes can also be divided into normal and mixed nouns.

REVIEW QUESTIONS FOR SECTION XVI

T F 1. When the Noun pushbutton is depressed, the Noun display light displays the number of the Noun being loaded.

T F 2. Depressing the Clear Key pushbutton clears the Verb, Noun and R1, R2 and R3 registers.

T F 3. The computer may display data as often as every five seconds.

T F 4. If the computer requests the operator to load more information, the operator doesn't have to respond to the computer's request.

T F 5. Information may not be displayed without depressing the KEY RELEASE key.

APPENDIX

RELAY CONTROL OF MODE SWITCHING

The relays, diodes and 40 second timer are packaged in the PSA trays and D & C electronics. The method of controlling mode switching circuits depends upon the setting of the transfer switch to the manual or computer position. With the transfer switch in manual, relays K8 through K13 are used as latching relays to hold relays K1 through K5 energized after the mode pushbutton is released. Modes can be selected in any sequence. The selection of a new mode deenergizes the presently latched-in relay. The only inertial subsystem bi-stable relay, K13, is used in the entry mode. The bi-stable entry mode relay, K13, is used to prevent a change of state due to a momentary power failure in the critical entry mode. Since K13 is bi-stable, a reset K13 command must be generated when entering each of the other five modes. During computer control, the mode relays K1 through K5 are held energized by a continuous signal supplied by the AGC. The mode relays consist of more than one relay for each designation. For example, K1 consists of five different relays which are always energized together. Three of the K1 relays are in PSA Tray 6, the CDU zeroing transformer relays and entry relay module; one in PSA Tray 5, the CDU zeroing and lock relay module; and one in the display and control. Figure A-1 lists the number of relays for each designation and indicates when each relay is energized during either manual or computer control. The mechanization of the inertial subsystem IMU and CDU inner axis loop is shown in Figure A-2. The middle and outer loops are similar except for Relay K5. Switching mechanization is shown in Figure A-3.

IMU Turn On. Upon switching the inertial subsystem into the operate mode, prime power is applied to all the subsystem power supplied. The 40-second time delay starts its timing cycle (see Figure A-2), and relay K7 is energized, lighting the IMU delay lamp on the condition annunciator. Relay K2 is energized placing the system in the coarse align mode. Relay K12 may also be energized depending on the position of the transfer switch and the condition of K13. The purpose of the coarse align mode is to slave the IMU gimbals to the CDU's while the gyro wheels are coming up to speed. After a 40-second interval, K6 is energized by the 40-second time delay circuit. When energized, K6 deenergizes K7, which extinguishes the IMU delay lamp, and deenergizes K2 which switches the inertial subsystem from the coarse align mode. If the subsystem was in the entry mode prior to turn-on, K13 is set and the subsystem returns to the entry mode. Otherwise, all the relays except K6 and K12 are deenergized placing the subsystem in the attitude control mode configuration. This condition continues until one of the six modes is selected.

Zero Encoder. The purpose of this mode is to drive the CDU shaft angle to a zero position utilizing the CDU's 16X and 1/2X shaft resolvers. The zero encoder mode is selected manually by pressing the zero encoder pushbutton, S5, (see Figure A-3) which energizes relay K8. Relay K8 is latched in by a signal which is routed through S5, S6, S7, S8, S9, S10, K9, K10, K11 and K13. All switches must be open; all relays must be deenergized; and K13 must not be set. Upon releasing S5, the latch-in requirements are satisfied and K8 remains energized. If the system is in manual control, has been turned on for at least 40 seconds, and the zero encoder mode button is depressed, K1 (zero encoder relay) and K4 (fine align relay) will energize. The zero encoder lamp lights but the fine align lamp is disabled by K1. A signal is provided to disable the digital to analog converter since

it is receiving pulses from the encoder and could provide an output to the motor drive amplifier. In the zero encoder mode, K4 being energized prevents the digital to analog converter from driving the CDU. If the system is in computer control, a command which holds K1 and K4 energized is received from the AGC and the latch-in relay, K8, is not required. A discrete is sent to the AGC by contacts on K1 and K4 to indicate that they are energized.

In the loop used to drive the CDU's to zero, an 800 cps reference signal is applied through K1 to the stator winding of the 16X and 1/2X CDU resolvers. The 16X resolver rotor output is switched by K4 into the motor drive amplifier while the 1/2X CDU resolver is wired directly into the selector circuit. The motor drive amplifier output is applied as the control signal to the CDU servo motor which drives the CDU gear train and positions the resolvers. The sine winding of the 16X and 1/2X resolver rotors is used since the sine function goes to zero at a zero shaft angle. The maximum time required for zeroing is approximately 30 seconds.

Coarse Align. This mode slaves the IMU gimbals to the CDU shaft angles. It is entered by 4 possible means: 1) pressing the coarse align pushbutton with the transfer switch in "manual", 2) AGC command of coarse align with the transfer switch in "computer" and "coarse align" requested through the DSKY, 3) IMU turned on for less than 40 seconds when the IMU is first turned on from the main D & C panel, 4) system in the "manual CDU" mode and the manual align button depressed.

If the mode is entered by depressing the coarse align pushbutton, then K9 is latched in. With K9 energized, the system is manual control, and the IMU turned on for at least 40 seconds, then K2 is energized. The three other methods of entering coarse align energize K2 directly. With K2 energized, the lamp lights unless the system is in manual CDU mode. Relay K2 permits a discrete signal to be sent to the AGC indicating the system mode of operation.

The mechanization of the coarse align mode is shown in Figure A-3. Relay K2 is located in each of the three coarse align amplifiers (one amplifier for each axis). The input signal to the coarse align amplifier is received from the CDU's 1X resolver which has been positioned to the desired IMU gimbal angle. The stator of the gimbal 1X resolver is excited with an 800 cps reference signal routed through K1. The rotors of the IMU and CDU 1X resolvers are connected. When the two rotor angles differ, an error signal proportional to the sine of the angular difference is picked off the CDU resolver rotor and applied to the coarse align amplifier. The signal is amplified, demodulated and sent through the coarse align relay, K2, to the stabilization loop's torque drive amplifier (TDA). The output of the torque drive amplifier is the control signal for the gimbal torque motors which drive the gimbals until the gimbal 1X resolver angular position equals the CDU 1X resolver angle. The error signal from the CDU's 1X resolver is also applied to the IMU-CDU difference meter on the IMU control panel. A demodulator circuit is provided in the D & C electronics to change the 800 cps signal to a dc signal to drive the IMU CDU difference meter.

Manual CDU. This mode is used in conjunction with the manual align mode as a backup for IMU alignment to establish coarse alignment of the IMU. The mode is entered by one of the three following methods: 1) pressing the manual CDU pushbutton with the inertial subsystem in manual control, 2) by AGC command of the Manual CDU mode when the system is in computer control, 3) turning on the G & N sync on the main display and control panel. If the mode is entered by pressing the pushbutton, K10 is latched in. If the system is in manual control and the IMU has been turned on for at least 40 seconds, then K3 is energized and the lamp lights. A discrete indicating the mode of operation is sent to the AGC, also the digital to analog converter is disabled. With K10 latched in, the manual align switch is activated and, when pressed, energizes the coarse align relay, K2. The coarse align lamp

does not light since K3 is energized. The G & N sync switch on the main display and control panel energizes K3 independently of computer or manual control. The switch is used during the attitude control mode to lock the CDU's and hold the spacecraft at a preferred orientation obtained by the pilot by maneuvering the spacecraft with the rotational hand controller.

The mechanization of the manual CDU mode is shown in Figure A-2. In the mechanization diagrams, K3 removes the 28-volt, B+ power to the motor drive amplifier to prevent the motor drive amplifier output from positioning the CDU's. The slew switch can drive the CDU by applying B+ excitation and an 800 cps signal to the motor drive amplifier.

Fine Align. The purposes of this mode are to bring the stable member to fine alignment by pulsing the torque ducosyns of the stabilization gyros when a fine align is desired and to slave the CDU's to the IMU gimbal angles. The number of required pulses is calculated and issued by the AGC based on optical alignment measurements. The mode is entered by one of the following methods: 1) pressing the fine align button with the inertial subsystem in computer control, 2) application of fine align commands from AGC with the subsystem in computer control, 3) using the rotational hand controller when the G & N sync switch on the main display and control panel is in the "ON" position, thereby energizing the SCS relay, K2. If the mode is entered manually, K11 is latched in and the fine align relay, K4, is energized to light the fine align lamp, provide a discrete to the AGC, and provide a disable command to the digital to analog converter. When the G & N sync switch is turned on, K4 is energized if the stabilization and control system relay, K2, is energized. First, the stabilization and control system must be in the G & N attitude control mode. Second, the astronaut must be using the rotational hand controller to change the spacecraft attitude. With these conditions the CDU's are slaved to the IMU gimbal angles, and when a new attitude is established, the CDU angles provide the reference for holding the spacecraft's new orientation.

Attitude Control. In this mode, steering or attitude control signals are generated so that the IMU gimbal angles and CDU shaft angles remain equal. The attitude of the spacecraft is controlled by the position of the CDU's. The mode can be entered by one of two methods: 1) pressing the pushbutton with the subsystem in computer control, and 2) by AGC attitude control commands with the subsystem in computer control. Attitude control does not have a separate mode relay but is mechanized by deenergizing all the mode relays, K1 through K5. Relay K12, which is latched in by the other deenergized mode pushbuttons and relays, lights the mode lamp and sends a discrete to the AGC. If any of the other five modes are entered, K12 is deenergized.

The error signal used for attitude control is the 1X CDU resolver sine output and it is sent through K2 and the pitch-yaw resolver and fixed resolution transformer to the SCS for positioning of the service propulsion engine. The IMU to CDU errors are driven out by positioning the spacecraft about the stable platform. The computer may drive the CDU's in this mode.

Entry Mode. The purpose of the entry mode is to: 1) reduce the system response time for generating an error signal about the roll entry axis, and 2) to eliminate the fixed resolution transformer.

The mode is entered by two methods: 1) pressing the entry pushbutton with the inertial subsystem in manual control, 2) AGC commanding the entry mode with system in computer control. If the entry mode is entered manually, bi-stable relay K13 is set and holds the system in entry until reset. Whenever any other mode pushbutton is pressed, a reset command is issued. With K13 set, the system in manual control, and the IMU turned on for at least 40 seconds, K5 is energized so it lights the entry lamp and issues a discrete to the AGC. In addition, K5 switches the IMU 1X resolver to the CDU 16X resolver for increased response to attitude commands.

NUMBER OF RELAYS	5	4	2	4	3	1	1	1	1	1		1	1
MODE \ RELAY	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13
STAND-BY													
IMU TURN-ON LESS THAN 40 SECONDS		M					M						
ZERO ENCODE	C / M			C		C / M		M					
COARSE ALIGN		C / M				C / M			M				
MANUAL CDU		*	C / M			C / M				M			
FINE ALIGN				C / M		C / M					M		
ATTITUDE CONTROL						C / M						C / M	
ENTRY					C / M	C / M							M

M — MANUAL CONTROL

C — COMPUTER CONTROL

* CLOSED DURING MANUAL ALIGN

42070

Figure A-1. ISS Relay Chart

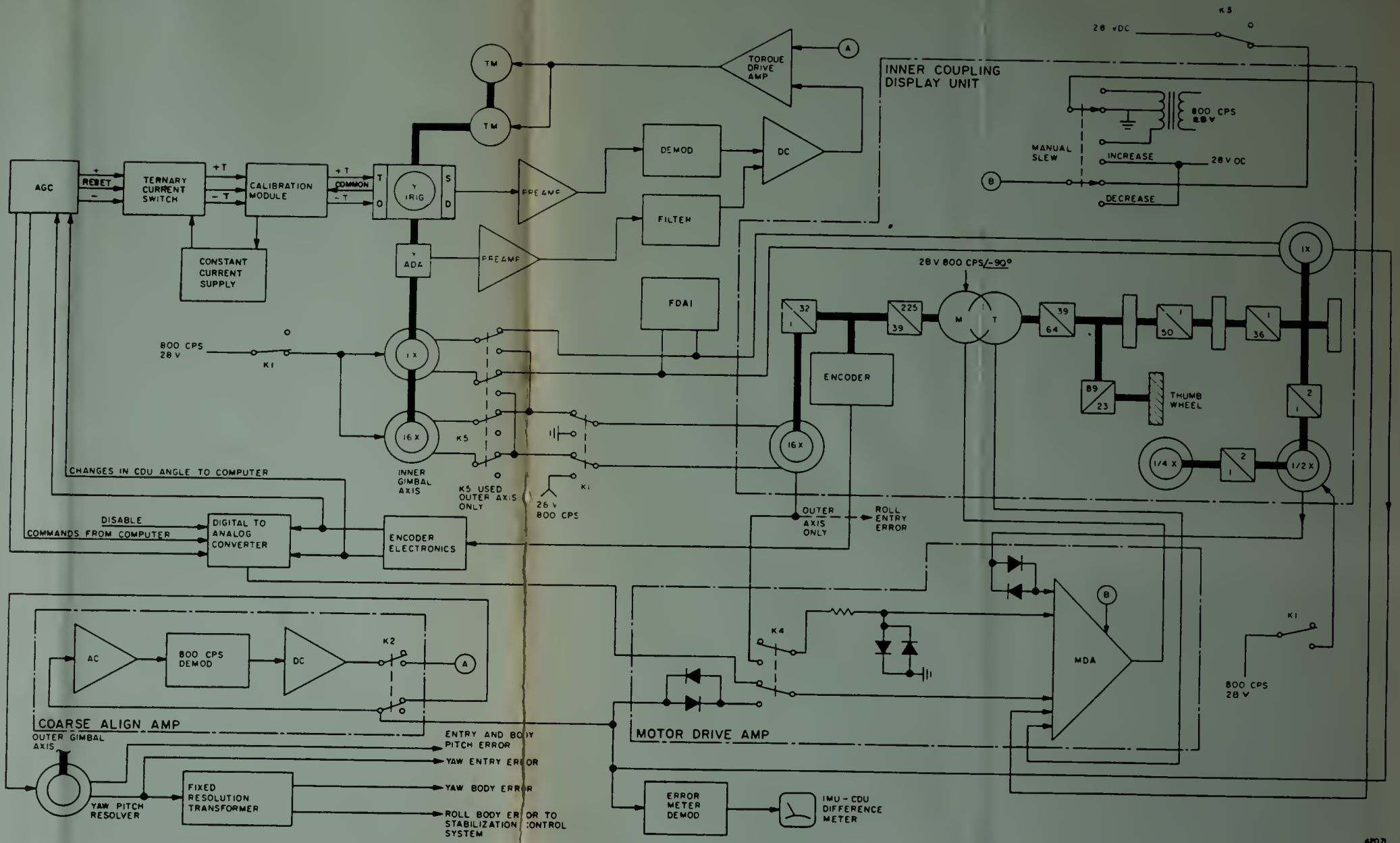


Figure A-2. Appendix IMU and CDU Inner Axis Mechanization

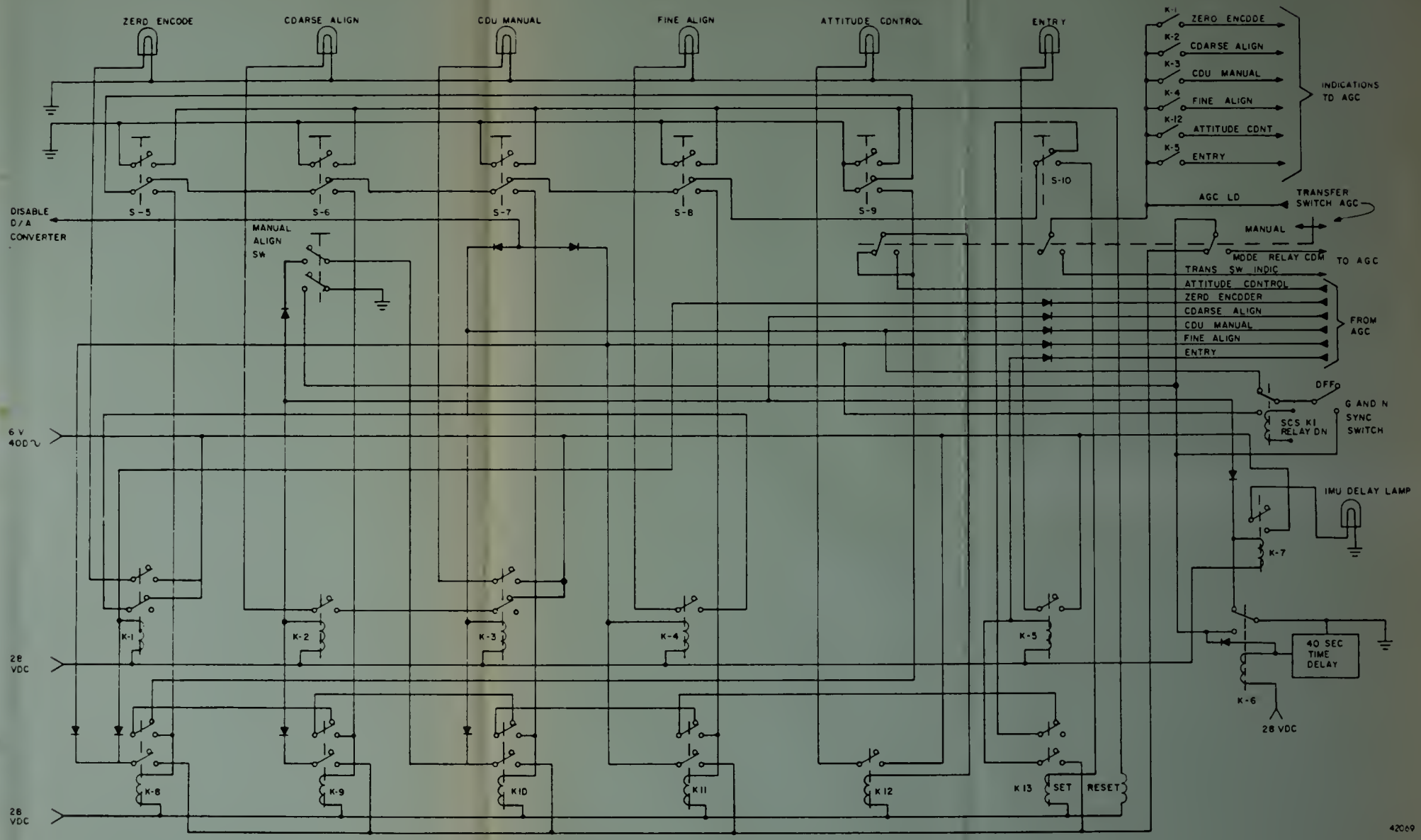


Figure A-3. Appendix Inertial Subsystem Mode Switching

Figure A-4. Block I Main D & C (Sheet 1 of 2)

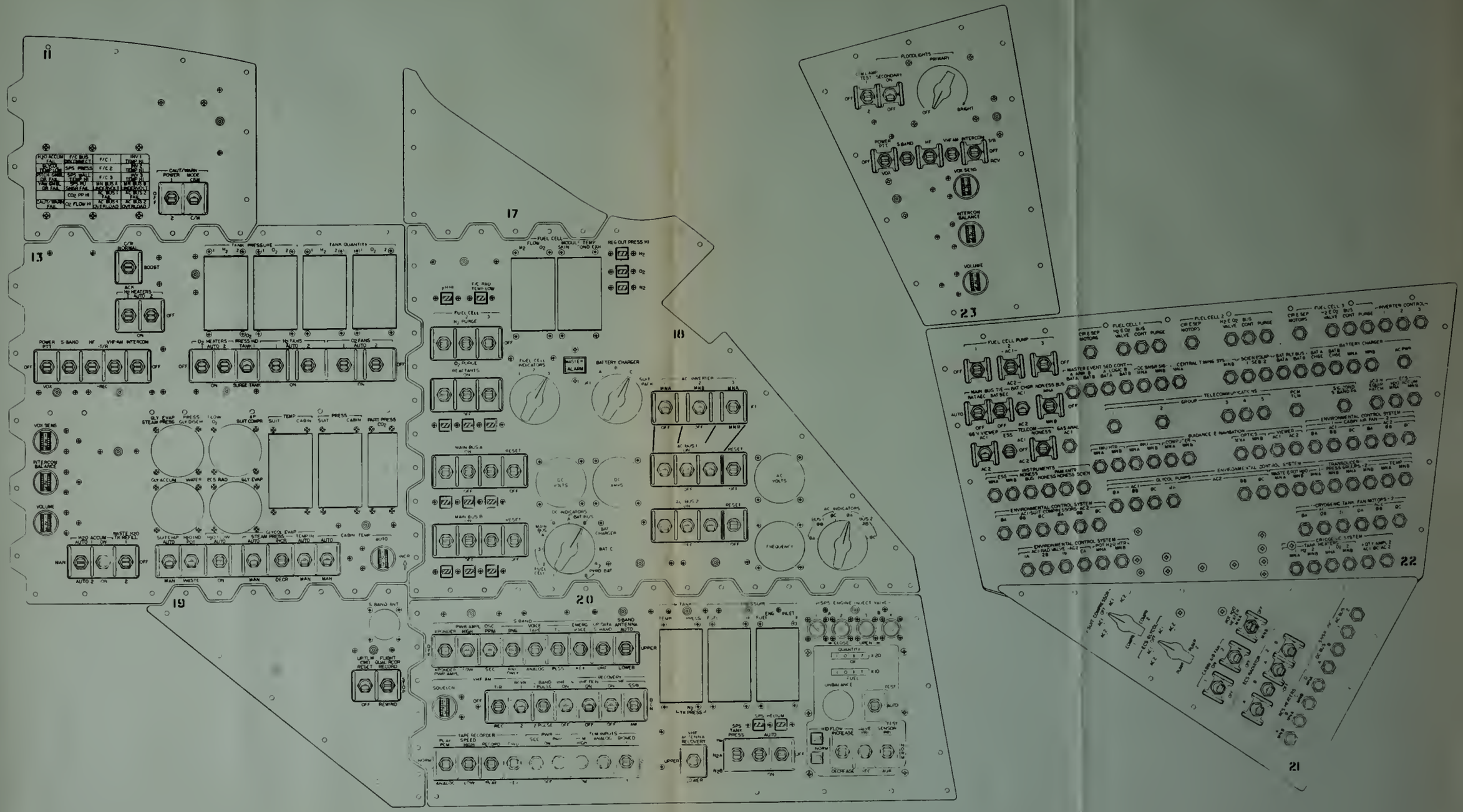


Figure A-4. Block I Main D & C (Sheet 2 of 2)

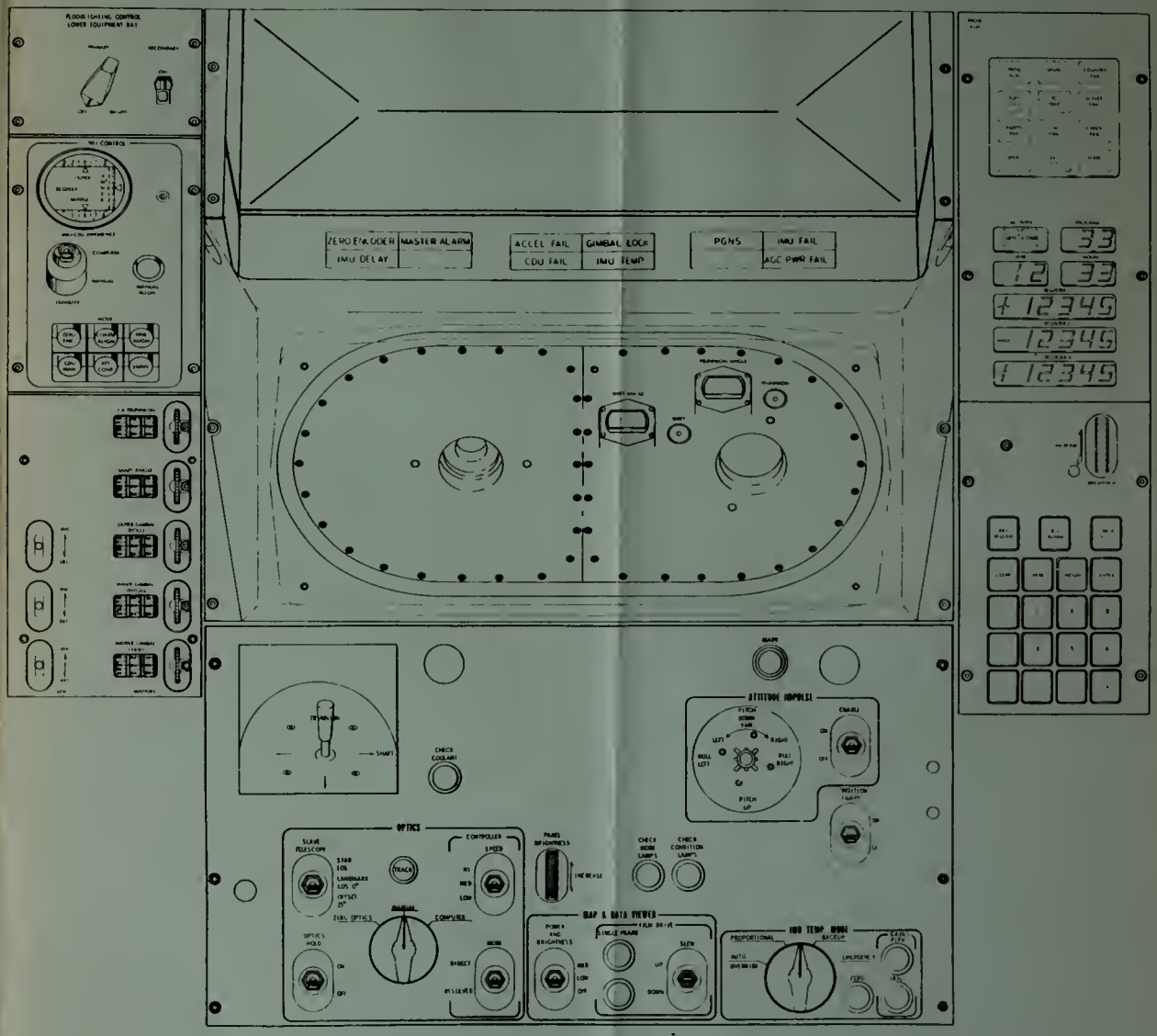


Figure A-5. Block I Lower D & C

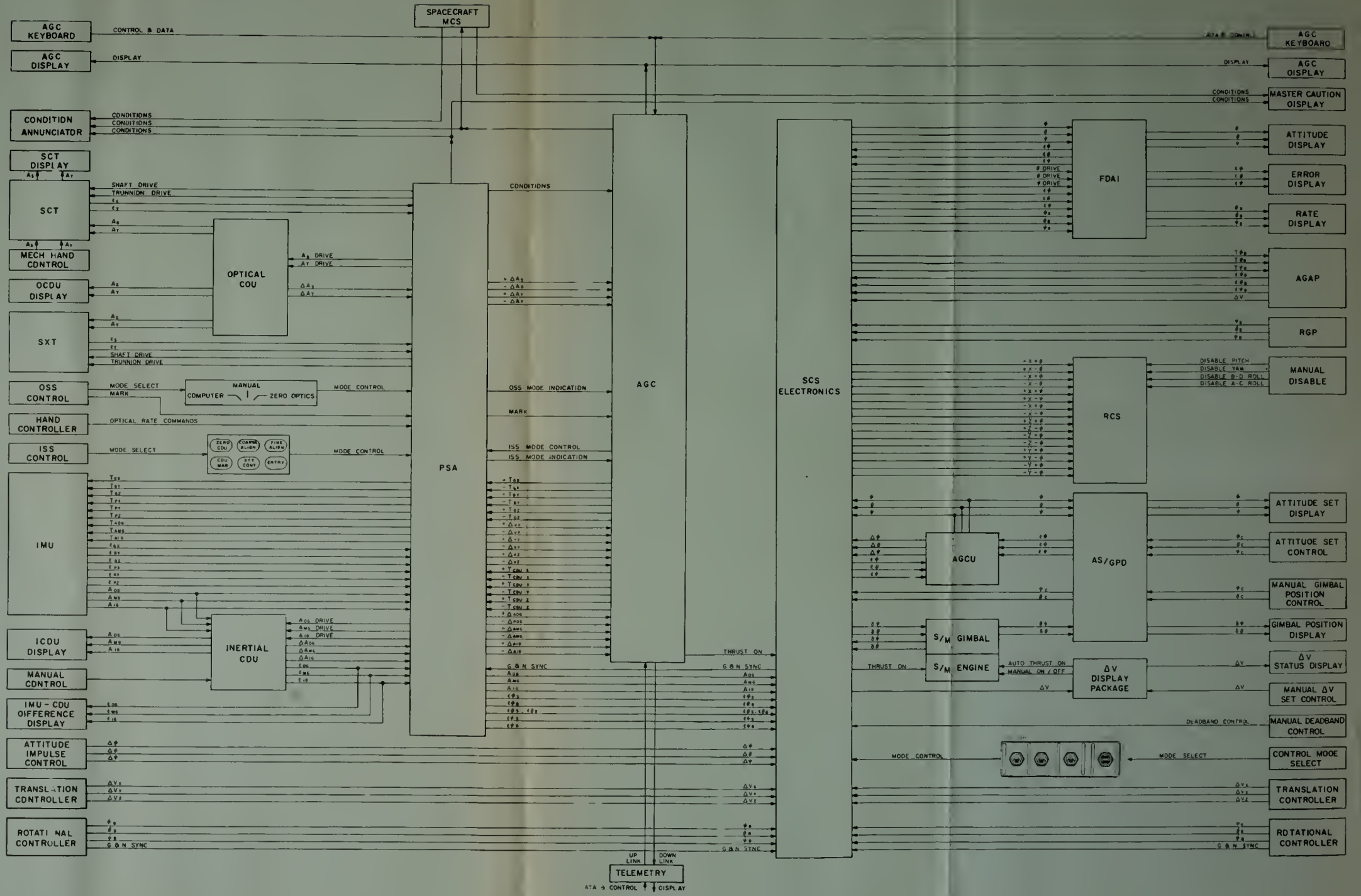


Figure A-6. Guidance, Navigation and Control System Block Diagram, Block I (Series 100)

APPENDIX

ANSWERS TO SECTION I REVIEW QUESTIONS

1. a. Optical navigation - see paragraph 1.3.3

   b. Inertial guidance - see paragraph 1.3.2

2. a. EPS - see paragraph 1.2.1.4

   b. ECS - see paragraph 1.2.1.5

   c. SCS - see paragraph 1.2.1.1

   d. RCS - see paragraph 1.2.1.3

   e. SPS - see paragraph 1.2.1.2

   f. C&IS - see paragraph 1.2.1.6

3. a. Navigation base (NB)

   b. Optical unit

   c. Inertial measurement unit (IMU)

   d. Coupling display units (CDU's)

   e. Power and servo assembly (PSA)

   f. Apollo guidance computer (AGC)

   g. Display and control panels

4. a. Inertial subsystem (ISS)

   b. Optical subsystem (OSS)

   c. Computer subsystem (CSS)

ANSWERS TO SECTION II REVIEW QUESTIONS

1. The two basic functions of the ISS are: (a) attitude control and (b) velocity measurements.

2. The IMU gimbal angles are transferred to the AGC through the three ISS CDU's.

3. The coarse align amplifier amplifys Δ angle (IMU - CDU) signals, the output of which is used to provide rapid alignment of the IMU gimbals.

APPENDIX

ANSWERS TO SECTION III REVIEW QUESTIONS

1. a. ~~False~~ True - 3 IRIGS, 3 PIPS and ~~1~~ (3) ADA

   b. True

   c. False - the ternary current switch torques only the IRIGS

   d. True

   e. True

2. Refer to figure 2-19.

3. The ADA has the purpose of measuring angular acceleration and supplying to the system the differential of the mechanical output. This is accomplished with a torsional pendulum (spring pendulum) and dc pickoff coils. The PIP supplies linear acceleration measurements to the system by means of a mass unbalance pendulum and its output is proportional to the acceleration as measured by an AC signal microsyn.

4. The stabilization amplifier has 2 inputs - an ADA signal (dc) and IRIG signal (ac), both preamplified externally. The ADA input is decoupled and summed with the rectified IRIG signal at the input to the servo amp. The servo amp output is a variable dc to the torque motor.

   The three amplifiers vary in their gain as adjusted by current feedback resistors in the output.

5. The dummy current switch provides a load to the constant current supply when no torquing pulses are sent to the IRIG. This provides better regulation of the current during switching to the torque microsyn.

6. To present a resistive load to the ternary current switch and constant current supply. To equalize its scale factor to the established criteria for all IRIG's.

7. The binary current switch having only 2 states supplies either a positive or negative torque pulse to the PIP. This, combined with the natural frequency of the oscillate at 533-1/3 cps in the 3-3 mode.

8. The purpose of the forward-backward counter is to insure that the data sent to the AGC is an actual gain in velocity. No output during zero G.

ANSWERS TO SECTION IV REVIEW QUESTIONS

1. a. AGC pulsing of the DAC which sends inputs to the MDA. This is done in the coarse align mode.

   b. Manual slew as in the manual CDU mode

   c. Gimbal angle - CDU error controlling the MDA to drive the CDU to the gimbal angle AG in the fine align mode

2. a. To permit visual readout of gimbal angles

   b. To indicate to the AGC, the position of the ISS gimbals

   c. To generate attitude error signals during attitude control

   d. To provide a drive signal to position the gimbals to the CDU shaft angle

3. The CDU is an analog device and the AGC is digital, therefore CDU outputs must be encoded into digital form prior to acceptance by the AGC. AGC inputs must be converted to analog form to be accepted by the CDU.

ANSWERS TO SECTION V REVIEW QUESTIONS

1. a. True. Attitude control and entry are obvious, however, in fine align with the G & N sync switch on and the SCS relay energized, whenever the astronaut establishes a new attitude, the ISS is used to maintain that attitude.

   b. False. The spacecraft axes during entry are parallel with Navigation Base axes as well. In attitude control, the X and Z axes are 33^{o} from the spacecraft axes.

   c. True

   d. True

   e. False. When "manual align" is depressed, the gimbals drive to the CDU angles.

2. The IMU goes into the turn on condition. (1) Prime power is applied to ISS power supplies, (2) a 40 second delay starts its timing cycle, while (3) the system enters the coarse align mode. (4) The wheel power is applied to gyros. (5) After 40 seconds the system enters either the entry or attitude control mode.

3. The purpose is to zero the encoder to the CDU zero angle. When this angle is zero, the computer memory storage for CDU angle pulses is erased and the CDU and computer are referenced.

4. The CDU angles as determined by computer command through the DAC.

ANSWERS TO SECTION VI REVIEW QUESTIONS

1. a. False, the IRIG control sensors control the heater current.

   b. True

   c. False, it will switch to emergency control.

   d. False. The PIP gain simulates overheat, the IRIG gain underheat.

   e. False, the preheater is a part of the thermostat module and has nothing to do with the bias heaters which are on the PIPS.

2. The alarm lamp would be lit and the system would be automatically switched to the emergency mode of operation.

3. There are 9 control heaters and 9 emergency heaters. One control and one emergency heater is found on each PIP and 2 of each type are found on each IRIG. In addition, each PIP has a fixed heater.

4. By pushing the zero button, the alarm circuitry would show up as functionally correct and K2 would energize. This means the problem is in one of the inertial indicating sensors or in the proportional amplifier. If the output of the proportional amplifier were observed at test points and it was found to be operating at a 50% duty cycle of 2 ampere pulses, the control circuit would be assumed to be functioning correctly. All that is left then is the possibility of an open indicating sensor. The bridge voltages may be observed at PSA Tray 7. In this case, the system would maintain temperature most accurately in the proportional mode since the backup mode is not usable.

ANSWERS TO SECTION VII REVIEW QUESTIONS

1. IMU Control
   CDU
   Display and Keyboard
   G & N Indicator
   Condition Annunciator
2. IMU Control
   CDU Panel (3 CDU's Only)
   G & N Indicator (Temp. Control Only)
3. Optics Hand Controller
   To control sextant and telescope movement
   Optics Control Group
   To permit moding of optics equipment
   Attitude Impulse
   To permit movement of the spacecraft by the astronaut while at the D & C
   IMU Temp. Cont.
   To control the modes of the IMU temperature control system

ANSWERS TO SECTION VIII REVIEW QUESTIONS

1. a. False. All ac power supplies have free running multivibrators to supply some frequency control.

   b. False. The IMU heater switch controls 28 vdc and the 3200 cps square and sine wave supplies to the temperature controller and inertial sensors of the ISS.

   c. True

   d. False. The PSA is cooled by conduction of heat to the cold plate.

   e. False. The signal is 0 - 5 vdc.

2. Refer to Figures 7-3 (12 volt dc portion) 7-4, 7-6.

3. Cordwood - encapsulated for vibration and acceleration protection.

   Heatsink - cordwood type but inserted in a heatsink and potted to provide conduction of heat for high power amplifiers and supplies.

ANSWERS TO SECTION IX REVIEW QUESTIONS

1. a. False. Sig. Cond. outputs are DC.

   b. False. The condition annunciator is a visual warning device only.

2. Torque Motor

   CDU Resolver

   Scaling

   IRIG and PIPA

   Gimbal

   Optics

3. The failure detect circuitry sends fail indications to the AGC which then acts on the information along with other inputs to determine if a malfunction actually exists. If it does, the AGC will send an error signal back to ISS to light the appropriate lamp on the condition annunciator.

4. The PGNS lamp would go on in the condition annunciator. The AGC would receive an IMU fail input from the monitor and detect circuit and if the AGC considers it a genuine failure it sends a discrete to the annunciator to light the IMU fail lamp.

ANSWERS TO SECTION X REVIEW QUESTIONS

1. True
2. True
3. False
4. True
5. True
6. False
7. True

ANSWERS TO SECTION XI REVIEW QUESTIONS

1. True
2. False
3. True
4. True
5. c. Parallel to the N/B Z axis.
6. a. 1.8^{o}
7. The SCT can be driven manually and readouts are provided on the SCT front panel.
8. a. The motor-generator flywheels have been lightened.

   b. The electrical connections have been changed.

ANSWERS TO SECTION XII REVIEW QUESTIONS

1. False
2. True
3. True
4. The purpose of the zero optics mode is to drive the SXT, SCT, and CDU's to an initial orientation, and to clear the AGC counters prior to making an optical sighting.
5. The hand controller output is resolved through the shaft angle in order to coarse the star image to move in the X-Y coordination system. Secondly, the shaft drive signal is resolved by the trunnion computing resolver in order to make the star image speed independent of trunnion angle.

ANSWERS TO SECTION XIII REVIEW QUESTIONS

1. A. Apollo Guidance Computer
   B. Navigation panel DSKY
   C. Main panel DSKY
2. Beneath the PSA
3. A. Timer
   B. Sequence Generator
   C. Central Processor
   D. Input-Output
   E. Memory
   F. Priority Control
   G. Power
4. Fixed memory cannot be written into
5. Binary ones complement
6. Through the DSKY's

ANSWERS TO SECTION XIV REVIEW QUESTIONS

1. False
2. False
3. True
4. True
5. False
6. True
7. False
8. False
9. True
10. False
11. False
12. True
13. True

ANSWERS TO SECTION XV REVIEW QUESTIONS

1. False
2. KEY RLSE
3. False
4. On the main panel DSKY
5. False

ANSWERS TO SECTION XVI REVIEW QUESTIONS

1. False
2. False
3. False
4. True
5. False